

Features

- Supply Voltage up to 40V
- Operating Voltage $V_S = 5V$ to 27V
- Typically 10 μA Supply Current During Sleep Mode
- Typically 57 μA Supply Current in Silent Mode
- Linear Low-drop Voltage Regulator:
 - Normal, Fail-safe, and Silent Mode
 - ATA6623: $V_{CC} = 3.3V \pm 2\%$
 - ATA6625: $V_{CC} = 5.0V \pm 2\%$
 - Sleep Mode: V_{CC} is Switched Off
- V_{CC} Undervoltage Detection with Reset Open Drain Output NRES (4 ms Reset Time)
- Voltage Regulator is Short-circuit and Over-temperature Protected
- LIN Physical Layer According to LIN Specification Revision 2.0 and SAEJ2602-2
- Wake-up Capability via LIN Bus (90 μs Dominant)
- TXD Time-out Timer
- Bus Pin is Overtemperature and Short-circuit Protected versus GND and Battery
- Advanced EMC and ESD Performance
- ESD HBM 8 kV at Pins LIN and VS Following STM5.1
- Interference and Damage Protection According to ISO/CD7637
- Package: SO8

1. Description

ATA6623/ATA6625 is a fully integrated LIN transceiver, designed according to the LIN specification 2.0, with a low-drop voltage regulator (3.3V/5V/50 mA). The combination of voltage regulator and bus transceiver makes it possible to develop simple, but powerful, slave nodes in LIN Bus systems. ATA6623/ATA6625 is designed to handle the low-speed data communication in vehicles (for example, in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20 kBaud with an RC oscillator for the protocol handling. The bus output is designed to withstand high voltage. Sleep mode (voltage regulator switched off) and Silent mode (communication off; V_{CC} voltage on) guarantee minimized current consumption.



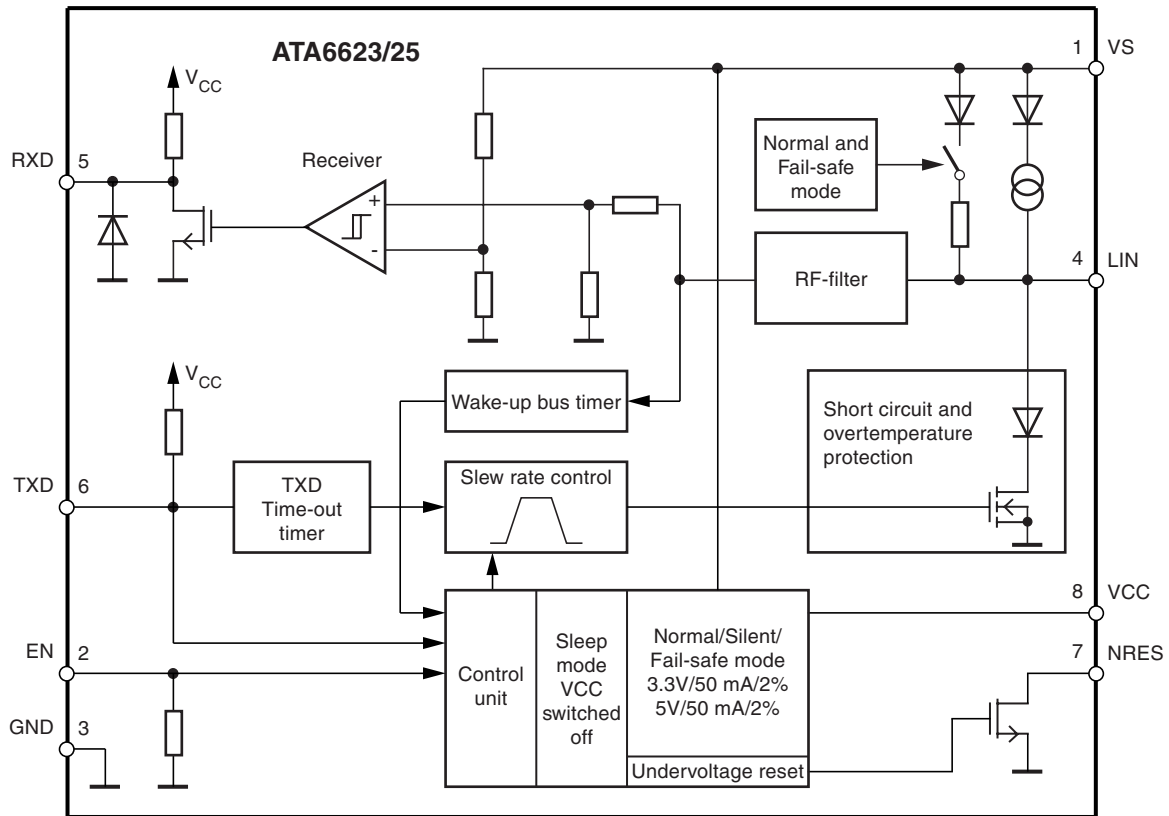
LIN Bus Transceiver with Integrated Voltage Regulator

ATA6623
ATA6625

Preliminary



Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SO8

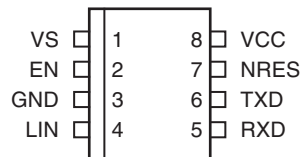


Table 2-1. Pin Description

Pin	Symbol	Function
1	VS	Battery supply
2	EN	Enables Normal mode if the input is high
3	GND	Ground, heat sink
4	LIN	LIN bus line input/output
5	RXD	Receive data output
6	TXD	Transmit data input
7	NRES	Output undervoltage reset, low at reset
8	VCC	Output voltage regulator 3.3V/5V/50 mA

3. Functional Description

3.1 Physical Layer Compatibility

Since the LIN physical layer is independent from higher LIN layers (e.g., LIN protocol layer), all nodes with a LIN physical layer according to revision 2.0 can be mixed with LIN physical layer nodes, which are according to older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

3.2 Supply Pin (VS)

LIN operating voltage is $V_S = 5V$ to $27V$. An undervoltage detection is implemented to disable transmission if V_S falls below $5V$, in order to avoid false bus messages. After switching on V_S , the IC starts with the Fail-safe mode and the voltage regulator is switched on (i.e., $3.3V/5V/50\text{ mA}$).

The supply current in Sleep mode is typically $10\ \mu A$ and $57\ \mu A$ in Silent mode.

3.3 Ground Pin (GND)

The IC is neutral on the LIN pin in the event of GND disconnection. It is able to handle a ground shift up to 11.5% of V_S .

3.4 Voltage Regulator Output Pin (VCC)

The internal $3.3V/5V$ voltage regulator is capable of driving loads with up to 50 mA , supplying the microcontroller and other ICs on the PCB and is protected against overload by means of current limitation and overtemperature shut-down. Furthermore, the output voltage is monitored and will cause a reset signal at the NRES output pin if it drops below a defined threshold V_{thun} .

3.5 Undervoltage Reset Output (NRES)

If the V_{CC} voltage falls below the undervoltage detection threshold of V_{thun} , NRES switches to low after t_{res_f} (Figure 6-1 on page 11). Even if $V_{CC} = 0V$ the NRES stays low, because it is internally driven from the V_S voltage. If V_S voltage ramps down, NRES stays low until $V_S < 1.5V$ and then becomes highly resistant.

The implemented undervoltage delay keeps NRES low for $t_{Reset} = 4\text{ ms}$ after V_{CC} reaches its nominal value.

3.6 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor according to LIN specification 2.0 is implemented. The voltage range is from $-27V$ to $+40V$. This pin exhibits no reverse current from the LIN bus to V_S , even in the event of a GND shift or V_{Batt} disconnection. The LIN receiver thresholds are compatible with the LIN protocol specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled.

3.7 Input Pin (TXD)

In Normal mode the TXD pin is the microcontroller interface to control the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in the recessive state.

3.8 Dominant Time-out Function (TXD)

The TXD input has an internal pull-up resistor. An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than $t_{DOM} > 6$ ms, the LIN bus driver is switched to the recessive state. Nevertheless, when switching to Sleep mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, switch TXD to high (> 10 μ s).

3.9 Output Pin (RXD)

The pin reports the state of the LIN-bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD; LIN low (dominant state) is reported by a low level at RXD. The output has an internal pull-up structure with typically 5 k Ω to V_{CC} . The AC characteristics are measured with an external load capacitor of 20 pF.

The output is short-circuit protected. In Unpowered mode (that is, $V_S = 0$ V), RXD is switched off.

3.10 Enable Input Pin (EN)

This pin controls the Operation mode of the interface. After power up of V_S (battery), the IC switches to Fail-safe mode, even if EN is low or unconnected (internal pull-down resistor). If EN is high, the interface is in Normal mode.

A falling edge at EN while TXD is still high forces the device to Silent mode. A falling edge at EN while TXD is low forces the device to Sleep mode.

4. Mode of Operation

Figure 4-1. Mode of Operation

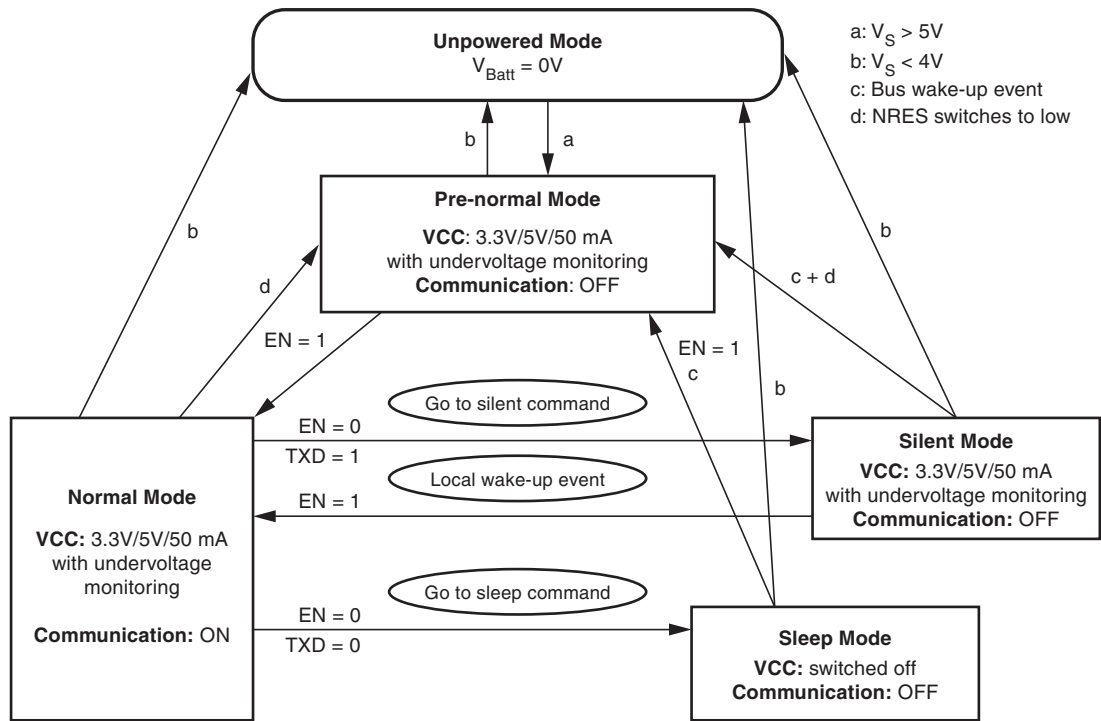


Table 4-1. Mode of Operation

Mode of Operation	Transceiver	V _{CC}	RXD	LIN
Fail safe	OFF	3.3V/5V	High	Recessive
Normal	ON	3.3V/5V	High	TXD depending
Silent	OFF	3.3V/5V	High	Recessive
Sleep	OFF	0V	0V	Recessive

4.1 Normal Mode

This is the normal transmitting and Receiving mode of the LIN Interface, in accordance with LIN specification 2.0. The V_{CC} voltage regulator operates with a 3.3V/5V output voltage, with a low tolerance of $\pm 2\%$ and a maximum output current of 50 mA.

If an undervoltage condition occurs, NRES is switched to low and the IC changes its state to Fail-safe mode. All features are available.

4.2 Silent Mode

A falling edge at EN while TXD is high switches the IC into Silent mode. The TXD Signal has to be logic high during the Mode Select window ([Figure 4-2 on page 7](#)). The transmission path is disabled in Silent mode. The overall supply current from V_{Batt} is a combination of the I_{V_{Ssi} = 57 μ A plus the V_{CC} regulator output current I_{V_{CCs}.}}

The 3.3V/5V regulator with 2% tolerance can source up to 50 mA. In Silent mode the internal slave termination between pin LIN and pin VS is disabled to minimize the power dissipation in case pin LIN is short-circuited to GND. Only a weak pull-up current (typically 10 μ A) between pin LIN and pin VS is present. The Silent mode can be activated independently from the current level on pin LIN.

If an undervoltage condition occurs, NRES is switched to low and the ATA6623/ATA6625 changes its state to Fail-safe mode.

A voltage less than the LIN Pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver.

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (t_{bus}) and the following rising edge at pin LIN (see [Figure 4-3 on page 7](#)) results in a remote wake-up request. The device switches from Silent mode to Fail-safe mode, then the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller ([Figure 4-3 on page 7](#)). EN high can be used to switch directly to Normal mode.

Figure 4-2. Switch to Silent Mode

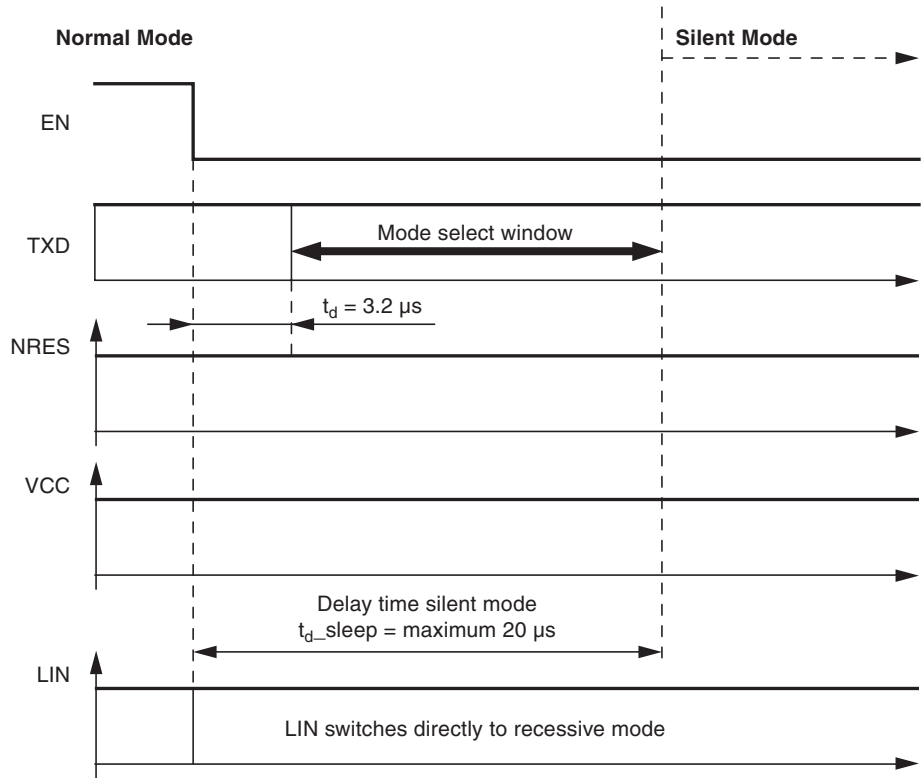
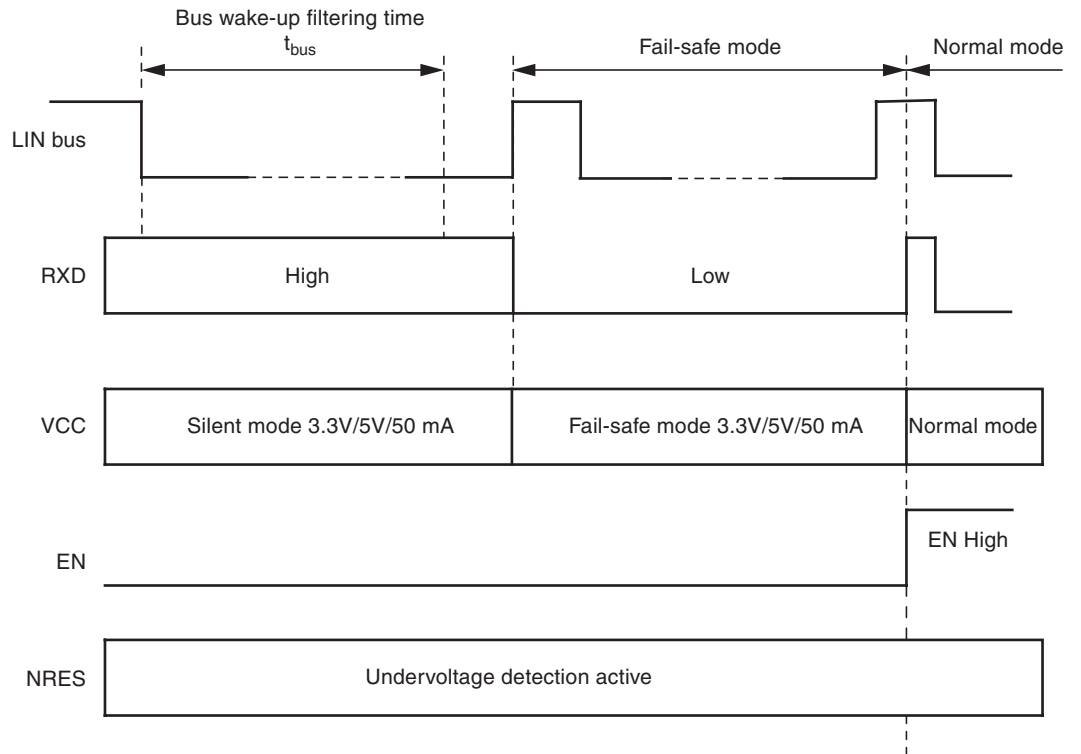


Figure 4-3. LIN Wake-up Waveform Diagram from Silent Mode



4.3 Sleep Mode

A falling edge at EN while TXD is low switches the IC into Sleep mode. The TXD Signal has to be logic low during the Mode Select window (Figure 4-4 on page 8).

In Sleep mode the transmission path is disabled. Supply current from V_{Batt} is typically $I_{V_{Sleep}} = 10 \mu A$. The V_{CC} regulator is switched off; NRES and RXD are low. The internal slave termination between pin LIN and pin VS is disabled to minimize the power dissipation in case pin LIN is short-circuited to GND. Only a weak pull-up current (typically $10 \mu A$) between pin LIN and pin VS is present. The Sleep mode can be activated independently from the current level on pin LIN.

A voltage less than the LIN Pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver.

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (t_{bus}) and a following rising edge at pin LIN respectively results in a remote wake-up request. The device switches from Sleep mode to Fail-safe mode.

The V_{CC} regulator is activated, and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at the RXD pin to interrupt the microcontroller (Figure 4-5 on page 9).

EN high can be used to switch directly from Sleep/Silent to Fail-safe mode. If EN is still high after VCC ramp up and undervoltage reset time, the IC switches to Normal mode.

Figure 4-4. Switch to Sleep Mode

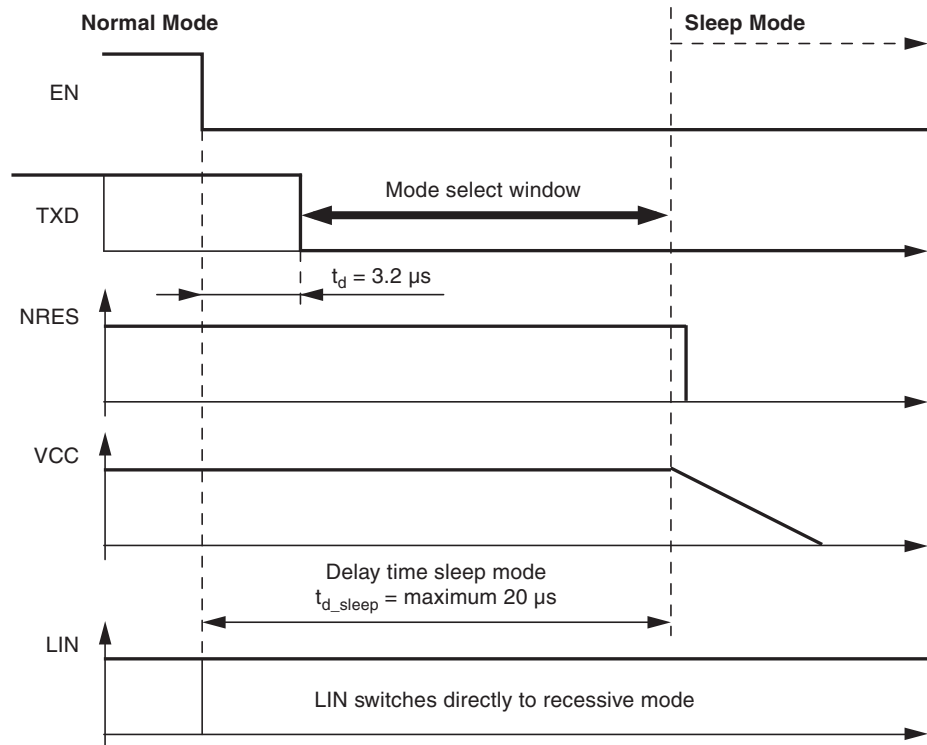
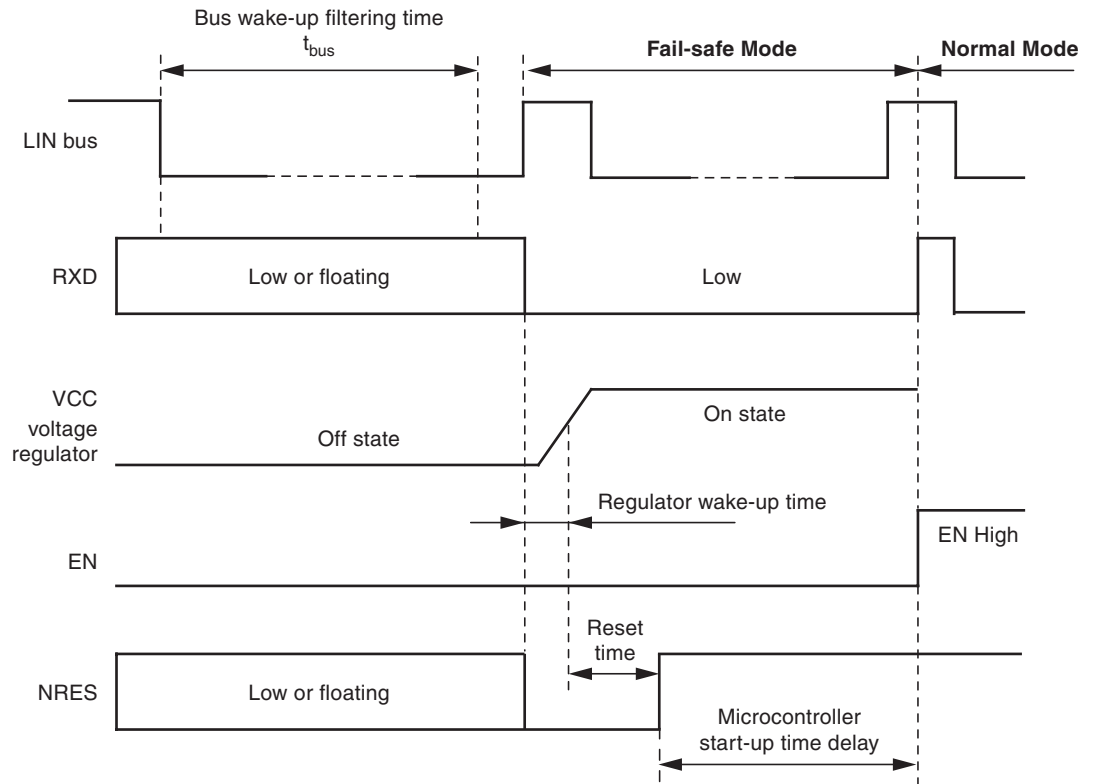


Figure 4-5. LIN Wake-up Diagram from Sleep Mode



4.4 Fail-safe Mode

At system power-up the device automatically switches to Fail-safe mode. The voltage regulator is switched on ($V_{CC} = 3.3V/5V/50\text{ mA}$), (see [Figure 6-1 on page 11](#)). The NRES output switches to low for $t_{res} = 4\text{ ms}$ and gives a reset to the microcontroller. LIN communication is switched off. The IC stays in this mode until EN is switched to high, and changes then to the Normal mode. A power down of V_{Batt} ($V_S < 4V$) during Silent- or Sleep mode switches the IC into the Fail-safe mode after power up. A logic low at NRES switches the IC into Fail-safe mode directly.

4.5 Unpowered Mode

If you connect battery voltage to the application circuit, the voltage at the VS pin increases according to the block capacitor (see [Figure 6-1 on page 11](#)). After VS is higher than the VS undervoltage threshold $V_{S_{th}}$, the IC mode changes from Unpowered mode to Fail-safe mode. The VCC output voltage reaches its nominal value after t_{VCC} . This time, t_{VCC} , depends on the VCC capacitor and the load.

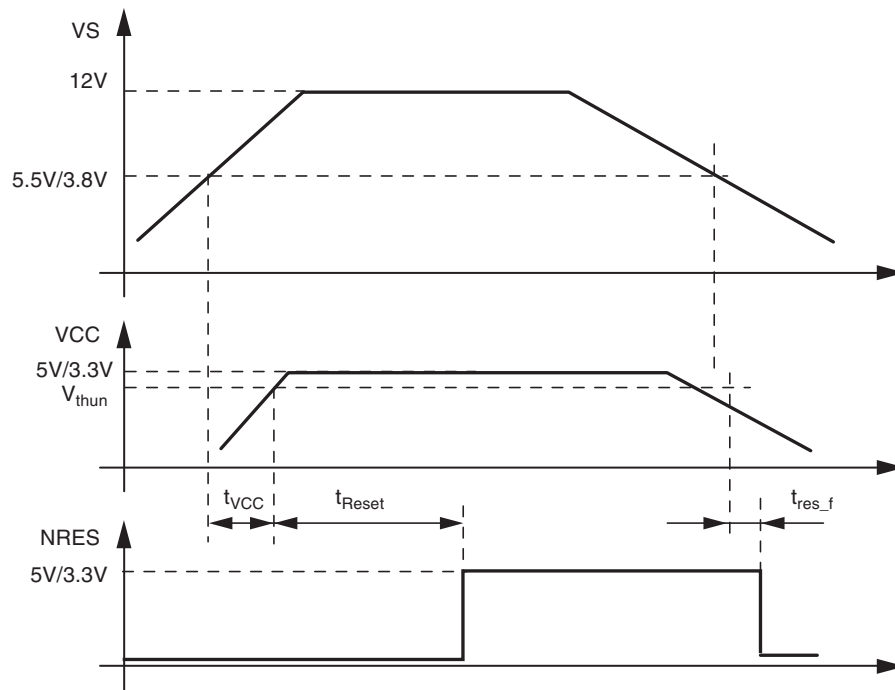
NRES is low for the reset time delay t_{Reset} ; no mode change is possible during this time.

5. Fail-safe Features

- During a short-circuit at LIN to V_{Battery} , the output limits the output current to $I_{\text{BUS_LIM}}$. Due to the power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys} , switches the output on again. RXD stays on high because LIN is high. During LIN overtemperature switch-off, the V_{CC} regulator is working independently.
- During a short-circuit from LIN to GND the IC can be switched into Sleep or Silent mode. If the short-circuit disappears, the IC starts with a remote wake-up.
- The reverse current is very low $< 15 \mu\text{A}$ at pin LIN during loss of V_{Batt} or GND. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.
- During a short circuit at VCC, the output limits the output current to I_{VCCn} . Because of undervoltage, NRES switches to low and sends a reset to the microcontroller. The IC switches into Fail-safe mode. If the chip temperature exceeds the value T_{VCCoff} , the V_{CC} output switches off. The chip cools down and after a hysteresis of T_{hys} , switches the output on again. Because of Fail-safe mode, the V_{CC} voltage will switch on again although EN is switched off from the microcontroller. The microcontroller can then start with normal operation.
- Pin EN provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.
- Pin RXD is set floating if V_{Batt} is disconnected.
- Pin TXD provides a pull-up resistor to force the transceiver into recessive mode if TXD is disconnected.
- If TXD is short-circuited to GND, it is possible to switch to Sleep mode via ENABLE after $t_{\text{dom}} > 20 \text{ ms}$.

6. Voltage Regulator

Figure 6-1. V_{CC} Voltage Regulator: Ramp Up and Undervoltage



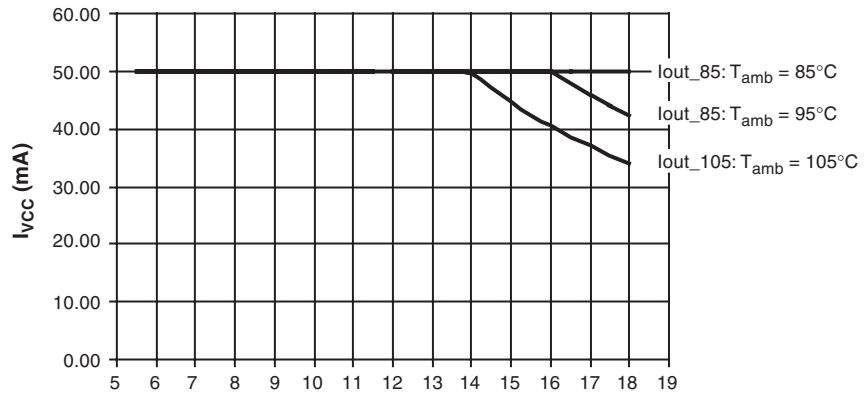
The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommended to use an electrolytic capacitor with $C > 10 \mu\text{F}$ and a ceramic capacitor with $C = 100 \text{ nF}$. The values of these capacitors can be varied by the customer, depending on the application.

With this special SO8 package (fused lead frame to pin3) an R_{thja} of 80 K/W is achieved. Therefore, it is recommended to connect pin 3 with a wide GND plate on the printed board to get a good heat sink.

The main power dissipation of the IC is created from the V_{CC} output current I_{VCC} , which is needed for the application.

Figure 6-2 shows the safe operating area of the ATA6623/ATA6625.

Figure 6-2. Power Dissipation: Save Operating Area versus V_{CC} Output Current and Supply Voltage V_S at Different Ambient Temperatures Due to $R_{thja} = 80 \text{ K/W}$



For programming purposes of the microcontroller it is potentially necessary to supply the V_{CC} output via an external power supply while the V_S Pin of the system basis chip is disconnected. This behavior is no problem for the system basis chip.

7. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage V_S	V_S	-0.3		+40	V
Pulse time ≤ 500 ms $T_a = 25^\circ\text{C}$ Output current $I_{VCC} \leq 50$ mA	V_S			+40	V
Pulse time ≤ 2 min $T_a = 25^\circ\text{C}$ Output current $I_{VCC} \leq 50$ mA	V_S			27	V
Logic pins (RxD, TxD, EN, NRES)		-0.3		+5.5	V
Output current NRES	I_{NRES}			+2	mA
LIN - DC voltage		-27		+40	V
V_{CC} - DC voltage		-0.3		+5.5	V
According to IBEE LIN EMC Test specification 1.0 following IEC 61000-4-2 - Pin VS, LIN to GND		± 6			KV
ESD HBM following STM5.1 with $1.5\text{ k}\Omega/100\text{ pF}$ - Pin VS, LIN to GND		± 8			KV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		± 3			KV
CDM ESD STM 5.3.1		± 750			V
Junction temperature	T_j	-40		+150	$^\circ\text{C}$
Storage temperature	T_s	-55		+150	$^\circ\text{C}$
Operating ambient temperature	T_a	-40		+125	$^\circ\text{C}$
Thermal resistance junction to ambient (free air)	R_{thja}			145	K/W
Special heat sink at GND (pin 3) on PCB	R_{thja}		80		K/W
Thermal shutdown of V_{CC} regulator	T_{VCCoff}	150	160	170	$^\circ\text{C}$
Thermal shutdown of LIN output	T_{LINoff}	150	160	170	$^\circ\text{C}$
Thermal shutdown hysteresis	T_{hys}		10		$^\circ\text{C}$

8. Electrical Characteristics

$5V < V_S < 27V$, $-40^{\circ}C < T_j < 150^{\circ}C$; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	VS Pin								
1.1	Nominal DC voltage range		VS	V_S	5	13.5	27	V	A
1.2	Supply current in Sleep mode	Sleep mode $V_{LIN} > V_S - 0.5V$ $V_S < 14V$ ($T_j = 25^{\circ}C$)	VS	$I_{VSsleep}$	3	10	14	μA	A
		Sleep mode $V_{LIN} > V_S - 0.5V$ $V_S < 14V$ ($T_j = 125^{\circ}C$)		$I_{VSsleep}$	5	11	16	μA	A
1.3	Supply current in Silent mode	Bus recessive $V_S < 14V$ ($T_j = 25^{\circ}C$) Without load at VCC		I_{VSsi}	47	57	67	μA	A
		Bus recessive $V_S < 14V$ ($T_j = 125^{\circ}C$) Without load at VCC		I_{VSsi}	56	66	76	μA	A
1.4	Supply current in Normal mode	Bus recessive $V_S < 14V$ Without load at VCC	VS	I_{VSrec}	0.3		0.8	mA	A
1.5	Supply current in Normal mode	Bus dominant $V_S < 14V$ VCC load current 50 mA	VS	I_{VSdom}	50		53	mA	A
1.6	V_S undervoltage threshold		VS	V_{Sth}	4.0	4.5	5	V	A
1.7	VS undervoltage threshold hysteresis		VS	V_{Sth_hys}		0.2		V	A
2	RXD Output Pin								
2.1	Low level input current	Normal mode $V_{LIN} = 0V$ $V_{RXD} = 0.4V$	RXD	I_{RXD}	1.3	2.5	8	mA	A
2.2	Low level output voltage	$I_{RXD} = 1\text{ mA}$	RXD	V_{RXDL}			0.4	V	A
2.3	Internal resistor to VCC		RXD	R_{RXD}	3	5	7	k Ω	A
3	TXD Input Pin								
3.1	Low level voltage input		TXD	V_{TXDL}	-0.3		+0.8	V	A
3.2	High level voltage input		TXD	V_{TXDH}	2		$V_{CC} + 0.3V$	V	A
3.3	Pull-up resistor	$V_{TXD} = 0V$	TXD	R_{TXD}	125	250	400	k Ω	A
3.4	High level leakage current	$V_{TXD} = 5V$	TXD	I_{TXD}	-3		+3	μA	A
4	EN Input Pin								
4.1	Low level voltage input		EN	V_{ENL}	-0.3		+0.8	V	A
4.2	High level voltage input		EN	V_{ENH}	2		$V_{CC} + 0.3V$	V	A
4.3	Pull-down resistor	$V_{EN} = 5V$	EN	R_{EN}	50	125	200	k Ω	A
4.4	Low level input current	$V_{EN} = 0V$	EN	I_{EN}	-3		+3	μA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 27V, -40°C < T_J < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5	NRES Open Drain Output Pin								
5.1	Low level output voltage	V _S ≥ 5.5V I _{NRES} = 1 mA I _{NRES} = 250 μA	NRES	V _{NRESL} V _{NRESL}			0.2 0.14	V V	A A
5.2	Low level output low	10 kΩ to V _{CC} V _{CC} = 0V	NRES	V _{NRESLL}			0.2	V	A
5.3	Undervoltage reset time	V _{VS} ≥ 5.5V C _{NRES} = 20 pF	NRES	t _{Reset}	2	4	6	ms	A
5.4	Reset debounce time for falling edge	V _{VS} ≥ 5.5V C _{NRES} = 20 pF	NRES	t _{res_f}	1.5		10	μs	A
6	VCC Voltage Regulator ATA6623								
6.1	Output voltage V _{CC}	4V < V _S < 18V (0 mA to 50 mA)	VCC	V _{CCnor}	3.234		3.366	V	A
6.2	Output voltage V _{CC} at low V _S	3V < V _S < 4V	VCC	V _{CClow}	V _{VS} - V _{Drop}		3.366	V	A
6.3	Regulator drop voltage	V _S > 3V, I _{VCC} = -15 mA	VCC	V _{Drop1}			200	mV	A
6.4	Regulator drop voltage	V _S > 3V, I _{VCC} = -50 mA	VCC	V _{Drop2}		500	700	mV	A
6.5	Line regulation maximum	4V < V _S < 18V	VCC	V _{CCline}			1	%	A
6.6	Load regulation maximum	5 mA < I _{VCC} < 50 mA	VCC	V _{CCload}		0.5	2	%	A
6.7	Power supply ripple rejection	10 Hz to 100 kHz C _{VCC} = 10 μF V _S = 14V, I _{VCC} = -15 mA			50			dB	C
6.8	Output current limitation	V _S > 4V	VCC	I _{VCCs}	-200	-160		mA	A
6.9	Load capacity	1Ω < ESR < 5Ω @ 100 kHz	VCC	C _{load}	1.8	10		μF	D
6.10	VCC undervoltage threshold	Referred to VCC V _S > 4V	VCC	V _{thunN}	2.8		3.2	V	A
6.11	Hysteresis of undervoltage threshold	Referred to VCC V _S > 4V	VCC	V _{hys_thun}		150		mV	A
6.12	Ramp up time V _S > 4V to V _{CC} = 3.3V	C _{VCC} = 2.2 μF I _{load} = -5 mA at VCC	VCC	t _{VCC}		100	250	μs	A
7	VCC Voltage Regulator ATA6625								
7.1	Output voltage V _{CC}	5.5V < V _S < 18V (0 mA to 50 mA)	VCC	V _{CCnor}	4.9		5.1	V	A
7.2	Output voltage V _{CC} at low V _S	4V < V _S < 5.5V	VCC	V _{CClow}	V _{VS} - V _D		5.1	V	A
7.3	Regulator drop voltage	V _S > 4V, I _{VCC} = -20 mA	VCC	V _{D1}			250	mV	A
7.4	Regulator drop voltage	V _S > 4V, I _{VCC} = -50 mA	VCC	V _{D2}		400	600	mV	A
7.5	Regulator drop voltage	V _S > 3.3V, I _{VCC} = -15 mA	VCC	V _{D3}			200	mV	A
7.6	Line regulation maximum	5.5V < V _S < 18V	VCC	V _{CCline}			1	%	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 27V, -40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.7	Load regulation maximum	5 mA < I _{VCC} < 50 mA	VCC	VCC _{load}		0.5	2	%	A
7.8	Output current limitation	V _S > 5.5V	VCC	I _{VCCs}	-200	-160		mA	A
7.9	Load capacity	1Ω < ESR < 5Ω @ 100 kHz	VCC	C _{load}	1.8	10		μF	D
7.10	VCC undervoltage threshold	Referred to VCC V _S > 5.5V	VCC	V _{thunN}	4.2		4.8	V	A
7.11	Hysteresis of undervoltage threshold	Referred to VCC V _S > 5.5V	VCC	V _{hys_{thun}}		250		mV	A
7.12	Ramp up time V _S > 5.5V to VCC = 5V	C _{VCC} = 2.2 μF I _{load} = -5 mA at VCC	VCC	T _{VCC}		130	300	μs	A
8	LIN Bus Driver: Bus Load Conditions: Load 1 (Small): 1 nF, 1 kΩ; Load 2 (Large): 10 nF, 500Ω; R_{RXD} = 5 kΩ; C_{RXD} = 20 pF 10.5, 10.6 and 10.7 Specifies the Timing Parameters for Proper Operation at 20 Kbps								
8.1	Driver recessive output voltage	Load1/Load2	LIN	V _{BUSrec}	0.9 × V _S		V _S	V	A
8.2	Driver dominant voltage	V _{VS} = 7V R _{load} = 500Ω	LIN	V _{LoSUP}			1.2	V	A
8.3	Driver dominant voltage	V _{VS} = 18V R _{load} = 500Ω	LIN	V _{HiSUP}			2	V	A
8.4	Driver dominant voltage	V _{VS} = 7V R _{load} = 1000Ω	LIN	V _{LoSUP_1k}	0.6			V	A
8.5	Driver dominant voltage	V _{VS} = 18V R _{load} = 1000Ω	LIN	V _{HiSUP_1k}	0.8			V	A
8.6	Pull-up resistor to V _S	The serial diode is mandatory	LIN	R _{LIN}	20	30	60	kΩ	A
8.7	LIN current limitation V _{BUS} = V _{Batt_max}		LIN	I _{BUS_LIM}	40	120	200	mA	A
8.8	Input leakage current at the receiver including pull-up resistor as specified	Input Leakage current Driver off V _{BUS} = 0V V _{Batt} = 12V	LIN	I _{BUS_PAS_dom}	-1	-0.35		mA	A
8.9	Leakage current LIN recessive	Driver off 8V < V _{Batt} < 18V 8V < V _{BUS} < 18V V _{BUS} ≥ V _{Batt}	LIN	I _{BUS_PAS_rec}		15	20	μA	A
8.10	Leakage current when control unit disconnected from ground. Loss of local ground must not affect communication in the residual network	GND _{Device} = V _S V _{Batt} = 12V 0V < V _{BUS} < 18V	LIN	I _{BUS_NO_gnd}	-10	+0.5	+10	μA	A
8.11	Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	V _{Batt} disconnected V _{SUP_Device} = GND 0V < V _{BUS} < 18V	LIN	I _{BUS}		5	15	μA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 27V, -40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9	LIN Bus Receiver								
9.1	Center of receiver threshold	$V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2$	LIN	V _{BUS_CNT}	$0.475 \times V_S$	$0.5 \times V_S$	$0.525 \times V_S$	V	A
9.2	Receiver dominant state	V _{EN} = 5V	LIN	V _{BUSdom}	-27		$0.4 \times V_S$	V	A
9.3	Receiver recessive state	V _{EN} = 5V	LIN	V _{BUSrec}	$0.6 \times V_S$		40	V	A
9.4	Receiver input hysteresis	V _{hys} = V _{th_rec} - V _{th_dom}	LIN	V _{BUShys}	$0.028 \times V_S$	$0.1 \times V_S$	$0.175 \times V_S$	V	A
9.5	Pre-wake detection LIN High level input voltage		LIN	V _{LINH}	V _S - 1V		V _S + 0.3V	V	A
9.6	Pre-wake detection LIN Low level input voltage	Activates the LIN receiver	LIN	V _{LINL}	-27		V _S - 3.3V	V	A
10	Internal Timers								
10.1	Dominant time for wake-up via LIN bus	V _{LIN} = 0V		t _{bus}	30	90	150	μs	A
10.2	Time delay for mode change from Pre-normal into Normal mode via pin EN	V _{EN} = 5V		t _{norm}	5		20	μs	A
10.3	Time delay for mode change from Normal mode to Sleep mode via pin EN	V _{EN} = 0V		t _{sleep}	2	7	15	μs	A
10.4	TXD dominant time out timer	V _{TXD} = 0V		t _{dom}	6	13	20	ms	A
10.5	Duty cycle 1	TH _{Rec(max)} = 0.744 × V _S TH _{Dom(max)} = 0.581 × V _S V _S = 7.0V to 18V t _{Bit} = 50 ms D1 = t _{bus_rec(min)} / (2 × t _{Bit})		D1	0.396				A
10.6	Duty cycle 2	TH _{Rec(min)} = 0.422 × V _S TH _{Dom(min)} = 0.284 × V _S V _S = 7.6V to 18V t _{Bit} = 50 ms D2 = t _{bus_rec(max)} / (2 × t _{Bit})		D2			0.581		A
10.7	Duty cycle 3	TH _{Rec(max)} = 0.778 × V _S TH _{Dom(max)} = 0.616 × V _S V _S = 7.0V to 18V t _{Bit} = 96 ms D3 = t _{bus_rec(min)} / (2 × t _{Bit})		D3	0.417				A
10.8	Duty cycle 4	TH _{Rec(min)} = 0.389 × V _S TH _{Dom(min)} = 0.251 × V _S V _S = 7.6V to 18V t _{Bit} = 96 ms D4 = t _{bus_rec(max)} / (2 × t _{Bit})		D4			0.590		A
10.9	Slope time falling and rising edge at LIN	V _S = 7.0V to 18V		t _{SLOPE_fall} t _{SLOPE_rise}	3.5		22.5	μs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 27V, -40°C < T_J < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
11	Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions (C_{RXD}): 20 pF; R_{pull-up} = 2.4 kΩ								
11.1	Propagation delay of receiver Figure 8-1	V _S = 7.0V to 18V t _{rx_pd} = max(t _{rx_pdr} , t _{rx_pdf})		t _{rx_pd}			6	μs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	V _S = 7.0V to 18V t _{rx_sym} = t _{rx_pdr} - t _{rx_pdf}		t _{rx_sym}	-2		+2	μs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 8-1. Definition of Bus Timing Characteristics

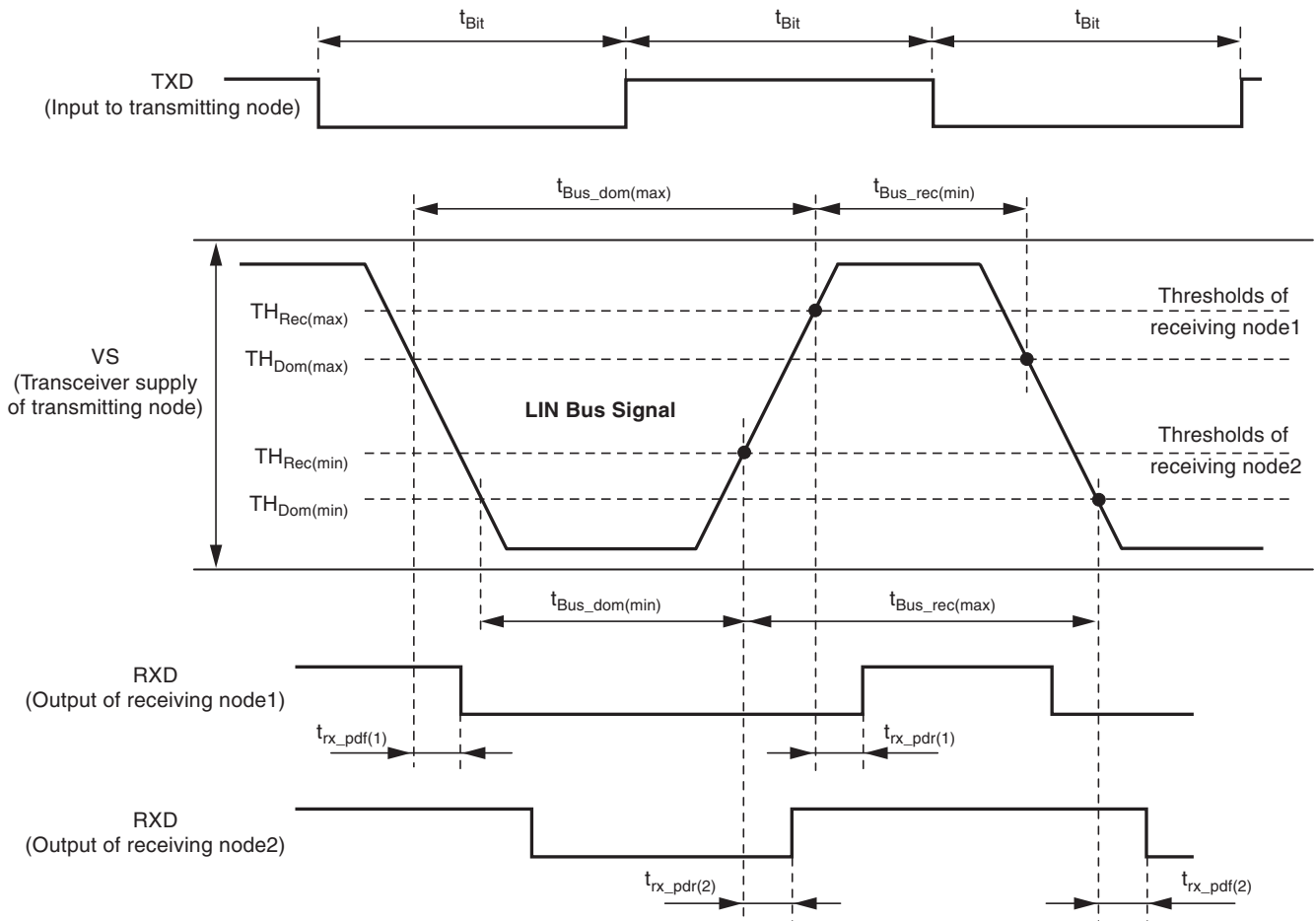
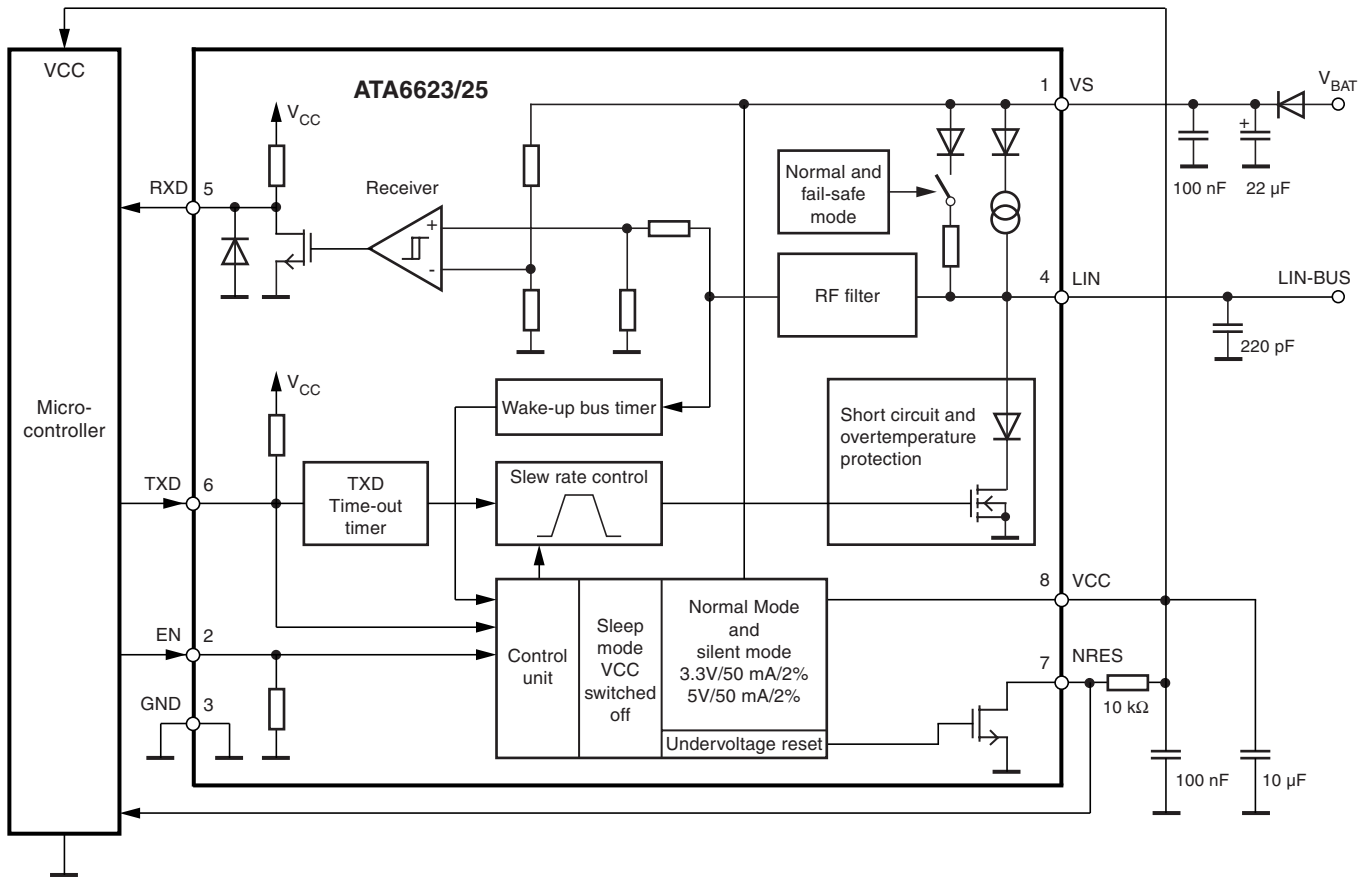


Figure 8-2. Application Circuit



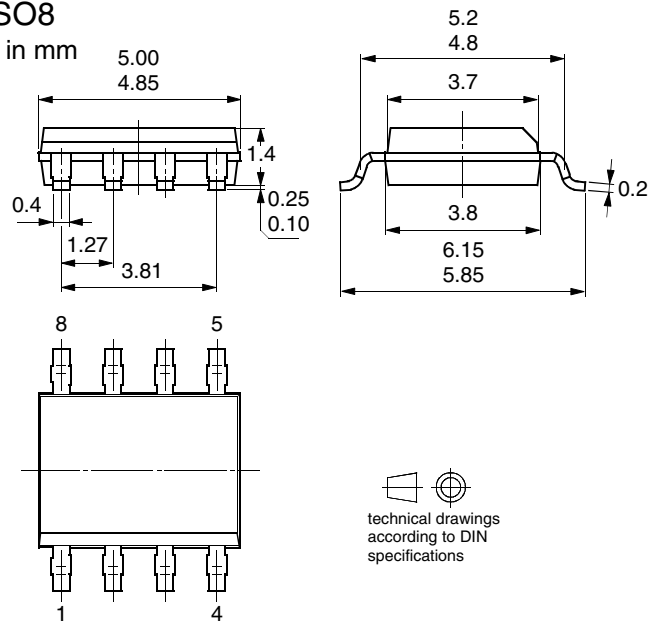
9. Ordering Information

Extended Type Number	Package	Remarks
ATA6623-TAQY	SO8	3.3V LIN system basis chip, Pb-free, 4k, taped and reeled
ATA6625-TAQY	SO8	5V LIN system basis chip, Pb-free, 4k, taped and reeled
ATA6623-TAPY	SO8	3.3V LIN system basis chip, Pb-free, 1k, taped and reeled
ATA6625-TAPY	SO8	5V LIN system basis chip, Pb-free, 1k, taped and reeled

10. Package Information

Package SO8

Dimensions in mm



11. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4957D-AUTO-07/07	<ul style="list-style-type: none"> • Features changed • Block diagram changed • Application diagram changed • Text changed under the headings: 3.2, 3.3, 3.4, 3.6, 3.7, 3.8, 3.9, 4, 4.1, 4.2, 4.3, 4.4, 4.5, 5.5, 5.6, 6 • Figure 4-2, 4-3, 4-4, 4-5, 8-2: changed • Figure title 6-1: text changed • Abs. Max. Ratings: row “Output current NRES” added • El. Char. table: values changed in the following rows: 1.3, 5.1, 5.3, 5.4, 6.9, 6.12, 7.9, 11.1
4957C-AUTO-02/07	<ul style="list-style-type: none"> • Features on page 1 changed • Table 2-1 “Pin Description” on page 2 changed • Section 3-1 “Physical Layer Compatibility” on page 3 added • Section 3-2 “Supply Pin (VS) on page 3 changed • Section 3-3 “Ground Pin (GND) on page 3 changed • Section 3-8 “Dominant Time-out Function (TXD)” on page 4 changed • Section 4-1 “Normal Mode” on page 5 changed • Section 4-2 “Silent Mode” on page 5 changed • Figure 4-3 “LIN Wake-up Waveform Diagram from Silent Mode” on page 6 changed • Section 4.3 “Sleep Mode” on page 7 changed • Section 4-5 “Unpowered Mode” on page 7 changed • Figure 4-4 “Switch to Sleep Mode” on page 8 changed • Figure 4-6 “V_{CC} Voltage Regulator: Ramp up and Undervoltage” on page 9 changed • Section 5 “Fail-safe Features on page 9 changed • Section 6 “Voltage Regulator” on page 10 changed • Section 7 “Absolute Maximum Ratings” on page 11 changed • Section 8 “Electrical Characteristics” on pages 12 to 16 changed • Section 9 “Ordering Information” on page 18 changed



Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
auto_control@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© 2007 Atmel Corporation. All rights reserved. Atmel®, logo and combinations thereof, and others are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.