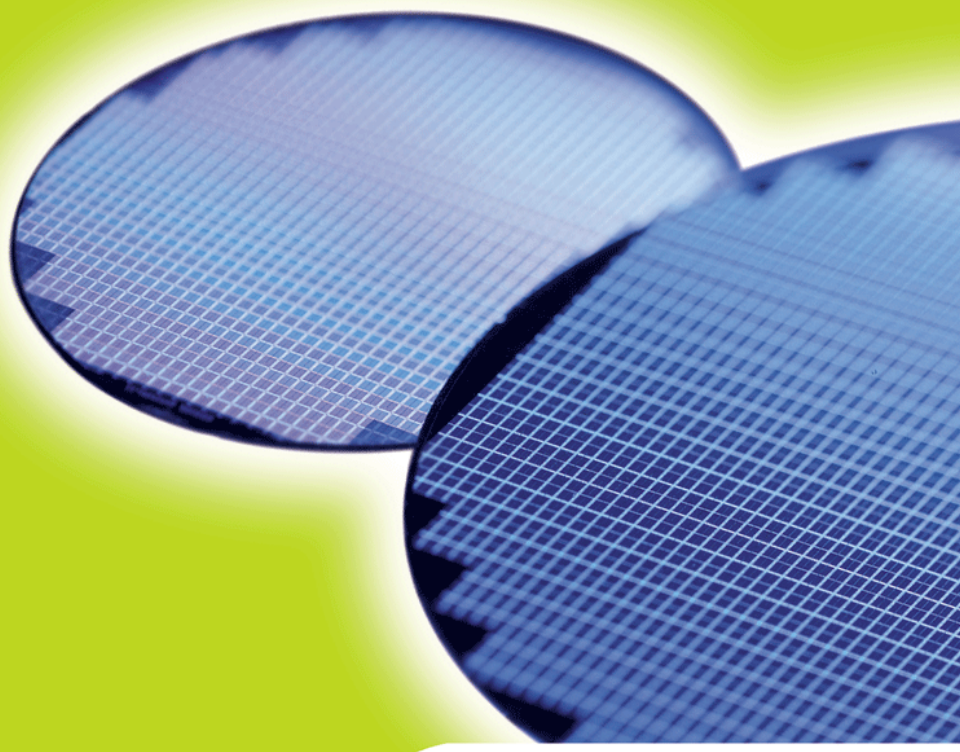
November 2006

HYB18M512160BFX-7.5

DRAMs for Mobile Applications
512-Mbit DDR Mobile-RAM
RoHS compliant



Data Sheet

Rev. 1.10

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HYB18M512160BFX-7.5, ,	
Revision History: 2006-11, Rev. 1.10	
Page	**Subjects (major changes since last revision)**
All	Qimonda Update
Pg 49	I_{DD6} is changed from 2.5mA to 2mA

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1 Overview

1.1 Features

- 4 banks × 8 Mbit × 16 organization
- Double-data-rate architecture : two data transfers per clock cycle
- Bidirectional data strobe (DQS) is transmitted / received with data; to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs and center-aligned with data for WRITEs
- Differential clock input (CK / $\overline{CK}$)
- Commands entered on positive CK edge; data and mask data are referenced to both edges of DQS
- Four internal banks for concurrent operation
- Programmable CAS latency: 2 and 3
- Programmable burst length: 2, 4, 8 and 16
- Programmable drive strength (full, half, quarter)
- Auto refresh and self refresh modes
- 8192 refresh cycles / 64ms
- Auto precharge
- Commercial (0°C to +70°C) operating temperature range
- TS pad to support Super-Extended temperature range
- 60-ball Very Thin FBGA package (10.5 × 10.5 × 1.0 mm)
- RoHS Compliant Product[1)]

Power Saving Features

- Low supply voltages: V_{DD} = 1.70 V – 1.90 V, V_{DDQ} = 1.70 V – 1.90 V
- Optimized operating (I_{DD0} , I_{DD4}), self refresh (I_{DD6}) and standby currents (I_{DD2} , I_{DD3})
- DDR I/O scheme with no DLL
- Programmable Partial Array Self Refresh (PASR)
- Temperature Compensated Self-Refresh (TCSR), controlled by on-chip temperature sensor
- Clock Stop, Power-Down and Deep Power-Down modes

Table 1 Performance

Part Number Speed Code		- 7.5	Unit
Clock Frequency (f_{CKmax})	CL = 3	133	MHz
	CL = 2	66	MHz
Access Time (t_{ACmax})		6.5	ns

Table 2 Memory Addressing Scheme

Item	Addresses
Banks	BA0, BA1
Rows	A0 - A12
Columns	A0 - A9

1)RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

Table 3 Ordering Information

Type[1)]	Package	Description
Commercial Temperature Range		
HYB18M512160BFX-7.5	P-VFBGA-60-1	133 MHz 4 Banks × 8 Mbit × 16 Low Power DDR SDRAM

1) HYB: Designator for memory products (HYB: standard temp. range)
18M: 1.8V DDR Mobile-RAM
512: 512 MBit density
160: 16 bit interface width
B: die revision
F: green product
-7.5: speed grades (min. clock cycle time)

1.2 Pin Configuration

1	2	3		7	8	9
V_{SS}	DQ15	V_{SSQ}	A	V_{DDQ}	DQ0	V_{DD}
V_{DDQ}	DQ13	DQ14	B	DQ1	DQ2	V_{SSQ}
V_{SSQ}	DQ11	DQ12	C	DQ3	DQ4	V_{DDQ}
V_{DDQ}	DQ9	DQ10	D	DQ5	DQ6	V_{SSQ}
V_{SSQ}	UDQS	DQ8	E	DQ7	LDQS	V_{DDQ}
V_{SS}	UDM	NC	F	NC	LDM	V_{DD}
CKE	CK	$\overline{CK}$	G	$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
A9	A11	A12	H	$\overline{CS}$	BA0	BA1
A6	A7	A8	J	A10/AP	A0	A1
V_{SS}	A4	A5	K	A2	A3	V_{DD}

Figure 1 Standard Ballout 512-Mbit DDR Mobile-RAM (Top View)

1.3 Description

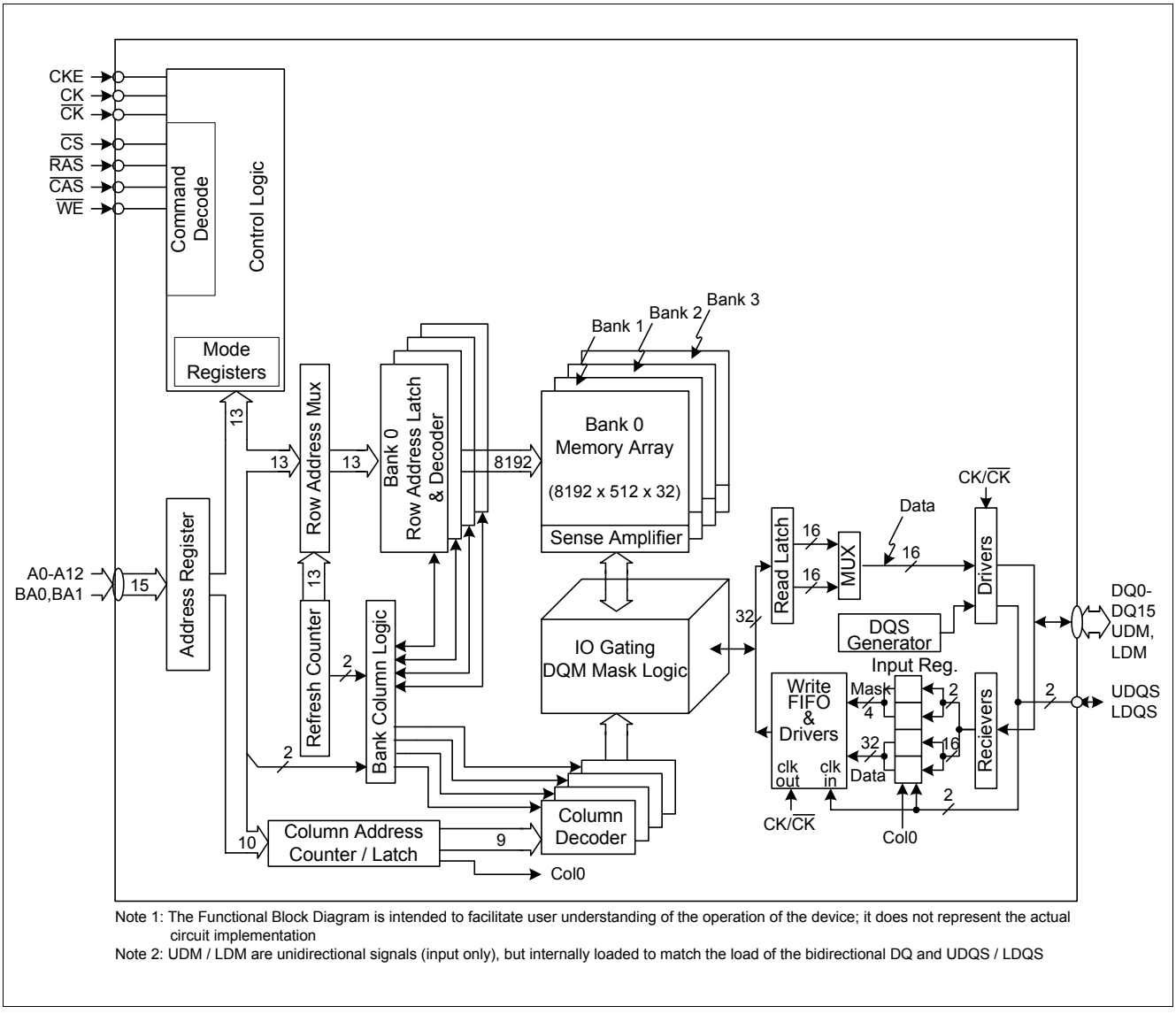
The HYB18M512160BFX is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

The HYB18M512160BFX uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a *2n* prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE access for the DDR Mobile-RAM consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

The HYB18M512160BFX is especially designed for mobile applications. It operates from a 1.8V power supply. Power consumption in self refresh mode is drastically reduced by an On-Chip Temperature Sensor (OCTS); it can further be reduced by using the programmable Partial Array Self Refresh (PASR).

A conventional data-retaining Power-Down (PD) mode is available as well as a non-data-retaining Deep Power-Down (DPD) mode. For further power-savings the clock may be stopped during idle periods.

The HYB18M512160BFX is housed in a 60-ball P-VFBGA package. It is available in Commercial (0°C to 70°C) temperature range.



Note 1: The Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent the actual circuit implementation
Note 2: UDM / LDM are unidirectional signals (input only), but internally loaded to match the load of the bidirectional DQ and UDQS / LDQS

Figure 2 Functional Block Diagram

1.4 Pin Definition and Description

Table 4 Pin Description

Ball	Type	Detailed Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control inputs are sampled on crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides precharge power-down and self refresh operation (all banks idle), or active power-down (row active in any bank). CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DQ0 - DQ15	I/O	**Data Inputs/Output:** Bi-directional data bus (16 bit)
LDQS, UDQS	I/O	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. LDQS corresponds to the data on DQ0 - DQ7; UDQS to the data on DQ8 - DQ15.
LDM, UDM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. DM may be driven HIGH, LOW, or floating during READs. LDM corresponds to the data on DQ0 - DQ7; UDM to the data on DQ8 - DQ15.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an ACTIVATE, READ, WRITE or PRECHARGE command is being applied. BA0, BA1 also determine which mode register is to be loaded during a MODE REGISTER SET command (MRS or EMRS).
A0 - A12	Input	**Address Inputs:** Provide the row address for ACTIVE commands and the column address and Auto Precharge bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 (=AP) is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10=LOW) or all banks (A10=HIGH). If only one bank is to be precharged, the bank is selected by BA0 and BA1. The address inputs also provide the op-code during a MODE REGISTER SET command.
V_{DDQ}	Supply	**I/O Power Supply:** Isolated power for DQ output buffers for improved noise immunity: V_{DDQ} = 1.70 V – 1.90 V
V_{SSQ}	Supply	**I/O Ground**
V_{DD}	Supply	**Power Supply:** Power for the core logic and input buffers, V_{DD} = 1.70 V – 1.90 V
V_{SS}	Supply	**Ground**
N.C.	–	**No Connect**

2 Functional Description

The 512-Mbit DDR Mobile-RAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

READ and WRITE accesses to the DDR Mobile-RAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the banks, A0 - A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR Mobile-RAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

2.1 Power On and Initialization

The DDR Mobile-RAM must be powered up and initialized in a predefined manner (see **Figure 3**). Operational procedures other than those specified may result in undefined operation.

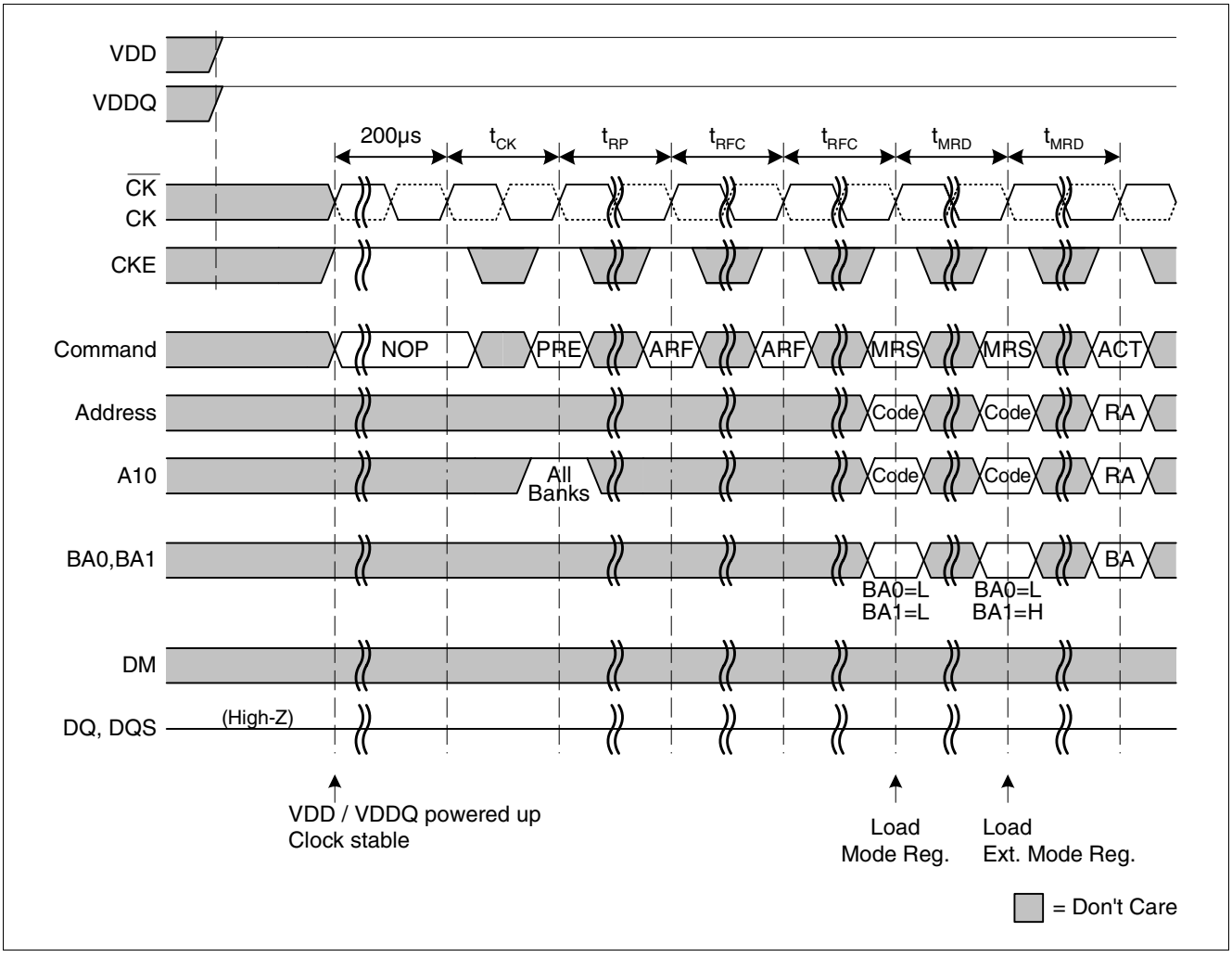


Figure 3 Power-Up Sequence and Mode Register Sets

1. At first, device core power (V_{DD}) and device IO power (V_{DDQ}) must be brought up simultaneously. Typically V_{DD} and V_{DDQ} are driven from a single power converter output.
   Assert and hold CKE to a HIGH level.
2. After V_{DD} and V_{DDQ} are stable and CKE is HIGH, apply stable clocks.
3. Wait for 200µs while issuing NOP or DESELECT commands.
4. Issue a PRECHARGE ALL command, followed by NOP or DESELECT commands for at least t_{RP} period.
5. Issue two AUTO REFRESH commands, each followed by NOP or DESELECT commands for at least t_{RFC} period.
6. Issue two MODE REGISTER SET commands for programming the Mode Register and Extended Mode Register, each followed by NOP or DESELECT commands for at least t_{MRD} period; the order in which both registers are programmed is not important.

Following these steps, the DDR Mobile-RAM is ready for normal operation.

2.2 Register Definition

2.2.1 Mode Register

The Mode Register is used to define the specific mode of operation of the DDR Mobile-RAM. This definition includes the selection of a burst length (bits A0-A2), a burst type (bit A3) and a CAS latency (bits A4-A6). The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

MR
Mode Register Definition **(BA[1:0] = 00_B)**

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**		**CL**		**BT**		**BL**	

Field	Bits	Type	Description
CL	[6:4]	w	**CAS Latency** 010 2 011 3 *Note: All other bit combinations are RESERVED.*
BT	3	w	**Burst Type** 0 Sequential 1 Interleaved
BL	[2:0]	w	**Burst Length** 001 2 010 4 011 8 100 16 *Note: All other bit combinations are RESERVED.*

2.2.1.1 Burst Length

READ and WRITE accesses to the DDR Mobile-RAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, 8 or 16 locations are available.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1 - A9 when the burst length is set to two, by A2 - A9 when the burst length is set to four, by A3 - A9 when the burst length is set to eight and by A4 - A9 when the burst length is set to sixteen. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

2.2.1.2 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in **Table 5**.

2.2.1.3 Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be programmed to 2 or 3 clocks.

If a READ command is registered and the latency is 3 clocks, the first data element will be valid after ($2 * t_{CK} + t_{AC}$). If a READ command is registered and the latency is 2 clocks, the first data element will be valid after ($t_{CK} + t_{AC}$). For details please refer to the READ command description.

Table 5 Burst Definition

Burst Length	Starting Column Address				Order of Accesses Within a Burst (Hexadecimal Notation)	
	A3	A2	A1	A0	Sequential	Interleaved
2				0	0 - 1	0 - 1
				1	1 - 0	1 - 0
4			0	0	0 - 1 - 2 - 3	0 - 1 - 2 - 3
			0	1	1 - 2 - 3 - 0	1 - 0 - 3 - 2
			1	0	2 - 3 - 0 - 1	2 - 3 - 0 - 1
			1	1	3 - 0 - 1 - 2	3 - 2 - 1 - 0
8		0	0	0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
		0	0	1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0	1 - 0 - 3 - 2 - 5 - 4 - 7 - 6
		0	1	0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1	2 - 3 - 0 - 1 - 6 - 7 - 4 - 5
		0	1	1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2	3 - 2 - 1 - 0 - 7 - 6 - 5 - 4
		1	0	0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
		1	0	1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4	5 - 4 - 7 - 6 - 1 - 0 - 3 - 2
		1	1	0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5	6 - 7 - 4 - 5 - 2 - 3 - 0 - 1
		1	1	1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6	7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
16	0	0	0	0	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F
	0	0	0	1	1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0	1-0-3-2-5-4-7-6-9-8-B-A-D-C-F-E
	0	0	1	0	2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1	2-3-0-1-6-7-4-5-A-B-8-9-E-F-C-D
	0	0	1	1	3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2	3-2-1-0-7-6-5-4-B-A-9-8-F-E-D-C
	0	1	0	0	4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3	4-5-6-7-0-1-2-3-C-D-E-F-8-9-A-B
	0	1	0	1	5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4	5-4-7-6-1-0-3-2-D-C-F-E-9-8-B-A
	0	1	1	0	6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5	6-7-4-5-2-3-0-1-E-F-C-D-A-B-8-9
	0	1	1	1	7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-F-E-D-C-B-A-9-8
	1	0	0	0	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7
	1	0	0	1	9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8	9-8-B-A-D-C-F-E-1-0-3-2-5-4-7-6
	1	0	1	0	A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9	A-B-8-9-E-F-C-D-2-3-0-1-6-7-4-5
	1	0	1	1	B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A	B-A-9-8-F-E-D-C-3-2-1-0-7-6-5-4
	1	1	0	0	C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B	C-D-E-F-8-9-A-B-4-5-6-7-0-1-2-3
	1	1	0	1	D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C	D-C-F-E-9-8-B-A-5-4-7-6-1-0-3-2
	1	1	1	0	E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D	E-F-C-D-A-B-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E	F-E-D-C-B-A-9-8-7-6-5-4-3-2-1-0

Notes

1. *For a burst length of 2, A1-Ai select the two-data-element block; A0 selects the first access within the block.*
2. *For a burst length of 4, A2-Ai select the four-data-element block; A0-A1 select the first access within the block.*
3. *For a burst length of 8, A3-Ai select the eight-data-element block; A0-A2 select the first access within the block.*
4. *For a burst length of 16, A4-Ai select the sixteen-data-element block; A0-A3 select the first access within the block.*
5. *Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block.*

2.2.2 Extended Mode Register

The Extended Mode Register controls additional low power features of the device. These include the Partial Array Self Refresh (PASR), the Temperature Compensated Self Refresh (TCSR) and the drive strength selection for the DQs. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 1) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements result in unspecified operation. Address bits A0 - A2 specify the Partial Array Self Refresh (PASR) and bits A5 - A6 the Drive Strength, while bits A7 - A12 shall be written to zero. Bits A3 and A4 are “don’t care” (see below).

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

EMR
Extended Mode Register **(BA[1:0] = 10_B)**

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**DS**		**(TCSR)**		**PASR**		

Field	Bits	Type	Description
DS	[6:5]	w	**Selectable Drive Strength** 00 Full Drive Strength 01 Half Drive Strength 10 Quarter Drive Strength *Note: All other bit combinations are RESERVED.*
TCSR	[4:3]	w	**Temperature Compensated Self Refresh** XX Superseded by on-chip temperature sensor (see text)
PASR	[2:0]	w	**Partial Array Self Refresh** 000 all banks 001 half array (BA1 = 0) 010 quarter array (BA1 = BA0 = 0) 101 1/8 array (BA1 = BA0 = RA12 = 0) 110 1/16 array (BA1 = BA0 = RA12 = RA11 = 0) *Note: All other bit combinations are RESERVED.*

2.2.2.1 Partial Array Self Refresh (PASR)

Partial Array Self Refresh is a power-saving feature specific to DDR Mobile-RAMs. With PASR, self refresh may be restricted to variable portions of the total array. The selection comprises all four banks (default), two banks, one bank, half of one bank, and a quarter of one bank. Data written to the non activated memory sections will get lost after a period defined by t_{REF} (cf. **Table 14**).

2.2.2.2 Temperature Compensated Self Refresh (TCSR) with On-Chip Temperature Sensor

DRAM devices store data as electrical charge in tiny capacitors that require a periodic refresh in order to retain the stored information. This refresh requirement heavily depends on the die temperature: high temperatures correspond to short refresh periods, and low temperatures correspond to long refresh periods.

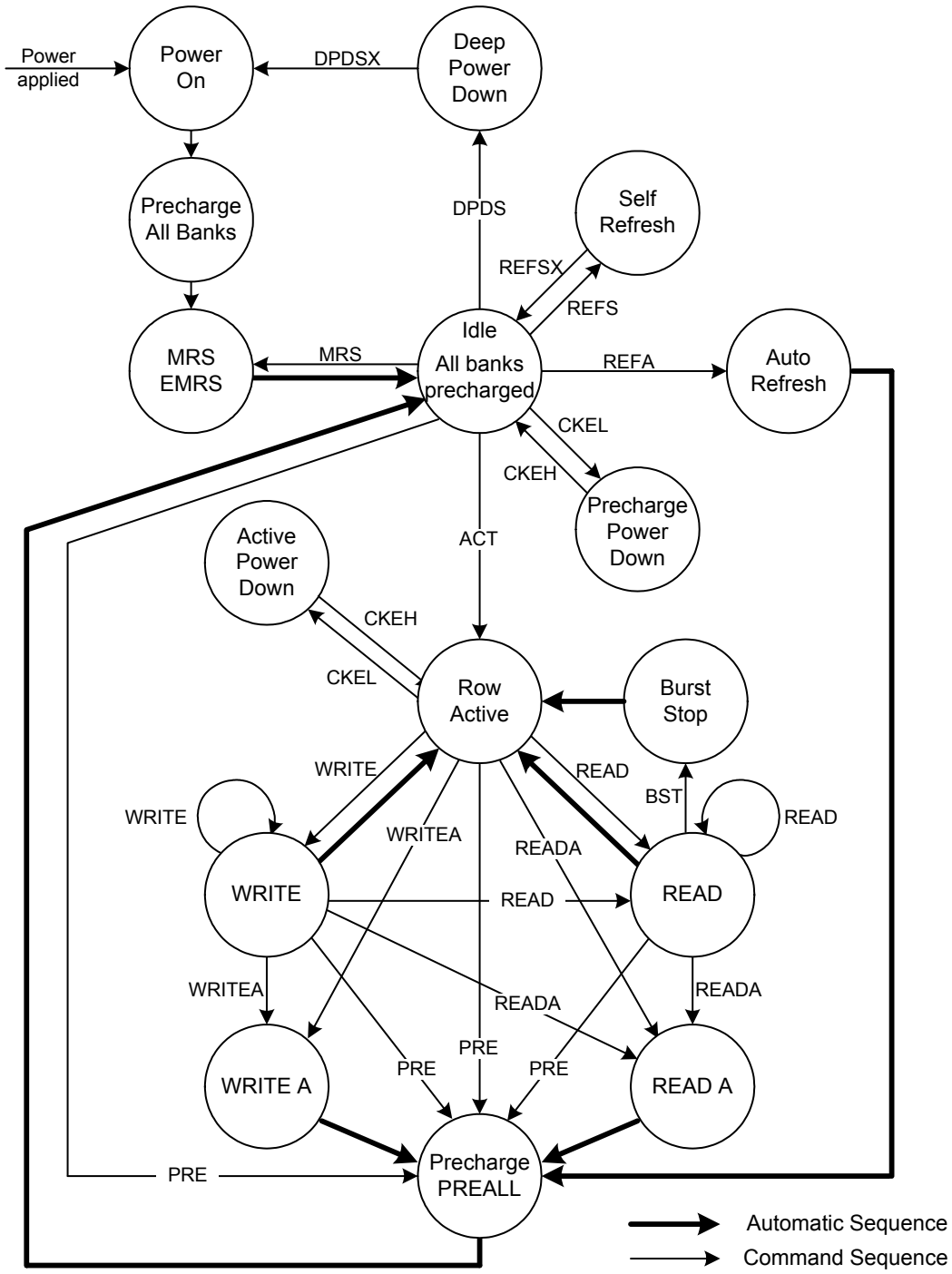
The DDR Mobile-RAM is equipped with an on-chip temperature sensor which continuously senses the actual die temperature and adjusts the refresh period in Self Refresh mode accordingly. This makes any programming of the TCSR bits in the Extended Mode Register obsolete. It also is the superior solution in terms of compatibility and power-saving, because

- it is fully compatible to all processors that do not support the Extended Mode Register
- it is fully compatible to all applications that only write a default (worst case) TCSR value, e.g. because of the lack of an external temperature sensor
- it does not require any processor interaction for regular TCSR updates

2.2.2.3 Selectable Drive Strength

The drive strength of the DQ output buffers is selectable via bits A5 and A6. The “full drive strength” (default) is suitable for heavier loaded systems. The “half drive strength” is intended for lightly loaded systems or systems with reduced performance requirements. Finally, for systems with point-to-point connection, a “quarter drive strength” is available. I-V curves for full and half drive strengths are included in this document.

2.3 State Diagram



ACT = Active
BST = Burst Terminate
CKEL = Enter Power-Down
CKEH = Exit Power-Down
DPDS = Enter Deep Power-Down
DPDSX = Exit Deep Power-Down
EMRS = Ext. Mode Reg. Set
MRS = Mode Register Set
PRE = Precharge
PREALL = Precharge All Banks
REFA = Auto Refresh
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
READ = Read w/o Auto Precharge
READA = Read with Auto Precharge
WRITE = Write w/o Auto Precharge
WRITEA = Write with Auto Precharge

Note: Use caution with this diagram. It is indented to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular situations involving more than one bank are not captured in full detail.

Figure 4 State Diagram

2.4 Commands

Table 6 Command Overview

Command		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Notes
NOP	DESELECT	H	X	X	X	X	1)2)
	NO OPERATION	L	H	H	H	X	1)2)
ACT	ACTIVE (Select bank and row)	L	L	H	H	Bank / Row	1)3)
RD	READ (Select bank and column and start read burst)	L	H	L	H	Bank / Col	1)4)
WR	WRITE (Select bank and column and start write burst)	L	H	L	L	Bank / Col	1)4)
BST	BURST TERMINATE or DEEP POWER-DOWN	L	H	H	L	X	1)5)
PRE	PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	1)6)
ARF	AUTO REFRESH or SELF REFRESH entry	L	L	L	H	X	1)7)8)
MRS	MODE REGISTER SET	L	L	L	L	Op-Code	1)9)

1) CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER DOWN.
2) DESELECT and NOP are functionally interchangeable.
3) BA0, BA1 provide the bank address, and A0 - A12 provide the row address.
4) BA0, BA1 provide the bank address, A0 - A9 provide the column address; A10 HIGH enables the Auto Precharge feature (nonpersistent), A10 LOW disables the Auto Precharge feature.
5) This command is BURST TERMINATE if CKE is HIGH, DEEP POWER-DOWN if CKE is LOW. The BURST TERMINATE command is defined for READ bursts with Auto Precharge disabled only; it is undefined (and should not be used) for read bursts with Auto Precharge enabled, and for write bursts.
6) A10 LOW: BA0, BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0, BA1 are “Don’t Care”.
7) This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
8) Internal refresh counter controls row and bank addressing; all inputs and I/Os are “Don’t Care” except for CKE.
9) BA0, BA1 select either the Mode Register (BA0 = 0, BA1 = 0) or the Extended Mode Register (BA0 = 0, BA1 = 1); other combinations of BA0, BA1 are reserved; A0 - A12 provide the op-code to be written to the selected mode register.

Table 7 DM Operation

Name (Function)	DM	DQs	Notes
Write Enable	L	Valid	1)
Write Inhibit	H	X	1)

1) Used to mask write data provided coincident with the corresponding data

Address (BA0, BA1, A0 - A12) and command inputs (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) are all registered on the crossing of the positive edge of CK and the negative edge of $\overline{CK}$. **Figure 5** shows the basic timing parameters, which apply to all commands and operations.

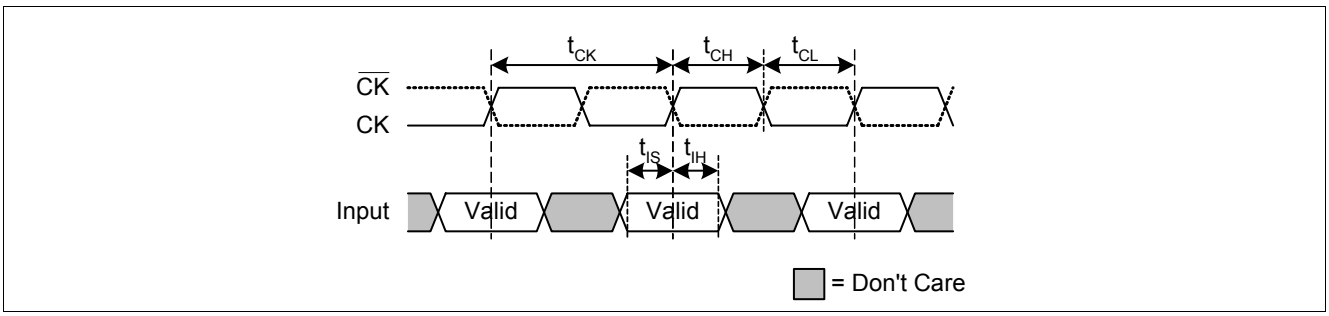


Figure 5 Address / Command Inputs Timing Parameters

Table 8 Inputs Timing Parameters[1)]

Parameter		Symbol	- 7.5		Unit	Notes
			Min.	Max.		
Clock high-level width		t_{CH}	0.45	0.55	t_{CK}	–
Clock low-level width		t_{CL}	0.45	0.55	t_{CK}	–
Clock cycle time	CL = 3	t_{CK}	7.5	–	ns	2)
	CL = 2		15	–		
Address and control input setup time	fast slew rate	t_{IS}	1.3	–	ns	3)4)5)
	slow slew rate		1.5	–		3)6)
Address and control input hold time	fast slew rate	t_{IH}	1.3	–	ns	3)4)
	slow slew rate		1.5	–		3)6)
Address and control input pulse width		t_{IPW}	3.0	–	ns	7)

1) All AC timing characteristics assume an input slew rate of 1.0 V/ns.
2) The only time that the clock frequency is allowed to change is during power-down, self-refresh or clock stop modes.
3) The transition time for address and command inputs is measured between V_{IH} and V_{IL}.
4) For command / address input slew rate ≥ 1V/ns.
5) A CK/$\overline{CK}$ differential slew rate of 2.0 V/ns is assumed for this parameter.
6) For command / address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns.
7) This parameter guarantees device timing. It is verified by device characterization but are not subject to production test.

2.4.1 NO OPERATION (NOP)

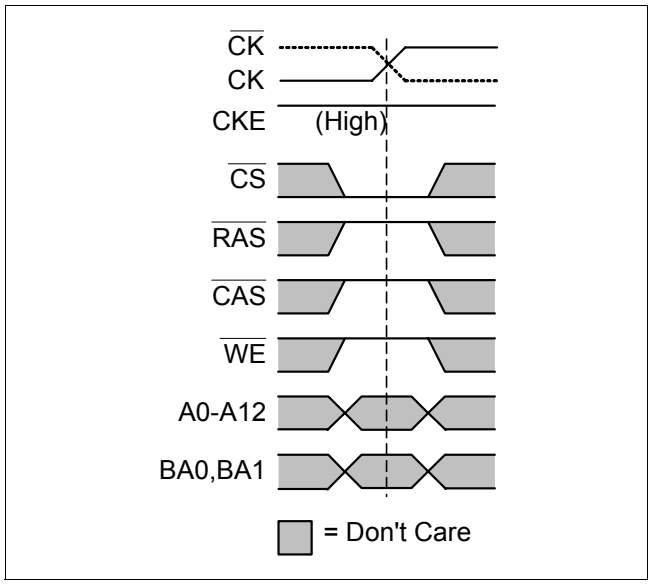


Figure 6 No Operation Command

The NO OPERATION (NOP) command is used to perform a NOP to a DDR Mobile-RAM which is selected ($\overline{CS}$ = LOW). This prevents unwanted commands from being registered during idle states. Operations already in progress are not affected.

2.4.2 DESELECT

The DESELECT function ($\overline{CS}$ = HIGH) prevents new commands from being executed by the DDR Mobile-RAM. The DDR Mobile-RAM is effectively deselected. Operations already in progress are not affected.

2.4.3 MODE REGISTER SET

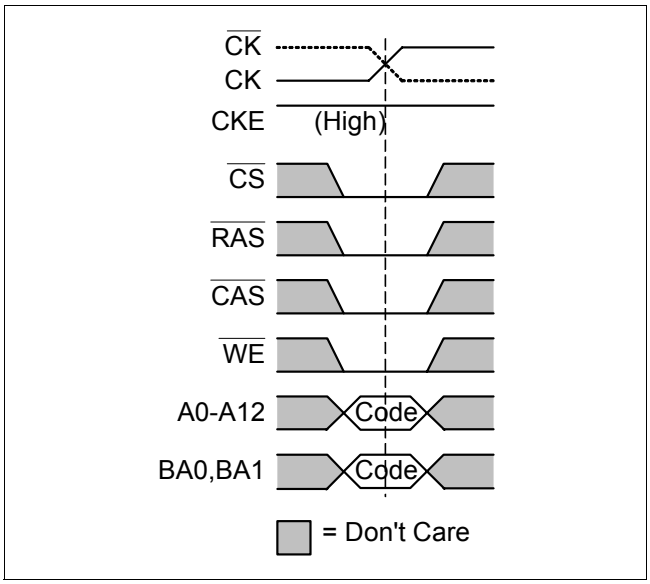


Figure 7 Mode Register Set Command

The Mode Register and Extended Mode Register are loaded via inputs A0 - A12 (see mode register descriptions in **Chapter 2.2**). The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.

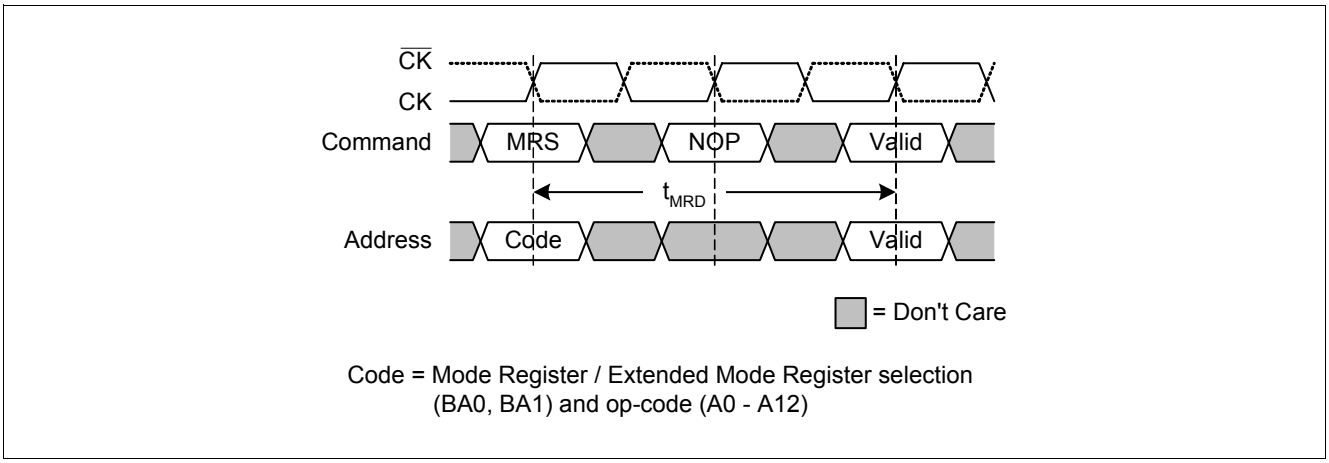


Figure 8 Mode Register Definition

Table 9 Timing Parameters for Mode Register Set Command

Parameter	Symbol	- 7.5		Unit	Notes
		Min.	Max.		
MODE REGISTER SET command period	t_{MRD}	2	–	t_{CK}	–

2.4.4 ACTIVE

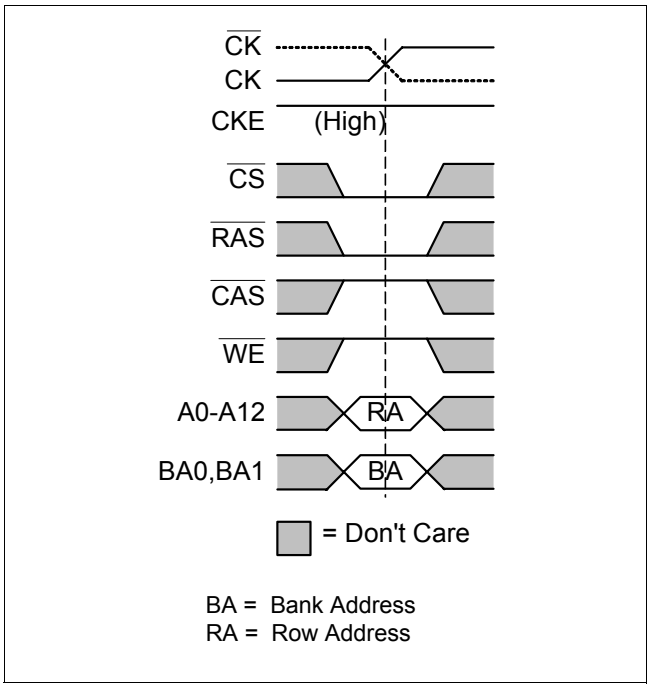


Figure 9 ACTIVE Command

Before any READ or WRITE commands can be issued to a bank within the DDR Mobile-RAM, a row in that bank must be "opened" (activated). This is accomplished via the ACTIVE command and addresses BA0, BA1, A0 - A12 (see **Figure 9**), which decode and select both the bank and the row to be activated. After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the t_{RCD} specification. A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged).

The minimum time interval between successive ACTIVE commands to the same bank is defined by t_{RC}. A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by t_{RRD}.

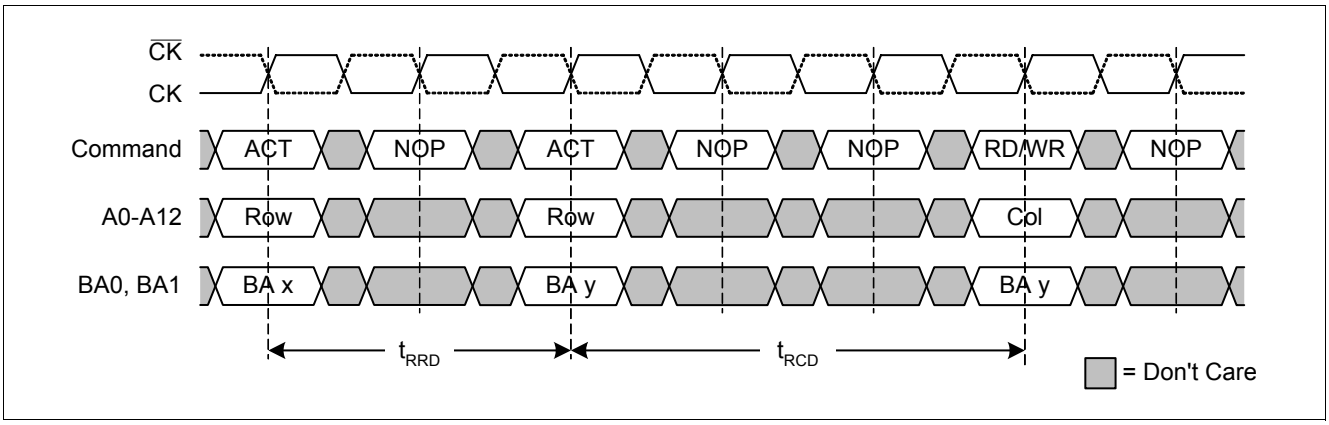


Figure 10 Bank Activate Timings

Table 10 Timing Parameters for ACTIVE Command

Parameter	Symbol	- 7.5		Unit	Notes
		Min.	Max.		
ACTIVE to ACTIVE command period	t_{RC}	65	–	ns	1)
ACTIVE to READ or WRITE delay	t_{RCD}	22.5	–	ns	1)
ACTIVE bank A to ACTIVE bank B delay	t_{RRD}	15	–	ns	1)

1) These parameters account for the number of clock cycles and depend on the operating frequency, as follows:
no. of clock cycles = specified delay / clock period ; round to the next higher integer.

2.4.5 READ

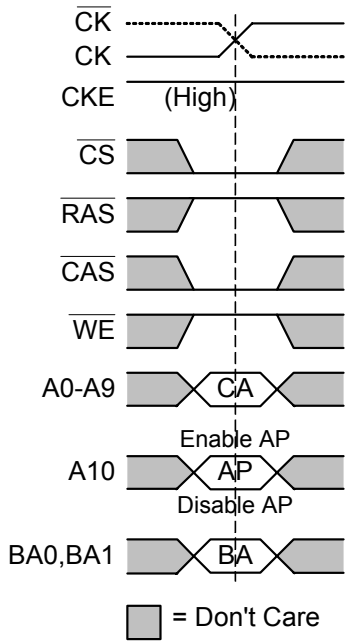
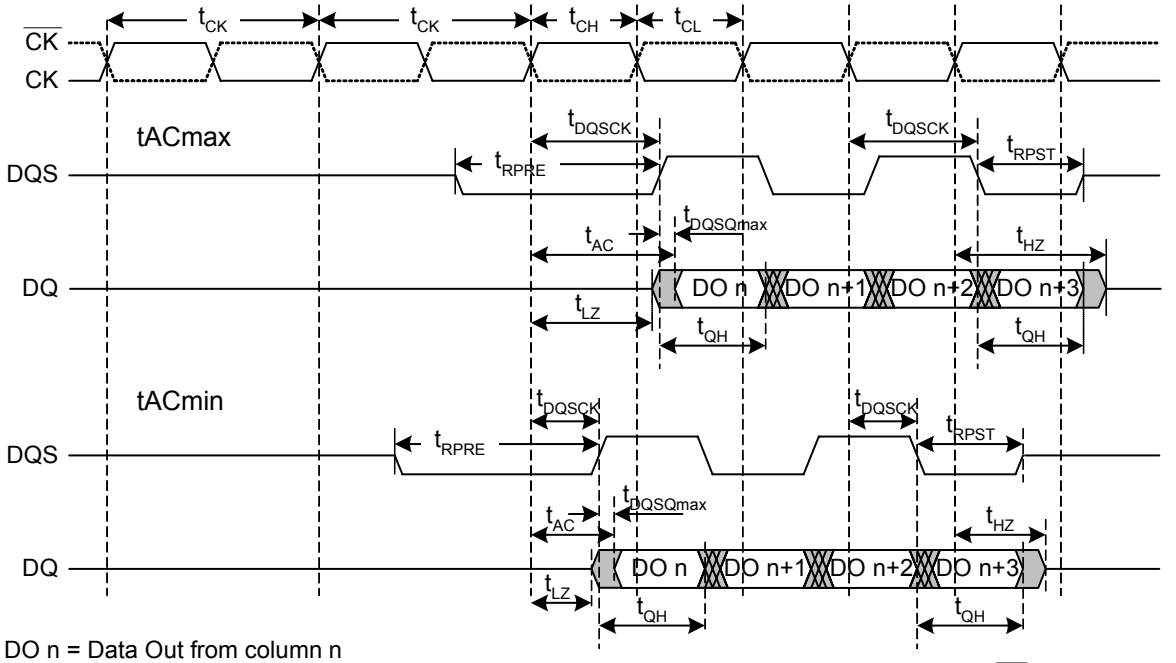


Figure 11 READ Command

READ bursts are initiated with a READ command, as shown in **Figure 11**.

Basic timings for the DQs are shown in **Figure 12**; they apply to all read operations.

The starting column and bank addresses are provided with the READ command and Auto Precharge is either enabled or disabled for that burst access. If Auto Precharge is enabled, the row that is accessed will start precharge at the completion of the burst, provided t_{RAS} has been satisfied. For the generic READ commands used in the following illustrations, Auto Precharge is disabled.



DO n = Data Out from column n
Burst Length = 4 in the case shown
CAS Latency = 3 in the case shown
All DQ are valid tAC after the CK edge. All DQ are valid tDQSQ after the DQS edge, regardless of tAC

Figure 12 Basic READ Timing Parameters for DQs

Table 11 Timing Parameters for READ Command

Parameter		Symbol	- 7.5		Unit	Notes
			Min.	Max.		
DQ output access time from CK/$\overline{CK}$		t_{AC}	2.0	6.5	ns	1)2)
DQS output access time from CK/$\overline{CK}$		t_{DQSCK}	2.0	6.5	ns	1)2)
DQ & DQS low-impedance time from CK/$\overline{CK}$		t_{LZ}	1.0	–	ns	3)
DQ & DQS high-impedance time from CK/$\overline{CK}$		t_{HZ}	–	6.5	ns	3)
DQS - DQ skew		t_{DQSQ}	–	0.6	ns	4)
DQ / DQS output hold time from DQS		t_{QH}	t_{HP}-t_{QHS}	–	ns	5)
Data hold skew factor		t_{QHS}	–	0.75	ns	5)
Read preamble	CL = 3	t_{RPRE}	0.9	1.1	t_{CK}	–
	CL = 2		0.7	1.1		
Read postamble		t_{RPST}	0.4	0.6	t_{CK}	–
ACTIVE to PRECHARGE command period		t_{RAS}	45	70,000	ns	6)
ACTIVE to ACTIVE command period		t_{RC}	65	–	ns	6)
ACTIVE to READ or WRITE delay		t_{RCD}	22.5	–	ns	6)
PRECHARGE command period		t_{RP}	22.5	–	ns	6)

1) The output timing reference level is $V_{DDQ}/2$.

2) Parameters t_{AC} and t_{QH} are specified for full drive strength and a reference load of 20pF. This reference load is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. For half drive strength with a nominal load of 10pF parameters t_{AC} and t_{QH} are expected to be in the same range. However, these parameters are not subject to production test but are estimated by device characterization. Use of IBIS or other simulation tools for system validation is suggested.

3) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

4) t_{DQSQ} consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

5) $t_{QH} = t_{HP} - t_{QHS}$, where t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL}, t_{CH}). t_{QHS} accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

6) These parameters account for the number of clock cycles and depend on the operating frequency, as follows:
no. of clock cycles = specified delay / clock period ; round to the next higher integer.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command.

The diagrams in **Figure 13** show general timing for each supported CAS latency setting. DQS is driven by the DDR Mobile-RAM along with output data. The initial low state on DQS is known as the read preamble; the low state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other READ commands have been initiated, the DQs will go High-Z.

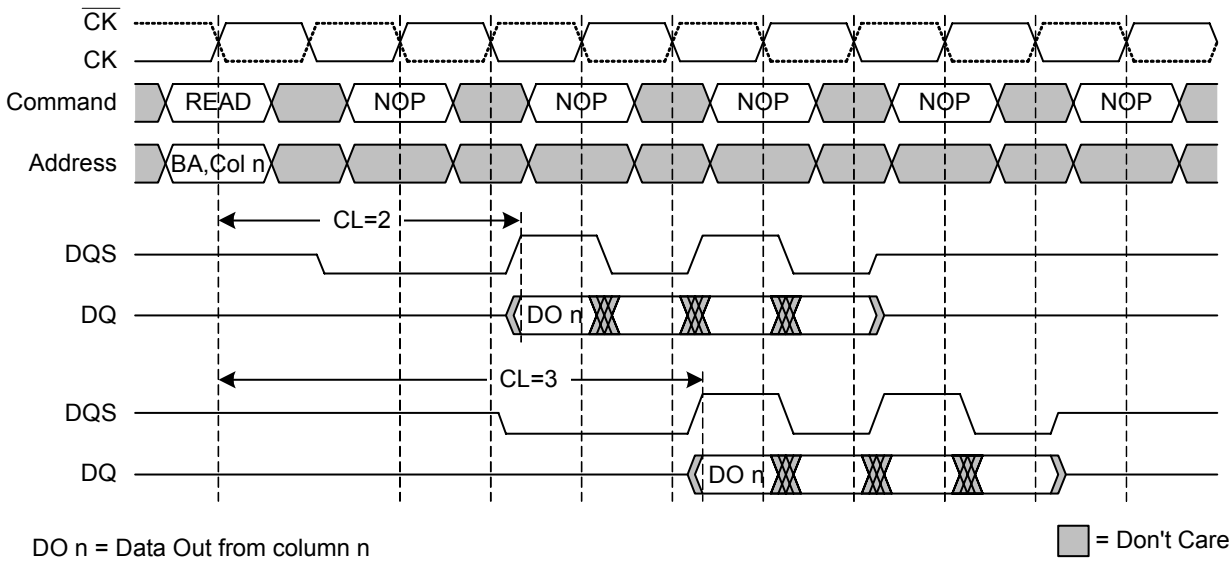


Figure 13 READ Burst

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated.

The new READ command should be issued x cycles after the first READ command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in **Figure 14**.

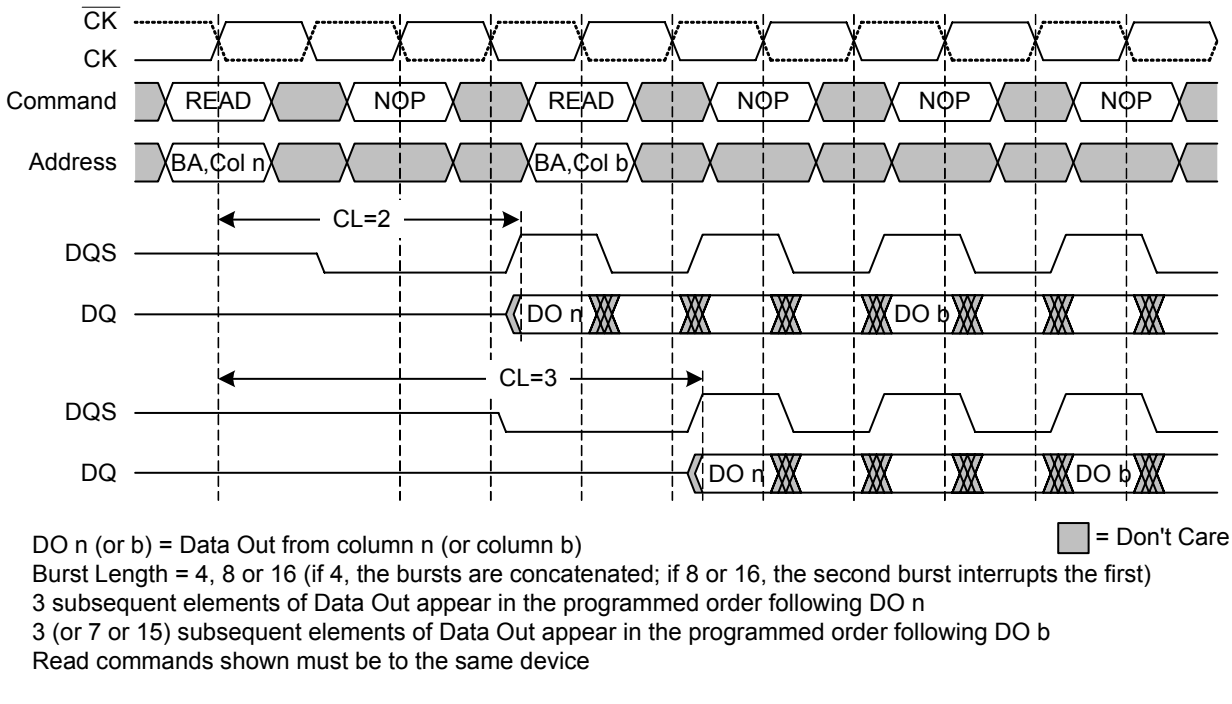


Figure 14 Consecutive READ Bursts

A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive READ data is illustrated in **Figure 15**.

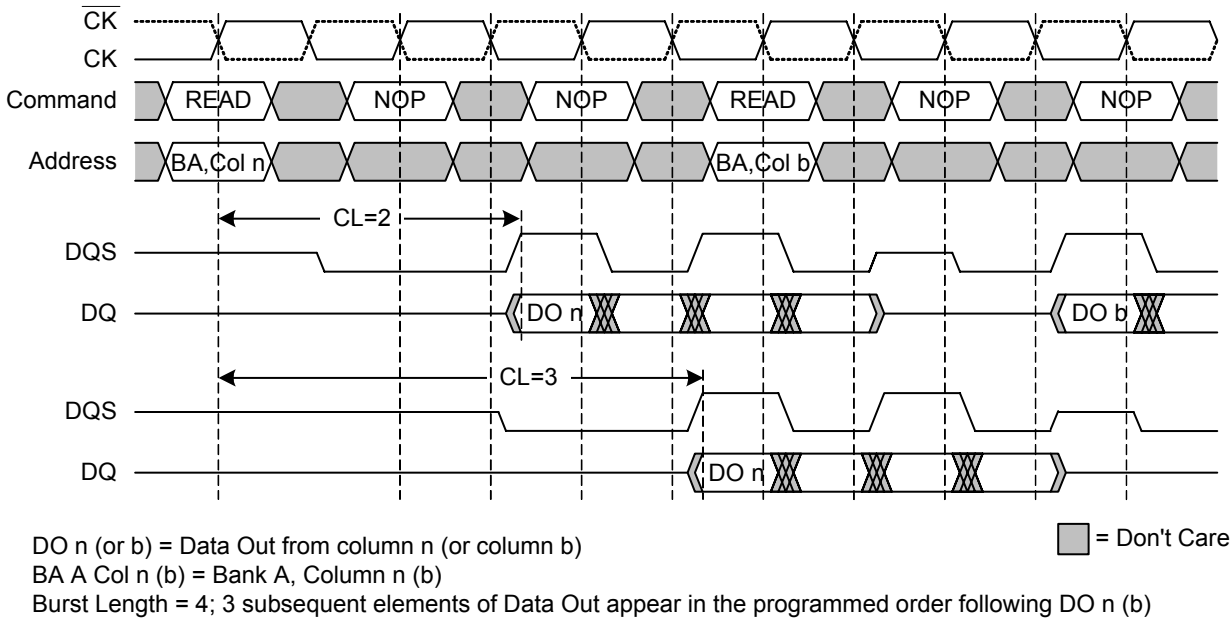


Figure 15 Nonconsecutive READ Bursts

Full-speed random READ accesses (Burst Length = 2, 4, 8 or 16) within a page (or pages) can be performed as shown in **Figure 16**.

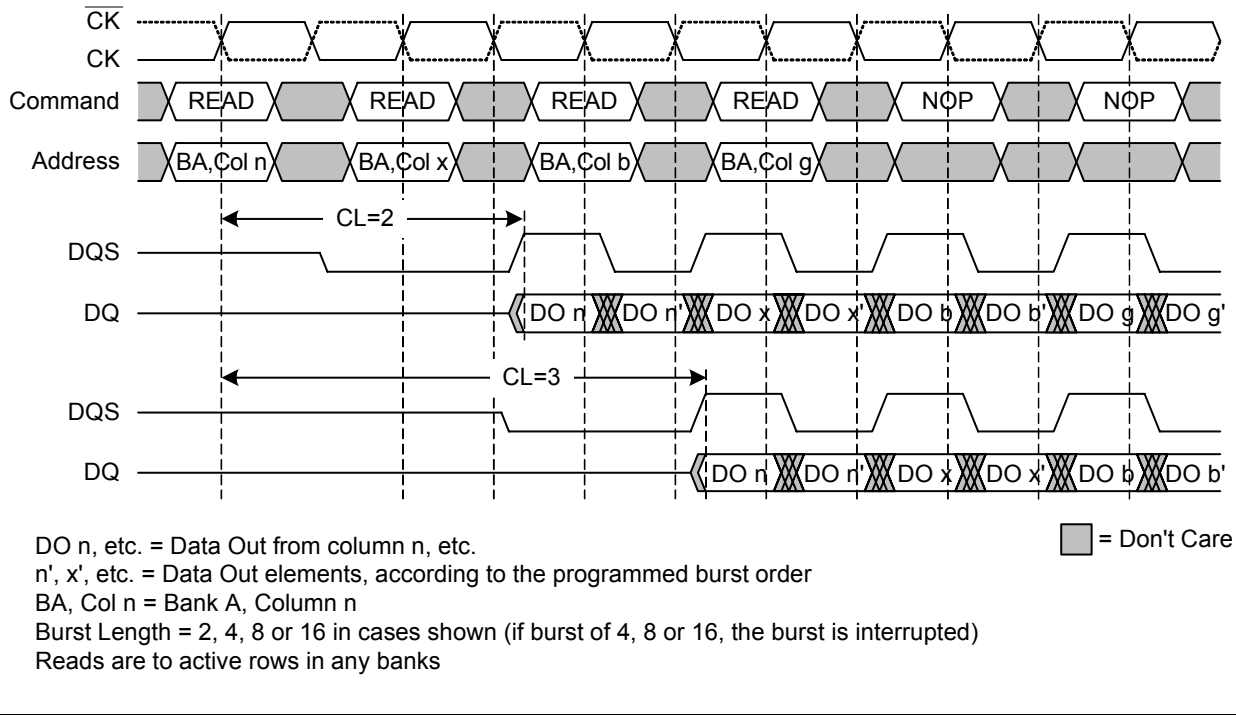
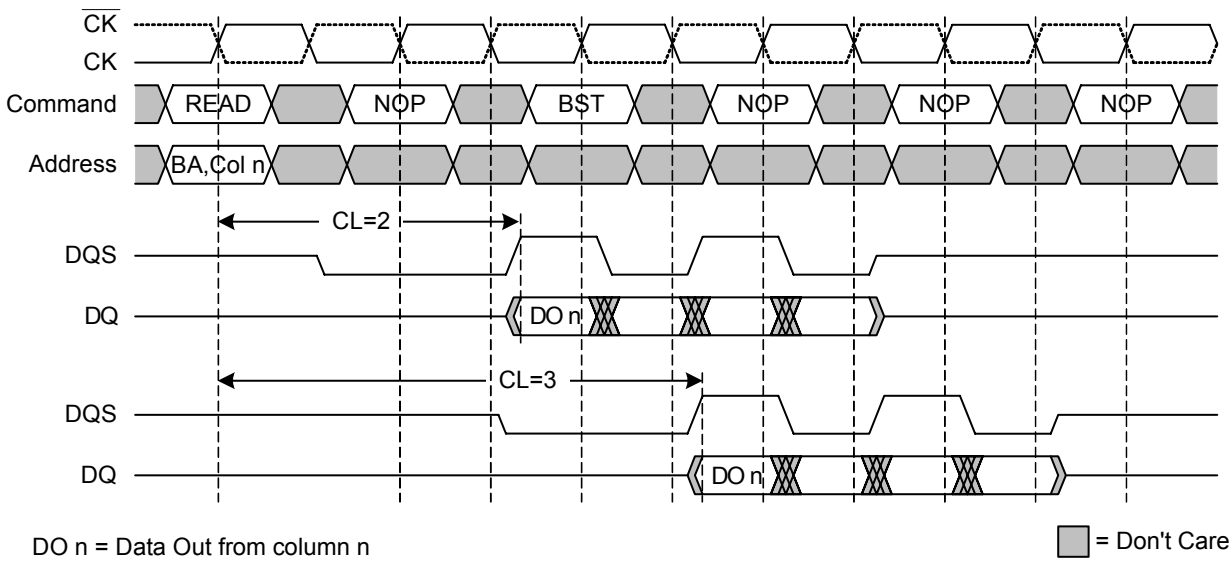


Figure 16 Random READ Accesses

2.4.5.1 READ Burst Termination

Data from any READ burst may be truncated using the BURST TERMINATE command (see **Figure 20**), provided that Auto Precharge was not activated. The BURST TERMINATE latency is equal to the CAS latency, i.e. the BURST TERMINATE command should be issued x clock cycles after the READ command, where x equals the number of desired data element pairs. This is shown in **Figure 17**.



DO n = Data Out from column n
BA, Col n = Bank A, Column n
Cases shown are bursts of 8 terminated after 4 data elements.
3 subsequent elements of Data Out appear in the programmed order following DO n

Figure 17 Terminating a READ Burst

2.4.5.2 READ to WRITE

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in **Figure 18**.

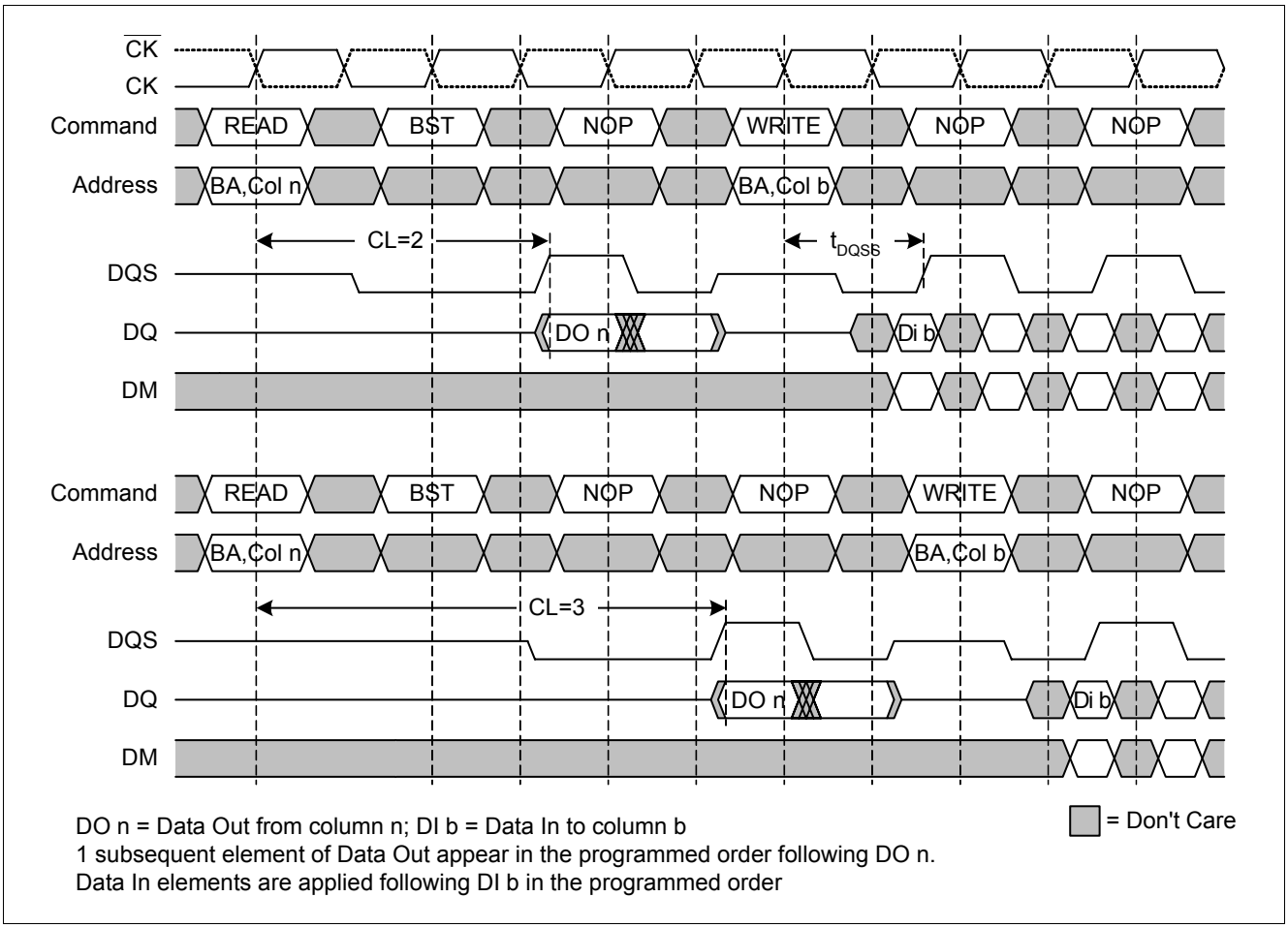


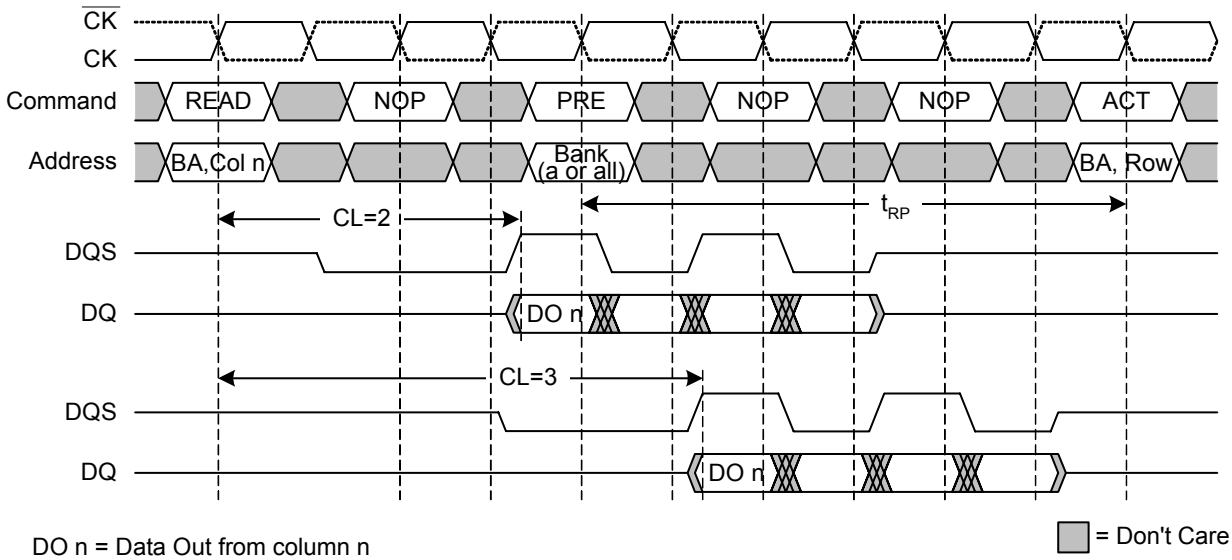
Figure 18 READ to WRITE

2.4.5.3 READ to PRECHARGE

A READ burst may be followed by, or truncated with a PRECHARGE command to the same bank (provided that Auto Precharge was not activated).

The PRECHARGE command should be issued x clock cycles after the READ command, where x equals the number of desired data element pairs. This is shown in **Figure 19**. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met. Please note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a READ being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same READ burst with Auto Precharge enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.



DO n = Data Out from column n
Cases shown are either uninterrupted burst of 4, or interrupted bursts of 8 or 16
3 subsequent elements of Data Out appear in the programmed order following DO n
Precharge may be applied at (BL / 2) tCK after the READ command.
Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
The ACTIVE command may be applied if tRC has been met.

Figure 19 READ to PRECHARGE

2.4.6 BURST TERMINATE

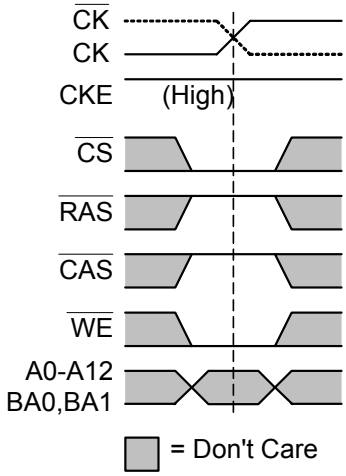


Figure 20 BURST TERMINATE Command

The BURST TERMINATE command is used to truncate READ bursts (with Auto Precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in **Figure 17**.

2.4.7 WRITE

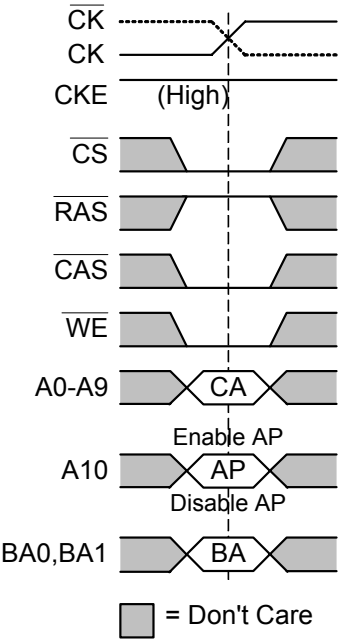


Figure 21 WRITE Command

WRITE bursts are initiated with a WRITE command, as shown in **Figure 21**. Basic timings for the DQs are shown in **Figure 22**; they apply to all write operations.

The starting column and bank addresses are provided with the WRITE command, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged at the completion of the write burst. For the generic WRITE commands used in the following illustrations, Auto Precharge is disabled.

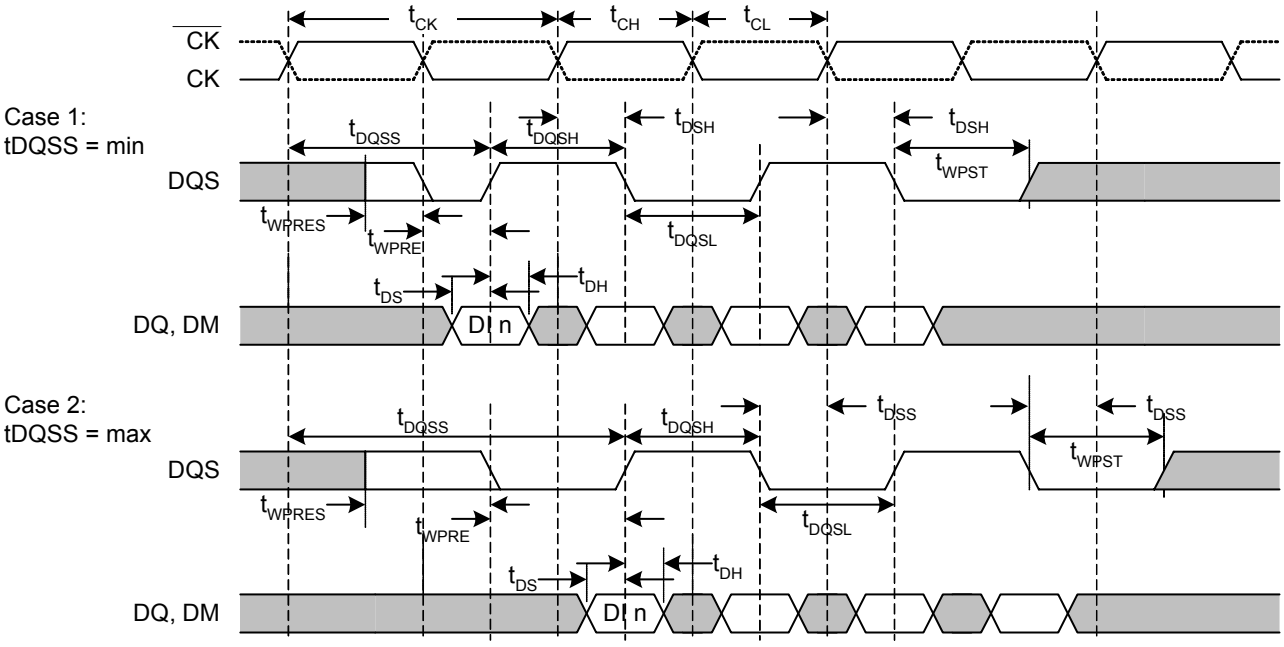


Figure 22 Basic WRITE Timing Parameters for DQs

Table 12 Timing Parameters for WRITE Command

Parameter		Symbol	- 7.5		Unit	Notes
			Min.	Max.		
DQ and DM input setup time	fast slew rate	t_{DS}	0.75	–	ns	1)2)3)
	slow slew rate		0.85	–		1)2)4)
DQ and DM input hold time	fast slew rate	t_{DH}	0.75	–	ns	1)2)3)
	slow slew rate		0.85	–		1)2)4)
DQ and DM input pulse width		t_{DIPW}	1.7	–	ns	5)
Write command to 1st DQS latching transition		t_{DQSS}	0.75	1.25	t_{CK}	–
DQS input high-level width		t_{DQSH}	0.4	0.6	t_{CK}	–
DQS input low-level width		t_{DQSL}	0.4	0.6	t_{CK}	–
DQS falling edge to CK setup time		t_{DSS}	0.2	–	t_{CK}	–
DQS falling edge hold time from CK		t_{DSH}	0.2	–	t_{CK}	–
Write preamble setup time		t_{WPRES}	0	–	ns	6)
Write postamble		t_{WPST}	0.4	0.6	t_{CK}	7)
Write preamble		t_{WPRE}	0.25	–	t_{CK}	–
ACTIVE to PRECHARGE command period		t_{RAS}	45	70,000	ns	8)
ACTIVE to ACTIVE command period		t_{RC}	65	–	ns	8)
ACTIVE to READ or WRITE delay		t_{RCD}	22.5	–	ns	8)
WRITE recovery time		t_{WR}	15	–	ns	8)
Internal write to Read command delay		t_{WTR}	1	–	t_{CK}	–
PRECHARGE command period		t_{RP}	22.5	–	ns	8)

1) DQ, DM and DQS input slew rate is measured between $V_{ILD(DC)}$ and $V_{IHD(AC)}$ (rising) or $V_{IHD(DC)}$ and $V_{ILD(AC)}$ (falling).
2) DQ, DM and DQS input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
3) Input slew rate ≥ 1.0 V/ns..
4) Input slew rate ≥ 0.5V/ns and < 1.0 V/ns.
5) This parameter guarantees device timing. It is verified by device characterization but are not subject to production test.
6) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
7) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
8) These parameters account for the number of clock cycles and depend on the operating frequency, as follows: *no. of clock cycles = specified delay / clock period ; round to the next higher integer*.

During WRITE bursts, the first valid data-in element is registered on the first rising edge of DQS following the WRITE command, and subsequent data elements are registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble. The time between the WRITE command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range (from 75% to 125% of a clock cycle). The diagrams in **Figure 23** show the two extremes of t_{DQSS} for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data is ignored.

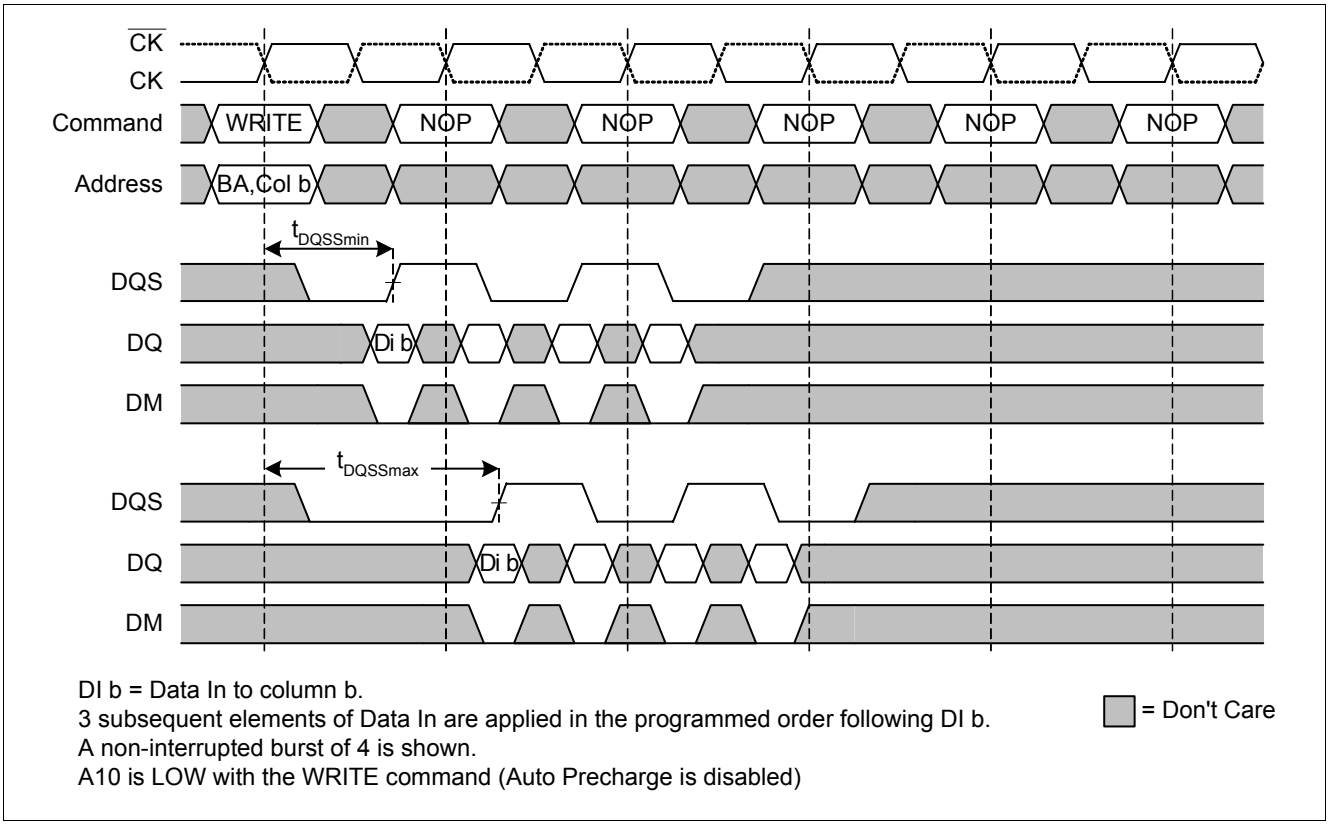


Figure 23 WRITE Burst (min. and max. tDQSS)

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any clock cycle following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued x clock cycles after the first WRITE command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture).

Figure 24 shows concatenated WRITE bursts of 4.

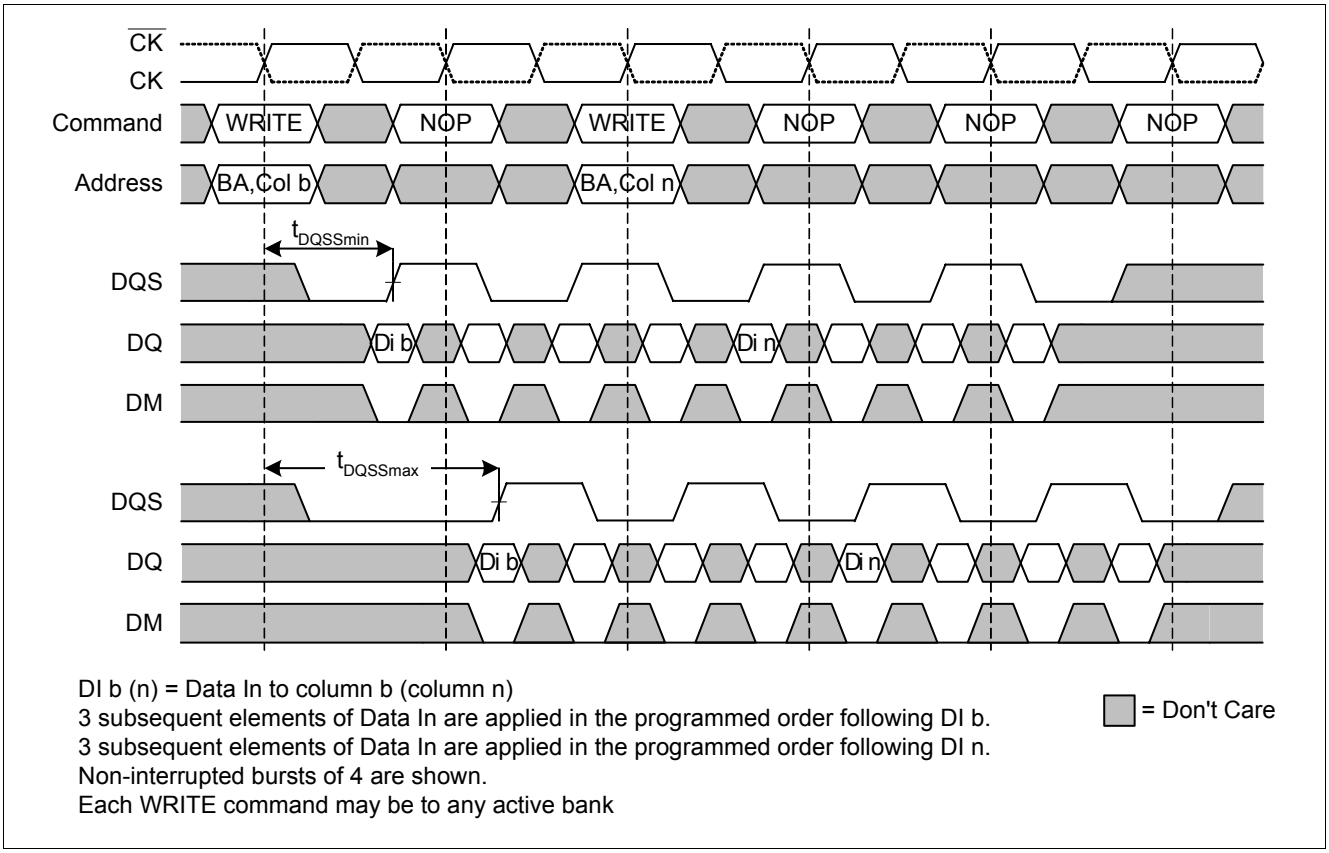


Figure 24 WRITE to WRITE (min. and max. tDQSS)

An example of non-consecutive WRITEs is shown in **Figure 25**.

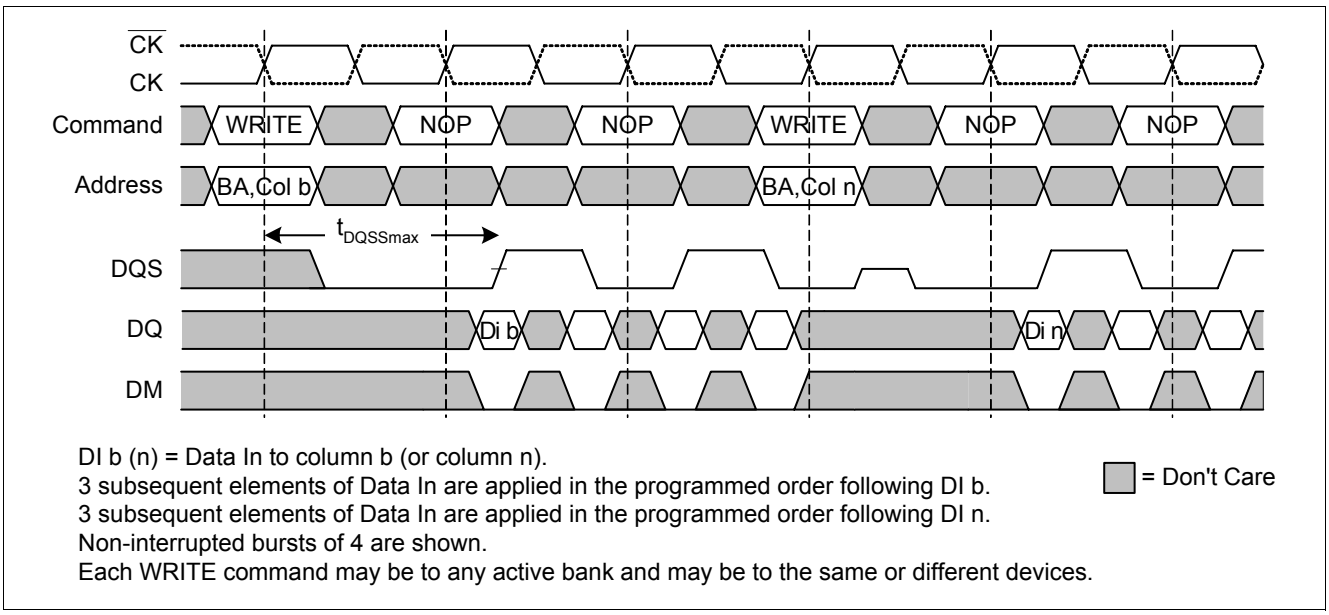


Figure 25 Non-Consecutive WRITE to WRITE (max. tDQSS)

Full-speed random WRITE accesses within a page or pages can be performed as shown in **Figure 26**.

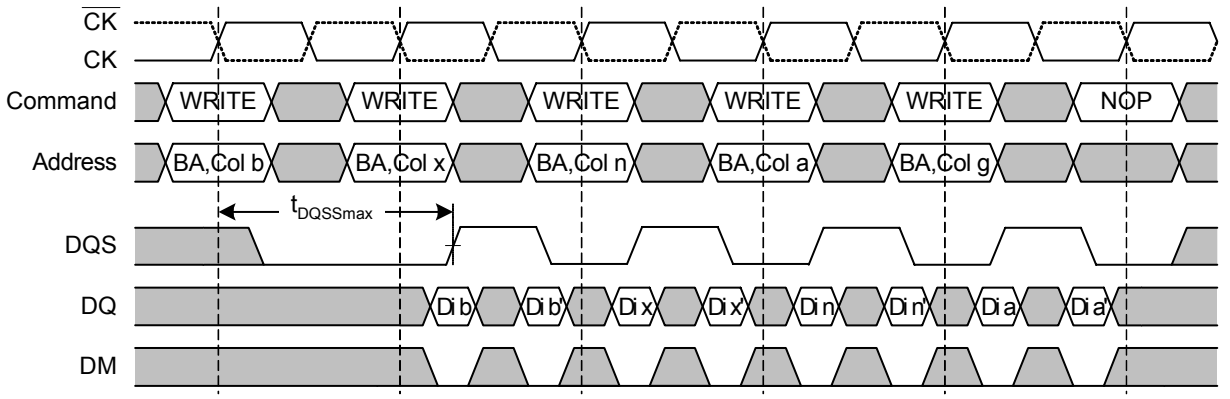


Figure 26 Random WRITE Cycles (max. tDQSS)

2.4.7.1 WRITE to READ

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst, t_{WTR} (WRITE to READ) should be met as shown in **Figure 27**.

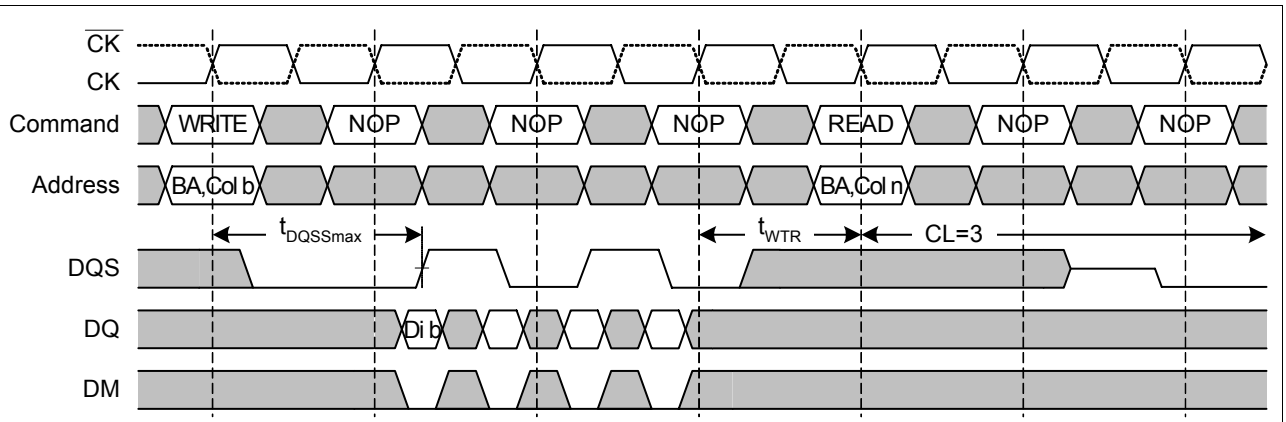
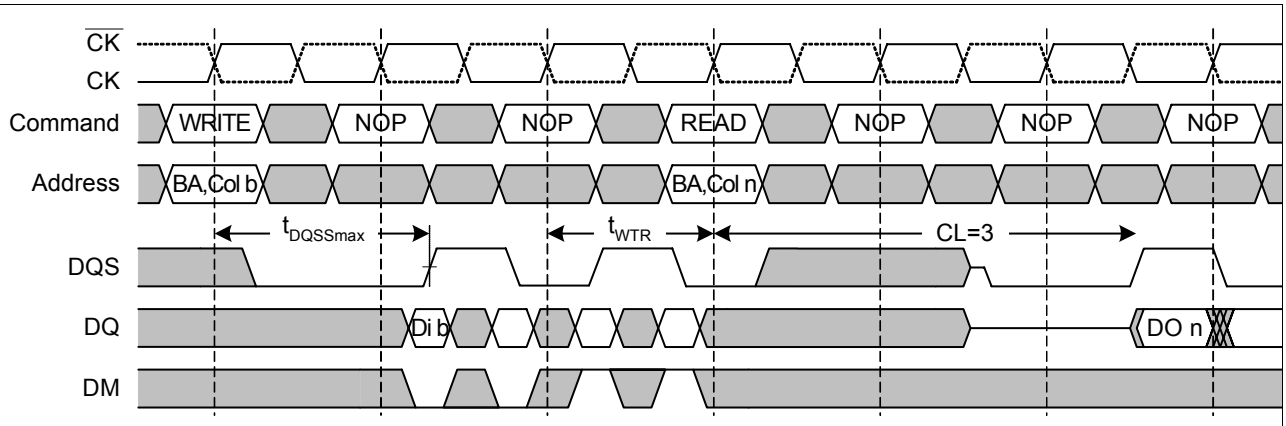


Figure 27 Non-Interrupting WRITE to READ (max. tDQSS)

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in **Figure 28**. Note that only the data-in pairs that are registered prior to the t_{WTR} period are written to the internal array, and any subsequent data-in must be masked with DM, as shown in **Figure 28**.



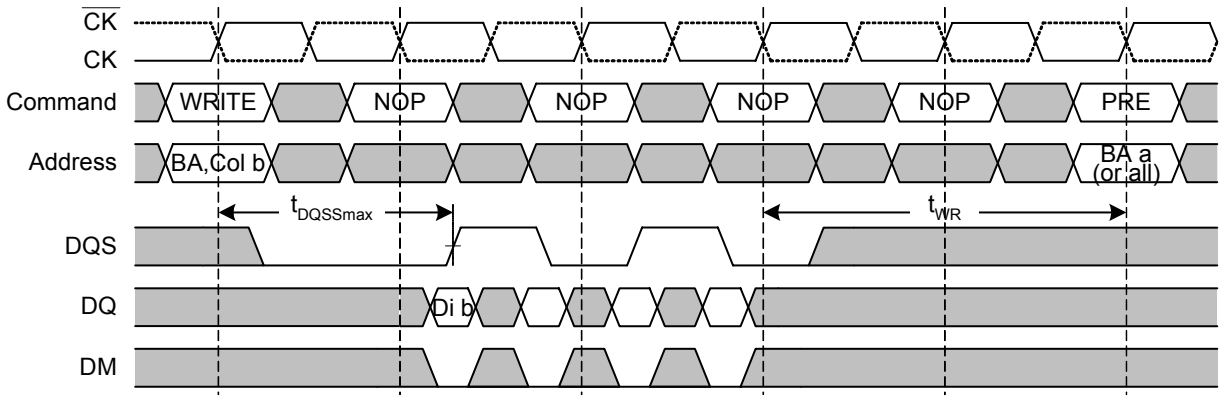
DI b = Data In to column b. DO n = Data Out from column n.
An interrupted burst of 4 is shown, 2 data elements are written.
3 subsequent elements of Data In are applied in the programmed order following DI b.
t_{WTR} is referenced from the positive clock edge after the last Data In pair.
A10 is LOW with the WRITE command (Auto Precharge is disabled)
The READ and WRITE commands are to the same device but not necessarily to the same bank.

= Don't Care

Figure 28 Interrupting WRITE to READ (Max. tDQSS)

2.4.7.2 WRITE to PRECHARGE

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, t_{WR} should be met as shown in **Figure 29**.



DI b = Data In to column b .
3 subsequent elements of Data In are applied in the programmed order following DI b.
A non-interrupted burst of 4 is shown.
t_{WR} is referenced from the positive clock edge after the last Data In pair.
A10 is LOW with the WRITE command (Auto Precharge is disabled)

= Don't Care

Figure 29 Non-Interrupting WRITE to PRECHARGE (Max. tDQSS)

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in **Figure 30**. Note that only the data-in pairs that are registered prior to the t_{WR} period are written to the internal array, and any

subsequent data in should be masked with DM. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

In the case of a WRITE burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same burst with Auto Precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

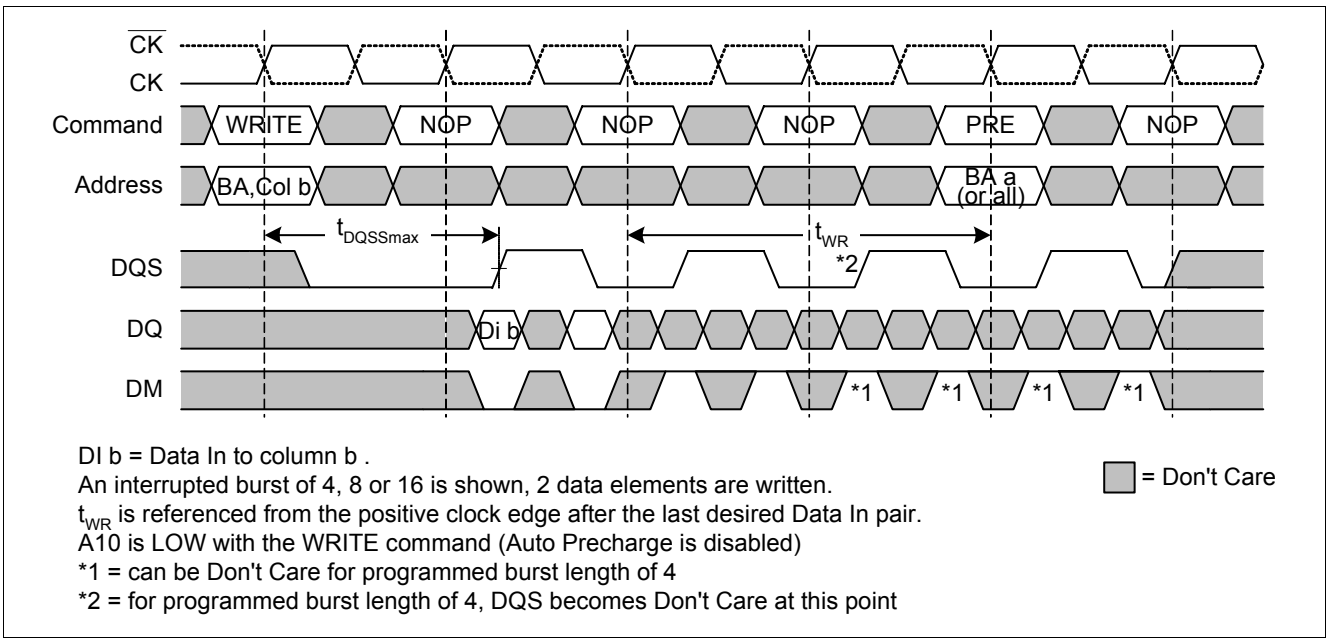


Figure 30 Interrupting WRITE to PRECHARGE (Max. tDQSS)

2.4.8 PRECHARGE

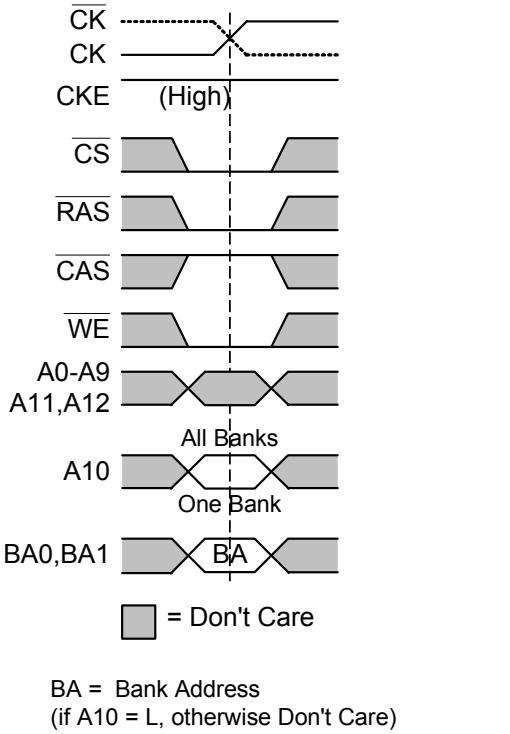


Figure 31 PRECHARGE Command

The PRECHARGE command is used to deactivate (close) the open row in a particular bank or the open rows in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.”

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

Table 13 Timing Parameters for PRECHARGE Command

Parameter	Symbol	- 7.5		Unit	Notes
		Min.	Max.		
ACTIVE to PRECHARGE command period	t_{RAS}	45	70,000	ns	1)
PRECHARGE command period	t_{RP}	22.5	–	ns	1)
WRITE recovery time	t_{WR}	15	–	ns	1)

1) These parameters account for the number of clock cycles and depend on the operating frequency, as follows:
no. of clock cycles = specified delay / clock period ; round to the next higher integer.

2.4.8.1 AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual-bank precharge functions described above, but without requiring an explicit command. This is accomplished by using A10 to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto Precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type.

2.4.9 AUTO REFRESH and SELF REFRESH

The DDR Mobile-RAM requires a refresh of all rows in an rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode. Dividing the number of rows into the rolling 64ms interval defines the average refresh interval, t_{REFI}, which is a guideline to controllers for distributed refresh timing.

2.4.9.1 AUTO REFRESH

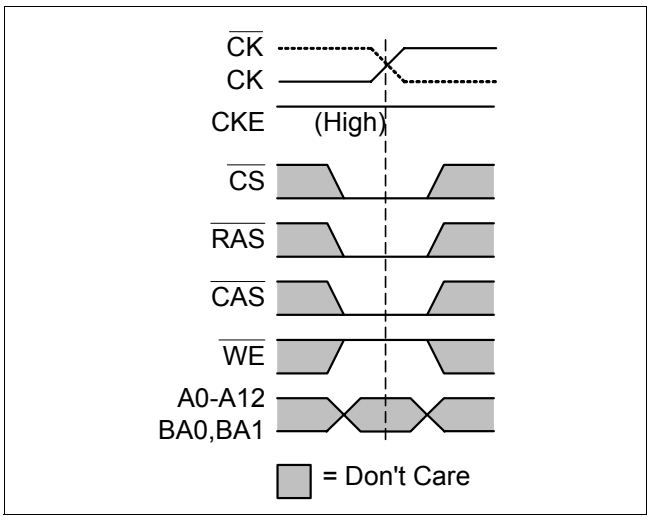


Figure 32 AUTO REFRESH Command

Auto Refresh is used during normal operation of the DDR Mobile-RAM. The command is nonpersistent, so it must be issued each time a refresh is required. A minimum time t_{RFC} is required between two AUTO REFRESH commands. The same rule applies to any access command after the Auto Refresh operation. All banks must be precharged prior to the AUTO REFRESH command.

The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. The DDR Mobile-RAM requires Auto Refresh cycles at an average periodic interval of t_{REFI} (max.).

Partial array mode has no influence on Auto Refresh mode.

To allow for improved efficiency in scheduling and switching between tasks, some fexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to the DDR Mobile-RAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 * t_{REFI}.

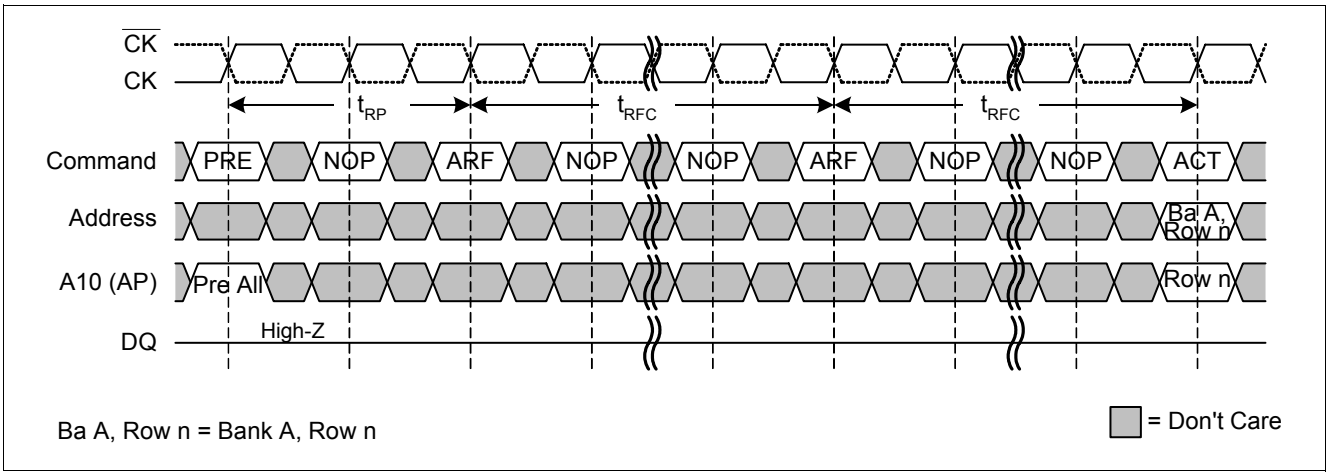


Figure 33 Auto Refresh

2.4.9.2 SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR Mobile-RAM, even if the rest of the system is powered down. When in the Self Refresh mode, the DDR Mobile-RAM retains data without external clocking. The DDR Mobile-RAM device has a built-in timer to accommodate Self Refresh operation. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is LOW. Input signals except CKE are “Don’t Care” during Self Refresh. The user may halt the external clock one clock after Self Refresh entry is registered.

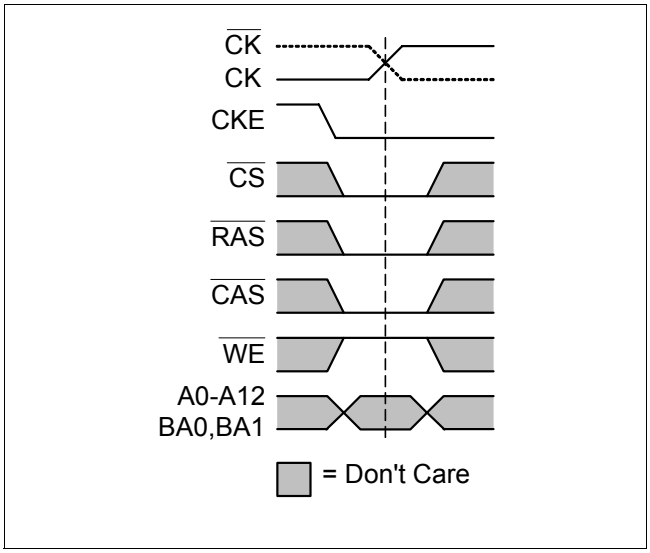


Figure 34 SELF REFRESH Entry Command

Once the command is registered, CKE must be held low to keep the device in Self Refresh mode. The device executes a minimum of one AUTO REFRESH command internally once it enters Self Refresh mode. The clock is internally disabled during Self Refresh operation to save power. The minimum time that the device must remain in Self Refresh mode is t_{RFC}.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least t_{XS} must be satisfied before a valid command can be issued to the device to allow for completion of any internal refresh in progress.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh an extra AUTO REFRESH command is recommended.

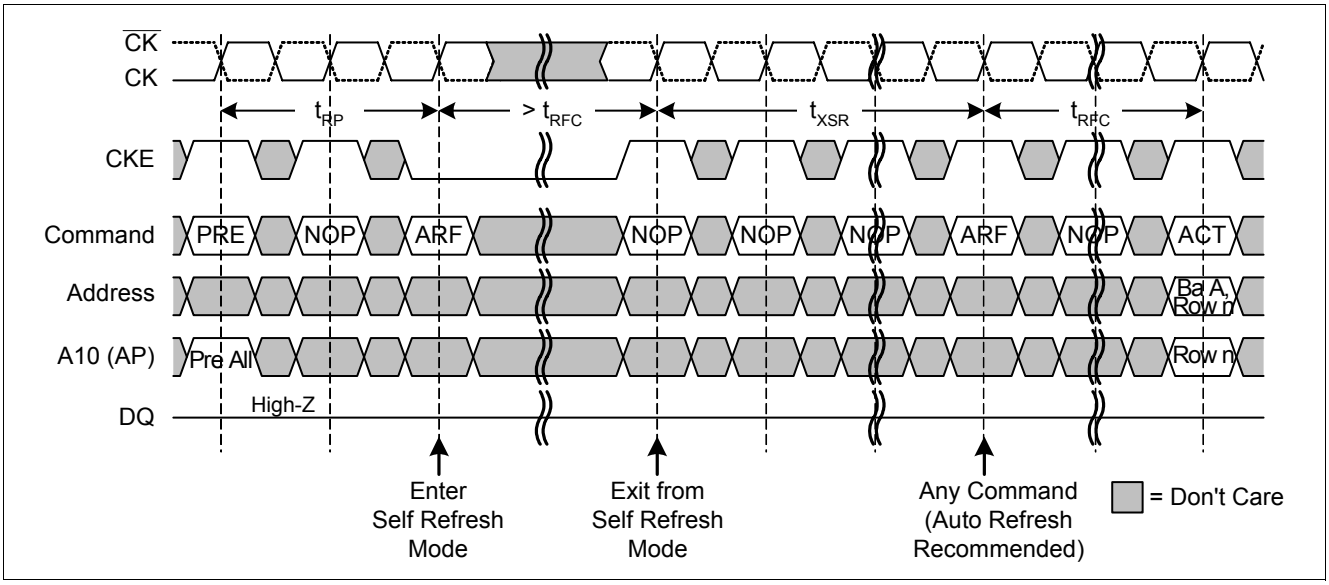


Figure 35 Self Refresh Entry and Exit

Table 14 Timing Parameters for AUTO REFRESH and SELF REFRESH Commands

Parameter	Symbol	- 7.5		Unit	Notes
		Min.	Max.		
AUTO REFRESH to ACTIVE/AUTO REFRESH command period	t_{RFC}	75	–	ns	1)
PRECHARGE command period	t_{RP}	22.5	–	ns	1)
Self refresh exit to next valid command delay	t_{XSR}	120	–	ns	1)
Refresh period	t_{REF}	–	64	ms	–
Average periodic refresh interval (8192 rows)	t_{REFI}	–	7.8	µs	2)

1) These parameters account for the number of clock cycles and depend on the operating frequency, as follows: *no. of clock cycles = specified delay / clock period ; round to the next higher integer*.

2) A maximum of eight AUTOREFRESH commands can be posted to the DDR Mobile-RAM device, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8 * tREFI.

2.4.10 POWER-DOWN

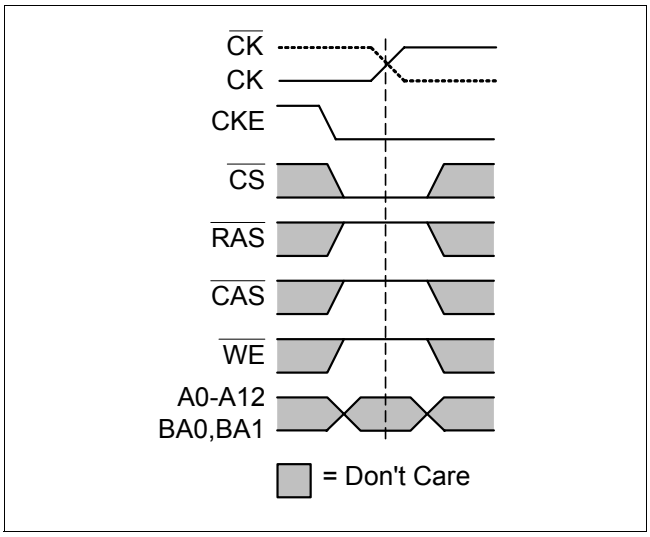


Figure 36 Power-Down Entry Command

Power-down is entered when CKE is registered LOW (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. In power-down mode, CKE LOW must be maintained, and all other input signals are “Don’t Care”. The minimum power-down duration is specified by t_{CKE}. However, power-down duration is limited by the refresh requirements of the device.

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESELECT command). A valid command may be applied t_{XP} after exit from power-down.

A minimum CKE high time of t_{CKE} is required between two consecutive power-down states.

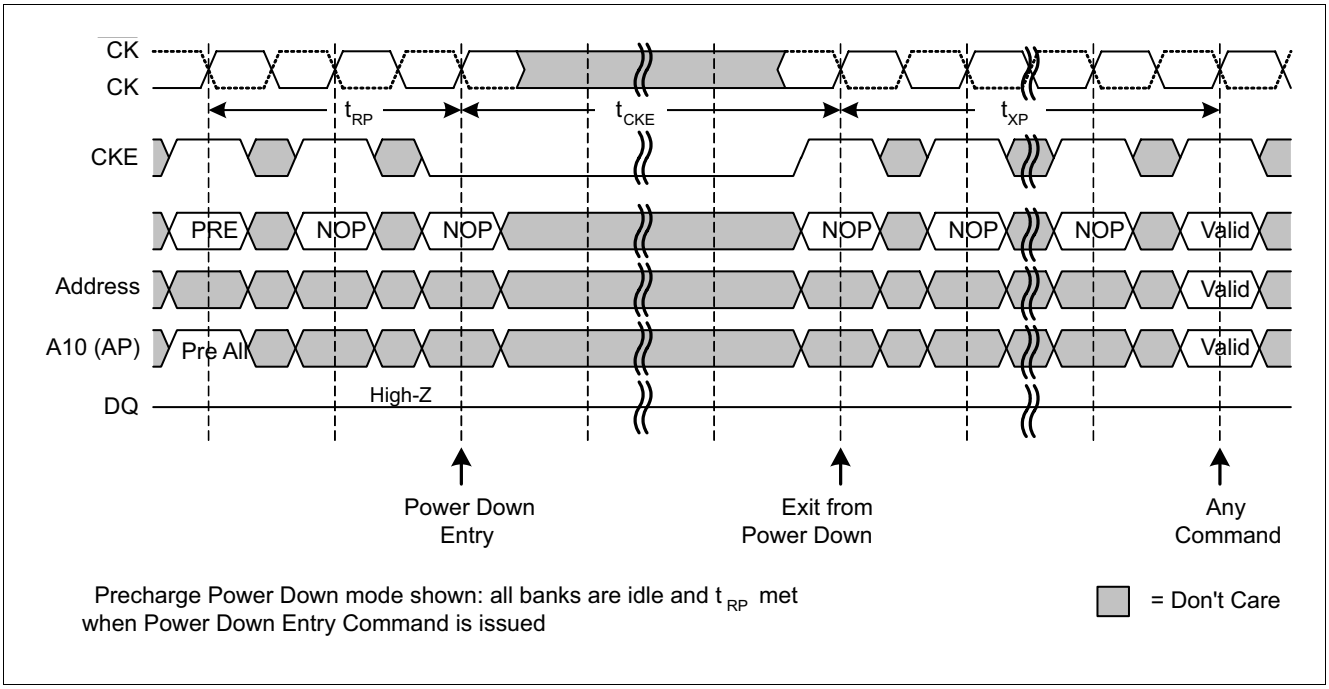


Figure 37 Power-Down Entry and Exit

Table 15 Timing Parameters for POWER-DOWN

Parameter	Symbol	- 7.5		Unit	Notes
		Min.	Max.		
Exit power down delay	t_{XP}	t_{CK}+ t_{IS}	–	ns	
CKE minimum high or low time	t_{CKE}	2	–	t_{CK}	–

2.4.10.1 DEEP POWER-DOWN

Deep Power-Down mode is a unique feature of DDR Mobile-RAMs for extremely low power consumption. Deep Power-Down mode is entered using the BURST TERMINATE command (cf **Table 6**) except that CKE is LOW. All internal voltage generators are stopped and all memory data is lost in this mode. To enter the Deep Power-Down mode all banks must be precharged.

The Deep Power-Down mode is asynchronously exited by asserting CKE HIGH. After the exit, the same command sequence as for power-up initialization, including the 200µs intial pause, has to be applied before any other command may be issued (cf. **Figure 4**).

2.4.11 CLOCK STOP

Stopping the clock during idle periods is a very effective method to reduce power consumption. The DDR Mobile-RAM supports clock stop in case:

- the last access command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of clock pulses per access command depends on the device's AC timing parameters and the clock frequency (see **Table 16**);
- the related timing condition (t_{RCD}, t_{WR}, t_{RP}, t_{RFC}, t_{MRD}) has been met;
- CKE is held HIGH.

When all conditions have been met, the device is either in "idle" or "row active" state (cf. **Figure 4**), and clock stop mode may be entered with CK held LOW and $\overline{CK}$ held HIGH.

Clock stop mode is exited by restarting the clock. At least one NOP command has to be issued before the next access command may be applied. Additional clock pulses might be required depending on the system characteristics.

Figure 38 illustrates the clock stop mode:

- initially the device is in clock stop mode;
- the clock is restarted with the rising edge of T0 and a NOP on the command inputs;
- with T1 a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command has completed;
- Tn is the last clock pulse required by the access command latched with T1
- the timing condition of this access command is met with the completion of Tn; therefore Tn is the last clock pulse required by this command and the clock is then stopped.

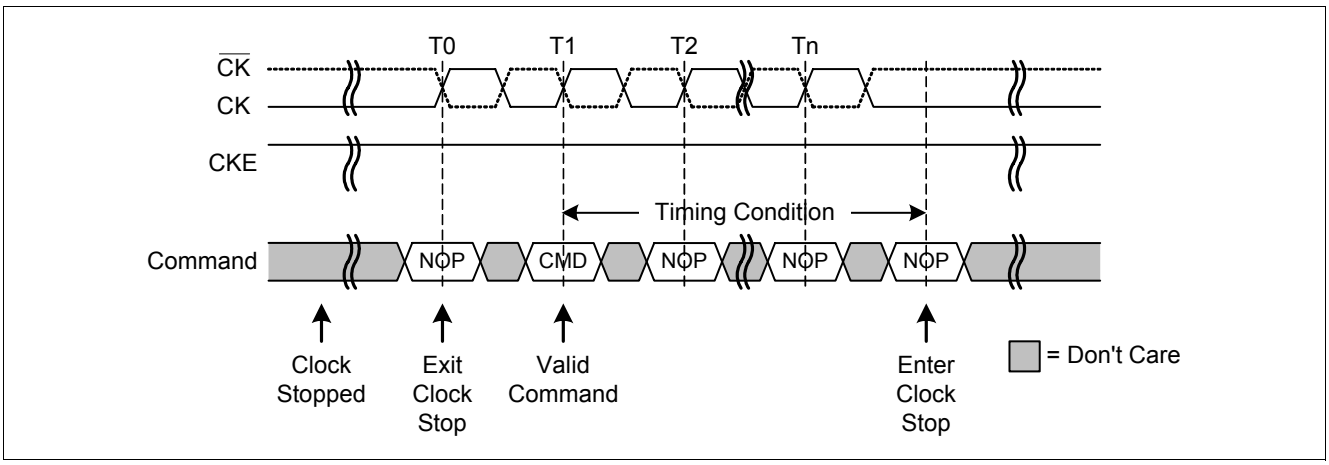


Figure 38 Clock Stop

Table 16 Minimum Number of Required Clock Pulses per Access Command

Command	Timing Condition	- 7.5	Unit	Notes
ACTIVE	t_{RCD}	3	t_{CK}	1)
READ (Auto-Precharge Disabled)	(BL / 2) + CL	5	t_{CK}	1)2)
READ (Auto-Precharge Enabled)	[(BL / 2) + t_{RP}] ; [(BL / 2) + CL]	5	t_{CK}	1)2)3)
WRITE (Auto-Precharge Disabled)	1 + (BL / 2) + t_{WR}	5	t_{CK}	1)2)
WRITE (Auto-Precharge Enabled)	1 + (BL / 2) + t_{DAL}	8	t_{CK}	1)2)
PRECHARGE	t_{RP}	3	t_{CK}	1)
AUTO REFRESH	t_{RFC}	10	t_{CK}	1)
MODE REGISTER SET	t_{MRD}	2	t_{CK}	

1) These parameters depend on the operating frequency; the number of clock cycles shown are calculated for a clock frequency of 133 MHz for -7.5.
2) The values apply for a burst length of 4 and a CAS latency of 3.
3) Both timing conditions need to be satisfied; if not equal, the larger value applies

2.4.12 Clock Frequency Change

Depending on system considerations, it might be desired to change the DDR Mobile-RAM's clock frequency while the device is powered up. The DDR Mobile-RAM supports a clock frequency change when the device is in:

- self refresh mode (see **Figure 35**);
- power-down mode (see **Figure 37**);
- clock stop mode (see **Figure 38**).

Once the clock runs stable at the new clock frequency, the timing conditions for exiting these states have to be met before applying the next access command. It should be pointed out that a continuous frequency drift is not considered a stable clock and therefore is not supported.

2.5 Function Truth Tables

Table 17 Truth Table - CKE

CKEn-1	CKEn	Current State	Command	Action	Notes
L	L	Power-Down	X	Maintain Power-Down	1)2)3)4)
		Self Refresh	X	Maintain Self Refresh	1) to 4)
		Deep Power-Down	X	Maintain Deep Power-Down	1) to 4)
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	1) to 5)
		Self Refresh	DESELECT or NOP	Exit Self Refresh	1) to 5)
		Deep Power-Down	X	Exit Deep Power-Down	1) to 4), 6)
H	L	All Banks Idle	DESELECT or NOP	Enter Precharge Power-Down	1) to 4)
		Bank(s) Active	DESELECT or NOP	Enter Active Power-Down	1) to 4)
		All Banks Idle	AUTO REFRESH	Enter Self Refresh	1) to 4)
		All Banks Idle	BURST TERMINATE	Enter Deep Power-Down	1) to 4)
H	H	see **Table 18** and **Table 19**			1) to 4)

1) CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2) Current state is the state immediately prior to clock edge n.
3) COMMAND n is the command registered at clock edge n; ACTION n is a result of COMMAND n.
4) All states and sequences not shown are illegal or reserved.
5) DESELECT or NOP commands should be issued on any clock edges occurring during t_{XP} or t_{XSR} period.
6) Exit from DEEP POWER DOWN requires the same command sequence as for power-up initialization.

Table 18 Current State Bank n - Command to Bank n

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command / Action	Notes
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	1)2)3)4)5)6)
	L	H	H	H	NO OPERATION (NOP / continue previous operation)	1) to 6)
Idle	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	L	L	H	AUTO REFRESH	1) to 7)
	L	L	L	L	MODE REGISTER SET	1) to 7)
Row Active	L	H	L	H	READ (select column and start Read burst)	1) to 6), 8)
	L	H	L	L	WRITE (select column and start Write burst)	1) to 6), 8)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1) to 6), 9)
Read (Auto-Precharge Disabled)	L	H	L	H	READ (truncate Read and start new Read burst)	1) to 6), 8)
	L	H	L	L	WRITE (truncate Read and start new Write burst)	1) to 6), 8), 10)
	L	L	H	L	PRECHARGE (truncate Read and start Precharge)	1) to 6), 9)
	L	H	H	L	BURST TERMINATE	1) to 6), 11)
Write (Auto-Precharge	L	H	L	H	READ (truncate Write and start Read burst)	1) to 6), 8), 12)
	L	H	L	L	WRITE (truncate Write and start Write burst)	1) to 6), 8)
	L	L	H	L	PRECHARGE (truncate Write burst, start Precharge)	1) to 6), 9),12)

1) This table applies when CKEn-1 was HIGH and CKEn is HIGH (see **Table 17**) and after t_{XP} or t_{XSR} has been met (if the previous state was power-down or self refresh).

2) This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.

3) Current state definitions:
   - Idle: The bank has been precharged, and t_{RP} has been met.
   - Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4) The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according to **Table 19**.
   - Precharging: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the “idle” state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the “row active” state.
   - Read with AP Enabled: Starts with registration of a READ command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   - Write with AP Enabled: Starts with registration of a WRITE command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.

5) The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.
   - Refreshing: Starts with registration of an AUTO REFRESH command and ends when t_{RC} is met. Once t_{RC} is met, the DDR Mobile-RAM is in the “all banks idle” state.
   - Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the DDR Mobile-RAM is in the “all banks idle” state.
   - Precharging All: Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks are in the idle state.

6) All states and sequences not shown are illegal or reserved.
7) Not bank-specific; requires that all banks are idle and no bursts are in progress.
8) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
9) May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
10) A WRITE command may be applied after the completion of the Read burst; otherwise, a BURST TERMINATE command must be used to end the Read burst prior to issuing a WRITE command.
11) Not bank-specific; BURST TERMINATE affects the most recent Read burst, regardless of bank.
12) Requires appropriate DM masking.

Table 19 Current State Bank n - Command to Bank m (different bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command / Action	Notes
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	1)2)3)4)5)6)
	L	H	H	H	NO OPERATION (NOP / continue previous operation)	1) to 6)
Idle	X	X	X	X	Any command otherwise allowed to bank m	1) to 6)
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (select column and start Read burst)	1) to 7)
	L	H	L	L	WRITE (select column and start Write burst)	1) to 7)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1) to 6)
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (truncate Read and start new Read burst)	1) to 7)
	L	H	L	L	WRITE (truncate Read and start Write burst)	1) to 8)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1) to 6)
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (truncate Write and start Read burst)	1) to 7), 9)
	L	H	L	L	WRITE (truncate Write and start new Write burst)	1) to 7)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1) to 6)
Read (with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (truncate Read and start new Read burst)	1) to 7)
	L	H	L	L	WRITE (truncate Read and start Write burst)	1) to 8)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1) to 6)
Write (with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	1) to 6)
	L	H	L	H	READ (truncate Write and start Read burst)	1) to 7)
	L	H	L	L	WRITE (truncate Write and start new Write burst)	1) to 7)
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	1) to 6)

1) This table applies when CKEn-1 was HIGH and CKEn is HIGH (see **Table 17**) and after t_{XP} or t_{XSR} has been met (if the previous state was power-down or self refresh).
2) This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

3) Current state definitions:
   - Idle: The bank has been precharged, and t_{RP} has been met.
   - Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Read with AP Enabled: see following text.
   - Write with AP Enabled: see following text.

   3a. The Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).

4) AUTO REFRESH, SELF REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5) A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6) All states and sequences not shown are illegal or reserved.
7) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
8) A WRITE command may be applied after the completion of the Read burst; otherwise, a BURST TERMINATE command must be used to end the Read burst prior to issuing a WRITE command.
9) Requires appropriate DM masking.

3 Electrical Characteristics

3.1 Operating Conditions

Table 20 Absolute Maximum Ratings

Parameter		Symbol	Values		Unit
			Min.	Max.	
Power Supply Voltage		V_{DD}	-0.3	2.7	V
Power Supply Voltage for Output Buffer		V_{DDQ}	-0.3	2.7	V
Input Voltage		V_{IN}	-0.3	V_{DDQ} + 0.3	V
Output Voltage		V_{OUT}	-0.3	V_{DDQ} + 0.3	V
Operation Case Temperature	Commercial	T_C	0	+70	°C
Storage Temperature		T_{STG}	-55	+150	°C
Power Dissipation		P_D	–	0.7	W
Short Circuit Output Current		I_{OUT}	–	50	mA

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 21 Pin Capacitances[1)2)3)]

Parameter	Symbol	Values		Unit
		Min.	Max.	
Input capacitance: CK, $\overline{CK}$	C_{I1}	1.5	2.5	pF
Delta input capacitance: CK, $\overline{CK}$	CD_{I1}	–	0.25	pF
Input capacitance: all other input-only pins	C_{I2}	1.5	2.5	pF
Delta input capacitance: all other input-only pins	CD_{I2}	–	0.5	pF
Input/output capacitance: DQ, DQS, DM	C_{IO}	3.5	4.5	pF
Delta input/output capacitance: DQ, DQS, DM	CD_{IO}	–	0.5	pF

1) These values are not subject to production test but verified by device characterization.

2) Input capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. VDD, VDDQ are applied and all other pins (except the pin under test) are floating. DQ's should be in high impedance state. This may be achieved by pulling CKE to low level.

3) Although DM is an input-only pin, it's input capacitance models the input capacitance of the DQ and DQS pins.

Table 22 Electrical Characteristics[1)2)]

Parameter	Symbol	Values		Unit	Notes
		Min.	Max.		
Power Supply Voltage	V_{DD}	1.70	1.90	V	–
Power Supply Voltage for DQ Output Buffer	V_{DDQ}	1.70	1.90	V	–
Input leakage current	I_{IL}	-1.0	1.0	µA	–
Output leakage current	I_{OL}	-1.5	1.5	µA	–
Address and Command Inputs (BA0, BA1, A0 - A12, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)					
Input high voltage	V_{IH}	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	–
Input low voltage	V_{IL}	-0.3	0.2 × V_{DDQ}	V	–
Clock Inputs (CK, $\overline{CK}$)					
DC input voltage	V_{IN}	-0.3	V_{DDQ} + 0.3	V	–
DC input differential voltage	$V_{ID(DC)}$	0.4 × V_{DDQ}	V_{DDQ} + 0.6	V	3)
AC input differential voltage	$V_{ID(AC)}$	0.6 × V_{DDQ}	V_{DDQ} + 0.6	V	3)
AC differential cross point voltage	V_{IX}	0.4 × V_{DDQ}	0.6 × V_{DDQ}	V	4)
Data Inputs (DQ0 - DQ15, LDM, UDM, LDQS, UDQS)					
DC input high voltage	$V_{IHD(DC)}$	0.7 × V_{DDQ}	V_{DDQ} + 0.3	V	–
DC input low voltage	$V_{ILD(DC)}$	-0.3	0.3 x V_{DDQ}	V	–
AC input high voltage	$V_{IHD(AC)}$	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	–
AC input low voltage	$V_{ILD(AC)}$	-0.3	0.2 × V_{DDQ}	V	–
Data Outputs (DQ0 - DQ15, LDQS, UDQS)					
Output high voltage	V_{OH}	0.9 × V_{DDQ}	–	V	–
Output low voltage	V_{OL}	–	0.1 × V_{DDQ}	V	–

1) 0 °C ≤ T_C ≤ 70 °C (comm.);
All voltages referenced to V_{SS}. V_{SS} and V_{SSQ} must be at same potential.

2) See **Table 25** and **Figure 39** for overshoot and undershoot definition.

3) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

4) The value of V_{IX} is expected to be equal to 0.5 x V_{DDQ} and must track variations in the DC level.

3.2 AC Characteristics

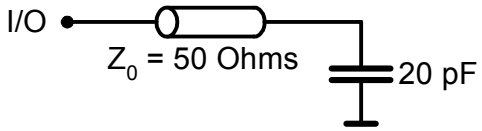
Table 23 AC Characteristics[1)2)3)4)]

Parameter		Symbol	- 7.5		Unit	Notes
			Min.	Max.		
DQ output access time from CK/$\overline{CK}$		t_{AC}	2.0	6.5	ns	5)6)
DQS output access time from CK/$\overline{CK}$		t_{DQSCK}	2.0	6.5	ns	5)6)
Clock high-level width		t_{CH}	0.45	0.55	t_{CK}	–
Clock low-level width		t_{CL}	0.45	0.55	t_{CK}	–
Clock half period		t_{HP}	min(t_{CL},t_{CH})		ns	7)8)
Clock cycle time	CL = 3	t_{CK}	7.5	–	ns	9)
	CL = 2		15	–		
DQ and DM input setup time	fast slew rate	t_{DS}	0.75	–	ns	10)11)12)
	slow slew rate		0.85	–		10)11)13)
DQ and DM input hold time	fast slew rate	t_{DH}	0.75	–	ns	10)11)12)
	slow slew rate		0.85	–		10)11)13)
DQ and DM input pulse width		t_{DIPW}	1.7	–	ns	14)
Address and control input setup time	fast slew rate	t_{IS}	1.3	–	ns	12)15)16)
	slow slew rate		1.5	–		13)15)16)
Address and control input hold time	fast slew rate	t_{IH}	1.3	–	ns	12)15)16)
	slow slew rate		1.5	–		13)15)16)
Address and control input pulse width		t_{IPW}	3.0	–	ns	14)
DQ & DQS low-impedance time from CK/$\overline{CK}$		t_{LZ}	1.0	–	ns	17)
DQ & DQS high-impedance time from CK/$\overline{CK}$		t_{HZ}	–	6.5	ns	17)
DQS - DQ skew		t_{DQSQ}	–	0.6	ns	18)
DQ / DQS output hold time from DQS		t_{QH}	t_{HP}-t_{QHS}	–	ns	8)
Data hold skew factor		t_{QHS}	–	0.75	ns	8)
Write command to 1st DQS latching transition		t_{DQSS}	0.75	1.25	t_{CK}	–
DQS input high-level width		t_{DQSH}	0.4	0.6	t_{CK}	–
DQS input low-level width		t_{DQSL}	0.4	0.6	t_{CK}	–
DQS falling edge to CK setup time		t_{DSS}	0.2	–	t_{CK}	–
DQS falling edge hold time from CK		t_{DSH}	0.2	–	t_{CK}	–
MODE REGISTER SET command period		t_{MRD}	2	–	t_{CK}	–
Write preamble setup time		t_{WPRES}	0	–	ns	19)
Write postamble		t_{WPST}	0.4	0.6	t_{CK}	20)
Write preamble		t_{WPRE}	0.25	–	t_{CK}	–
Read preamble	CL = 3	t_{RPRE}	0.9	1.1	t_{CK}	21)
	CL = 2		0.7	1.1		
Read postamble		t_{RPST}	0.4	0.6	t_{CK}	–
ACTIVE to PRECHARGE command period		t_{RAS}	45	70,000	ns	22)
ACTIVE to ACTIVE command period		t_{RC}	65	–	ns	22)
AUTO REFRESH to ACTIVE/AUTO REFRESH command period		t_{RFC}	75	–	ns	22)
ACTIVE to READ or WRITE delay		t_{RCD}	22.5	–	ns	22)
PRECHARGE command period		t_{RP}	22.5	–	ns	22)
ACTIVE bank A to ACTIVE bank B delay		t_{RRD}	15	–	ns	22)
WRITE recovery time		t_{WR}	15	–	ns	22)
Auto precharge write recovery + precharge time		t_{DAL}			t_{CK}	23)

Table 23 AC Characteristics[1)2)3)4)] (cont'd)

Parameter	Symbol	- 7.5		Unit	Notes
		Min.	Max.		
Internal write to Read command delay	t_{WTR}	1	–	t_{CK}	–
Self refresh exit to next valid command delay	t_{XSR}	120	–	ns	22)
Exit power down delay	t_{XP}	t_{CK}+ t_{IS}	–	ns	
CKE minimum high or low time	t_{CKE}	2	–	t_{CK}	–
Refresh period	t_{REF}	–	64	ms	–
Average periodic refresh interval (8192 rows)	t_{REFI}	–	7.8	µs	24)

1) 0 °C ≤ T_C ≤ 70 °C (comm.); V_{DD} = V_{DDQ} = 1.70 V - 1.90 V. All voltages referenced to V_{SS}.
2) All parameters assume proper device initialization.
3) The CK/$\overline{CK}$ input reference level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/$\overline{CK}$ is V_{DDQ}/2.
4) All AC timing characteristics assume an input slew rate of 1.0 V/ns.
5) The output timing reference level is V_{DDQ}/2.
6) Parameters t_{ac} and t_{DQSCK} are specified for full drive strength and a reference load as shown below. This circuit is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. For half drive strength with a nominal load of 10pF parameters t_{AC} and t_{DQSCK} are expected to be in the same range. However, these parameters are not subject to production test but are estimated by device characterization. Use of IBIS or other simulation tools for system validation is suggested.



7) Min (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
8) t_{QH} = t_{HP} - t_{QHS}, where t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL}, t_{CH}). t_{QHS} accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
9) The only time that the clock frequency is allowed to change is during power-down, self-refresh or clock stop modes.
10) DQ, DM and DQS input slew rate is measured between $V_{ILD(DC)}$ and $V_{IHD(AC)}$ (rising) or $V_{IHD(DC)}$ and $V_{ILD(AC)}$ (falling).
11) DQ, DM and DQS input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
12) Input slew rate ≥ 1.0 V/ns..
13) Input slew rate ≥ 0.5V/ns and < 1.0 V/ns.
14) These parameters guarantee device timing. They are verified by device characterization but are not subject to production test.
15) The transition time for address and command inputs is measured between V_{IH} and V_{IL}.
16) A CK/$\overline{CK}$ differential slew rate of 2.0 V/ns is assumed for this parameter.
17) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
18) t_{DQSQ} consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
19) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
20) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

21) A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).

22) These parameters account for the number of clock cycles and depend on the operating frequency, as follows: *no. of clock cycles = specified delay / clock period ; round to the next higher integer*.

23) t_{DAL} = (t_{WR} / t_{CK}) + (t_{RP} / t_{CK}): for each of the terms above, if not already an integer, round to the next higher integer.

24) A maximum of eight AUTOREFRESH commands can be posted to the DDR Mobile-RAM device, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8 * tREFI.

Table 24 Output Slew Rate Characteristics [1)]

Parameter	Typical Range	Minimum	Maximum	Unit	Notes
Pullup and Pulldown Slew Rate (Full Drive Buffer)	TBD	0.7	2.5	V/ns	2)
Pullup and Pulldown Slew Rate (Half Drive Buffer)	TBD	0.3	1.0	V/ns	2)
Output Slew Rate Matching Ratio (Pullup to Pulldown)	-	0.7	1.4	-	3)

1) Output slew rate is measured between $V_{ILD(DC)}$ and $V_{IHD(AC)}$ (rising) or $V_{IHD(DC)}$ and $V_{ILD(AC)}$ (falling).

2) The parameter is measured using a 20pF capacitive load connected to VSSQ.

3) The ratio of the pullup slew rate to the pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

Table 25 AC Overshoot / Undershoot Specification

Parameter	Maximum	Unit	Notes
Maximum peak amplitude allowed for overshoot	0.9	V	–
Maximum peak amplitude allowed for undershoot	0.9	V	–
Maximum overshoot area above VDD	3.0	V-ns	–
Maximum undershoot area below VSS	3.0	V-ns	–

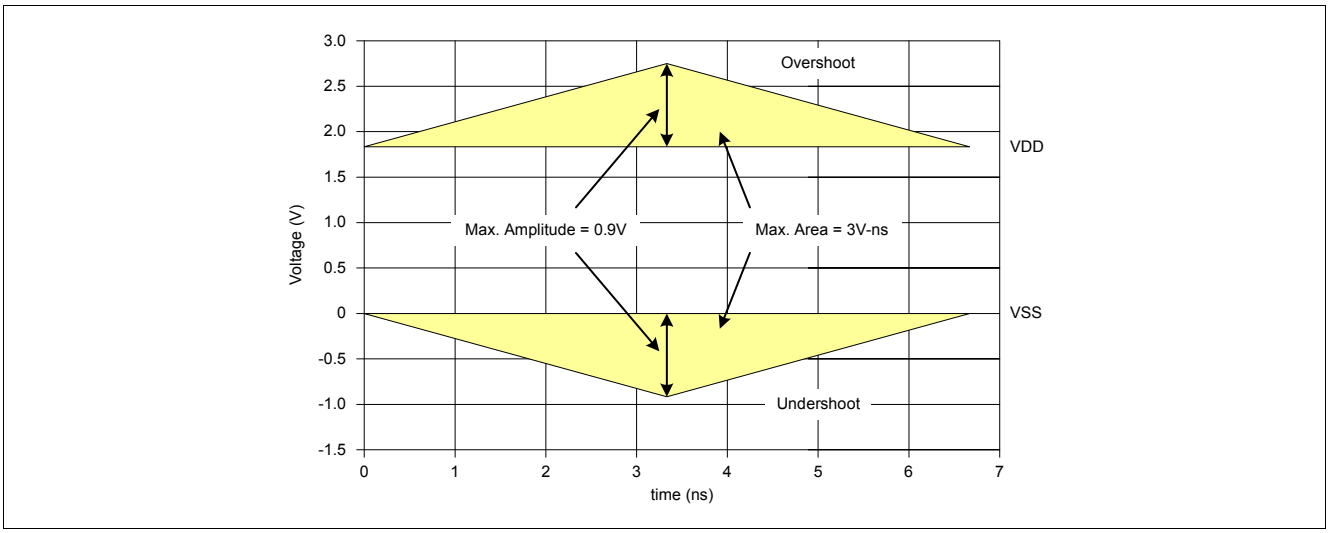


Figure 39 AC Overshoot and Undershoot Definition

3.3 Operating Currents

Table 26 Maximum Operating Currents[1)2)3)4)5)]

Parameter & Test Conditions	Symbol	Value	Unit
		- 7.5	
Operating one bank active-precharge current: $t_{RC} = t_{RCmin}$; $t_{CK} = t_{CKmin}$; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	I_{DD0}	50	mA
Precharge power-down standby current: all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2P}	2.2	mA
Precharge power-down standby current with clock stop: all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2PS}	2.1	mA
Precharge non power-down standby current: all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2N}	15	mA
Precharge non power-down standby current with clock stop: all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD2NS}	2.6	mA
Active power-down standby current: one bank active, CKE is LOW; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3P}	2.3	mA
Active power-down standby current with clock stop: one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3PS}	2.2	mA
Active non power-down standby current: one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, $t_{CK} = t_{CKmin}$; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3N}	22	mA
Active non power-down standby current with clock stop: one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD3NS}	2.7	mA
Operating burst read current: one bank active; BL = 4; CL = 3; $t_{CK} = t_{CKmin}$; continuous read bursts; I_{OUT} = 0 mA; address inputs are SWITCHING; 50% data change each burst transfer	I_{DD4R}	75	mA
Operating burst write current: one bank active; BL = 4; $t_{CK} = t_{CKmin}$; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	I_{DD4W}	75	mA
Auto-Refresh current: $t_{RC} = t_{RFCmin}$; $t_{CK} = t_{CKmin}$; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	I_{DD5}	135	mA
Self refresh current: CKE is LOW; CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are STABLE; data bus inputs are STABLE	I_{DD6}	2	mA
Deep Power Down current	I_{DD8}	50[6)]	µA

1) 0 °C ≤ T_C ≤ 70 °C (comm.); $V_{DD} = V_{DDQ}$ = 1.70 V - 1.90 V.
Recommended Operating Conditions unless otherwise noted

2) IDD specifications are tested after the device is properly intialized and measured at 133 MHz for -7.5 speed grade.

3) Input slew rate is 1.0 V/ns.

4) Definitions for IDD:
   LOW is defined as $V_{IN} \leq 0.1 * V_{DDQ}$;
   HIGH is defined as $V_{IN} \geq 0.9 * V_{DDQ}$;
   STABLE is defined as inputs stable at a HIGH or LOW level;
   SWITCHING is defined as:
   - address and command: inputs changing between HIGH and LOW once per two clock cycles;
   - data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE
5) All parameters are measured with no output loads.
6) I_{DD8} current is typical.

4 Package Outlines

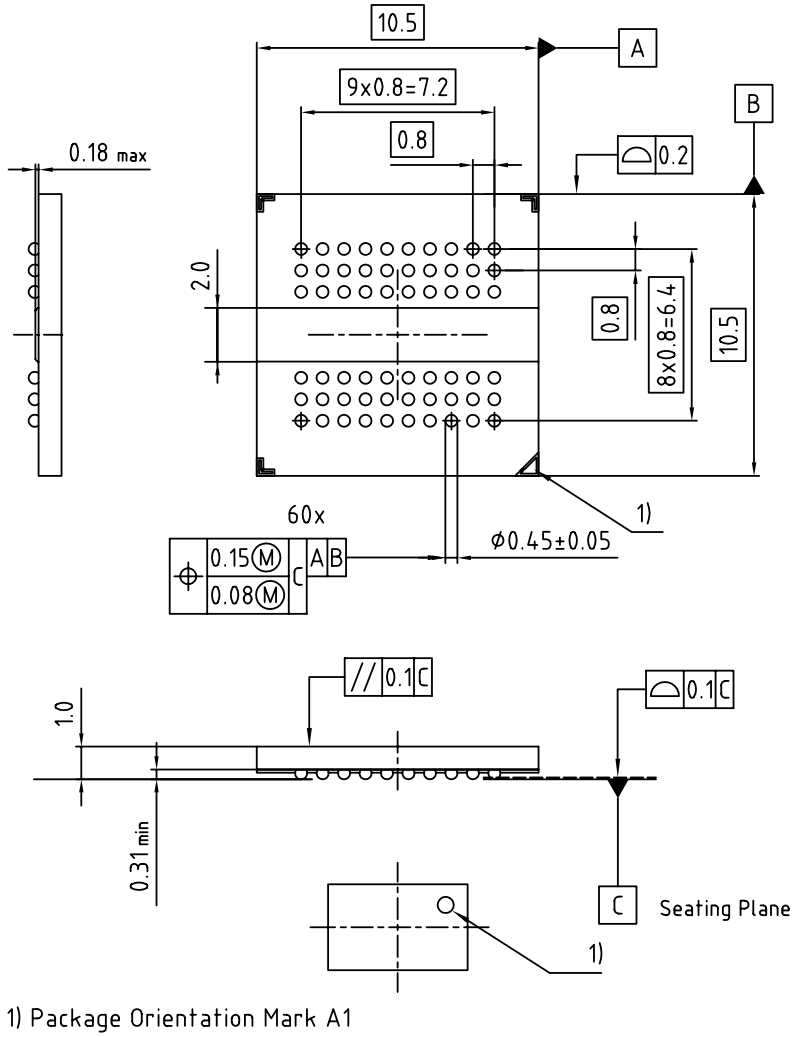


Figure 40 **P-VFBGA-60-1** (Plastic Very Thin Fine Ball Grid Array Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

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