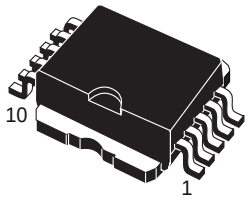
VND670SP

DUAL HIGH SIDE SWITCH WITH DUAL POWER MOS GATE DRIVER (BRIDGE CONFIGURATION)

TYPE	$R_{DS(on)}$	I_{OUT}	V_{DSS}
VND670SP	30 mΩ	15 A	40 V

- OUTPUT CURRENT:15A PER CHANNEL
- 5V LOGIC LEVEL COMPATIBLE INPUTS
- GATE DRIVE FOR TWO EXTERNAL POWER MOS
- UNDERVOLTAGE AND OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CROSS-CONDUCTION PROTECTION
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER CONSUMPTION
- PWM OPERATION UP TO 10 KHz
- PROTECTION AGAINST:
  LOSS OF GROUND AND LOSS OF V_{CC}
- REVERSE BATTERY PROTECTION (*)

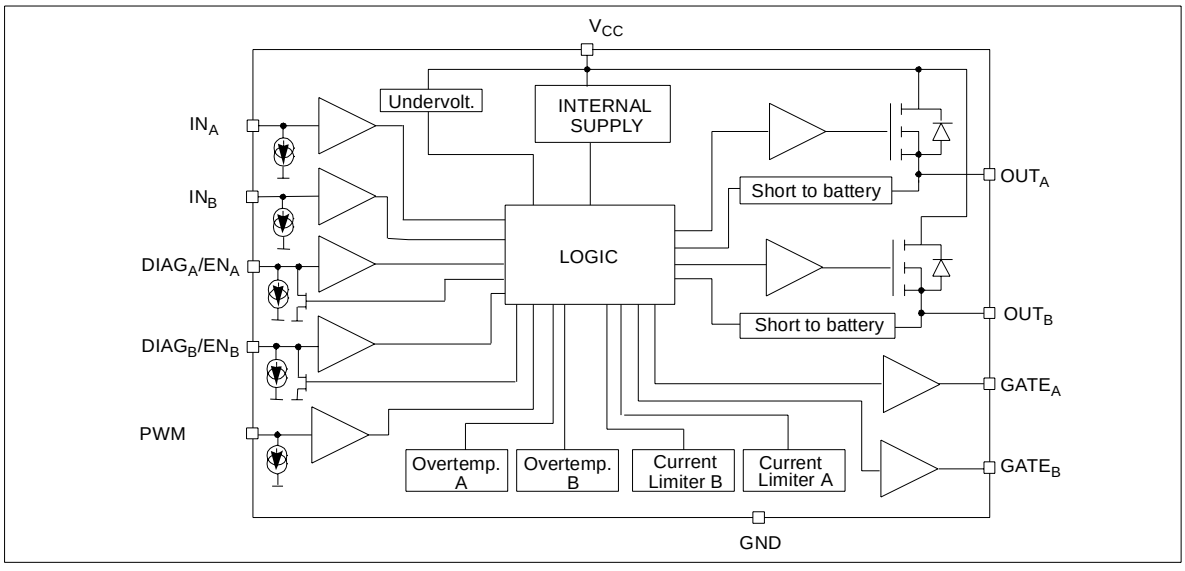


PowerSO-10™

DESCRIPTION

The VND670SP is a monolithic device made using STMicroelectronics VIPower technology M0-3, intended for driving motors in full bridge configuration. The device integrates two 30 mΩ Power MOSFET in high side configuration, and provides gate drive for two external Power MOSFET used as low side switches. IN_A and IN_B allow to select clockwise or counter clockwise drive or brake; $DIAG_A/EN_A$, $DIAG_B/EN_B$ allow to disable one half bridge and feedback diagnostic. Built-in thermal shut-down, combined with a current limiter, protects the chip in overtemperature and short circuit conditions. Short to battery protects the external connected low-side Power MOSFET.

BLOCK DIAGRAM

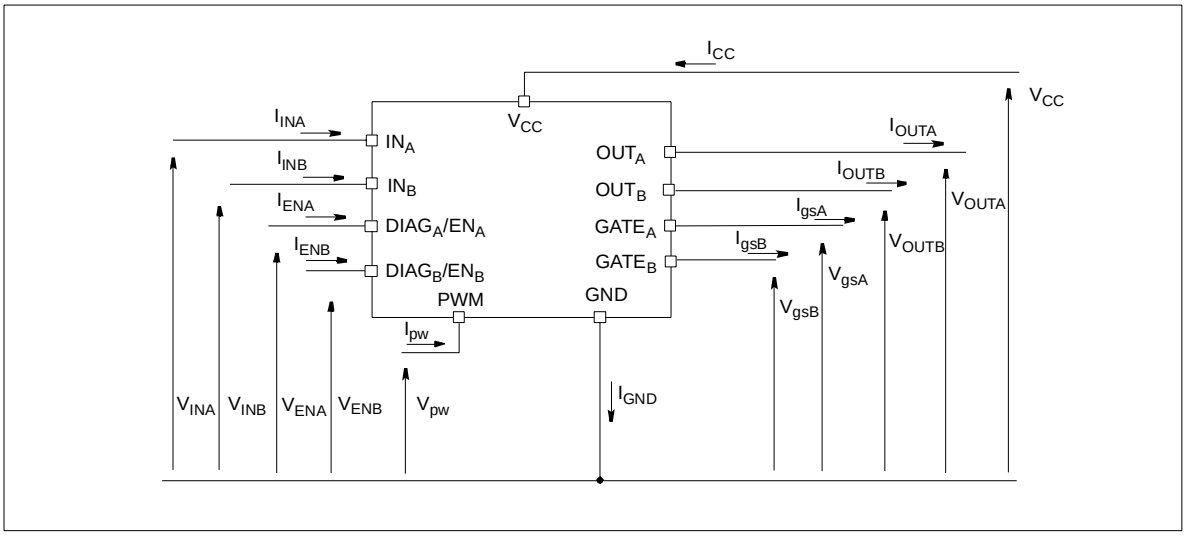


(*) See note at page 5

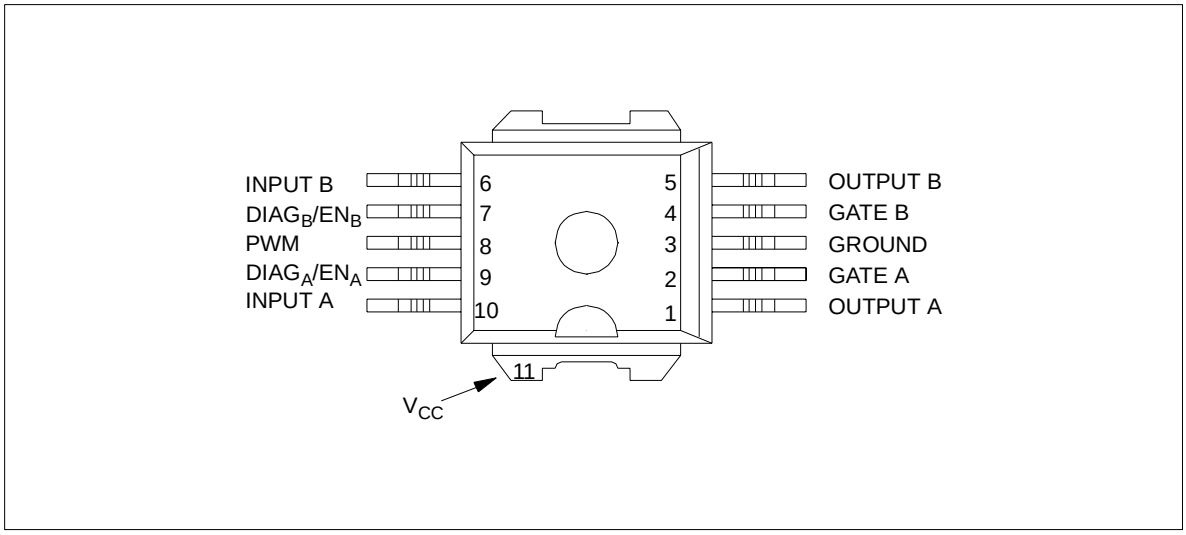
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 .. 40	V
I_{max1}	Maximum output current (continuous)	15	A
I_{max2}	Maximum output current (250 ms pulse duration)	20	A
I_R	Reverse output current (continuous)	-15	A
I_{IN}	Input current	+/- 10	mA
I_{EN}	Enable pin current	+/- 10	mA
I_{pw}	PWM pin current	+/- 10	mA
I_{gs}	Output gate current	+/- 20	mA
V_{ESD}	Electrostatic discharge (R=1.5kΩ, C=100pF)	2000	V
T_j	Junction operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

CURRENT AND VOLTAGE CONVENTIONS



CONNECTION DIAGRAM (TOP VIEW)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (per channel)	(MAX)	1.4	°C/W
$R_{thj\text{-}amb}$ (*)	Thermal resistance junction-ambient	(MAX)	50	°C/W

(*) When mounted using the recommended pad size on FR-4 board (See AN515 Application Note).

ELECTRICAL CHARACTERISTICS (V_{CC}=9V up to 18V; -40°C<T_j<150°C; unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		5.5		36	V
R_{ON}	On state resistance	I_{LOAD}=12A I_{LOAD}=12A; Tj=25ºC		 26	50 30	mΩ mΩ
I_s	Supply current	ON state OFF state			15 40	mA µA
V_{gate}	Gate output voltage		5.0		8.5	V
$V_{gs,cl}$	Gate output clamp voltage	I_{gs}=-1 mA	6.0	6.8	8.0	V

SWITCHING (V_{CC}=13V, R_{LOAD} =1.1Ω)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{D(on)}$	Turn-on delay time	Input rise time < 1µs (see fig. 1)		50	150	µs
$t_{D(off)}$	Turn-off delay time			45	135	µs
t_r	Output voltage rise time			50	150	µs
t_f	Output voltage fall time			40	120	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope			160	500	V/ms
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope			230	1200	V/ms
t_{dong}	V_{gs}Turn-on delay time	C1=4.7nF Break to ground configuration (see fig. 2)		0.5	2	µs
t_{rg}	V_{gs} rise time			2.6	10	µs
t_{doffg}	V_{gs}Turn-off delay time			1.0	5.0	µs
t_{fg}	V_{gs} fall time			2.2	10	µs
t_{del}	External MOSFET turn-on dead time	(see fig. 3)	150	600	1800	µs

PROTECTION AND DIAGNOSTIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{USD}	Undervoltage shut-down				5.5	V
V_{OV}	Overvoltage shut-down		36	43		V
I_{LIM}	Current limitation		30	45		A
T_{TSD}	Thermal shut-down temperature	V_{IN} = 3.25 V	150	170	200	°C
V_{ocl}	Output turn-off clamp voltage	I_{LOAD}=12A, L=6mH	V_{CC}-55		V_{CC}-41	V
V_{sat}	External MOSFET saturation voltage detection threshold		2.5	4.2	5.5	V

ELECTRICAL CHARACTERISTICS (continued)

PWM

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{pwl}	PWM low level voltage				1.5	V
I_{pwl}	PWM pin current	V_{pw}=1.5V	1			µA
V_{pwh}	PWM high level voltage		3.25			V
I_{pwh}	PWM pin current	V_{pw}=3.25V			10	µA
$V_{pwhhyst}$	PWM hysteresis voltage		0.5			V
V_{pwcl}	PWM clamp voltage	I_{pw} = 1 mA I_{pw} = -1 mA	V_{CC}+0.3 -5.0	V_{CC}+0.7 -3.5	V_{CC}+1.0 -2.0	V V
V_{pwtest}	Test mode PWM pin voltage		-3.5	-2.0	-0.5	V
I_{pwtest}	Test mode PWM pin current	V_{pwtest} = -2.0 V	-2000	-500		µA

LOGIC INPUT (IN_A/IN_B)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				1.5	V
I_{INL}	Input current	V_{IN}=1.5 V	1			µA
V_{IH}	Input high level voltage		3.25			V
I_{INH}	Input current	V_{IN}=3.25 V			10	µA
V_{IHYST}	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN}=1mA I_{IN}=-1mA	6.0 -1.0	6.8 -0.7	8.0 -0.3	V V

ENABLE (LOGIC I/O PIN)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{ENL}	Enable low level voltage	Normal operation ($DIAG_X$/EN_X pin acts as an input pin)			1.5	V
I_{ENL}	Enable pin current	V_{EN}= 1.5 V	1			µA
V_{ENH}	Enable high level voltage	Normal operation ($DIAG_X$/EN_X pin acts as an input pin)	3.25			V
I_{ENH}	Enable pin current	V_{EN}= 3.25 V			10	µA
V_{EHYST}	Enable hysteresis voltage	Normal operation ($DIAG_X$/EN_X pin acts as an input pin)	0.5			V
V_{ENCL}	Enable clamp voltage	I_{EN}=1mA I_{EN}=-1mA	6.0 -1.0	6.8 -0.7	8.0 -0.3	V V
V_{DIAG}	Enable output low level voltage	Fault operation ($DIAG_X$/EN_X pin acts as an input pin) I_{EN}=1.6 mA			0.4	V

WAVEFORMS AND TRUTH TABLE

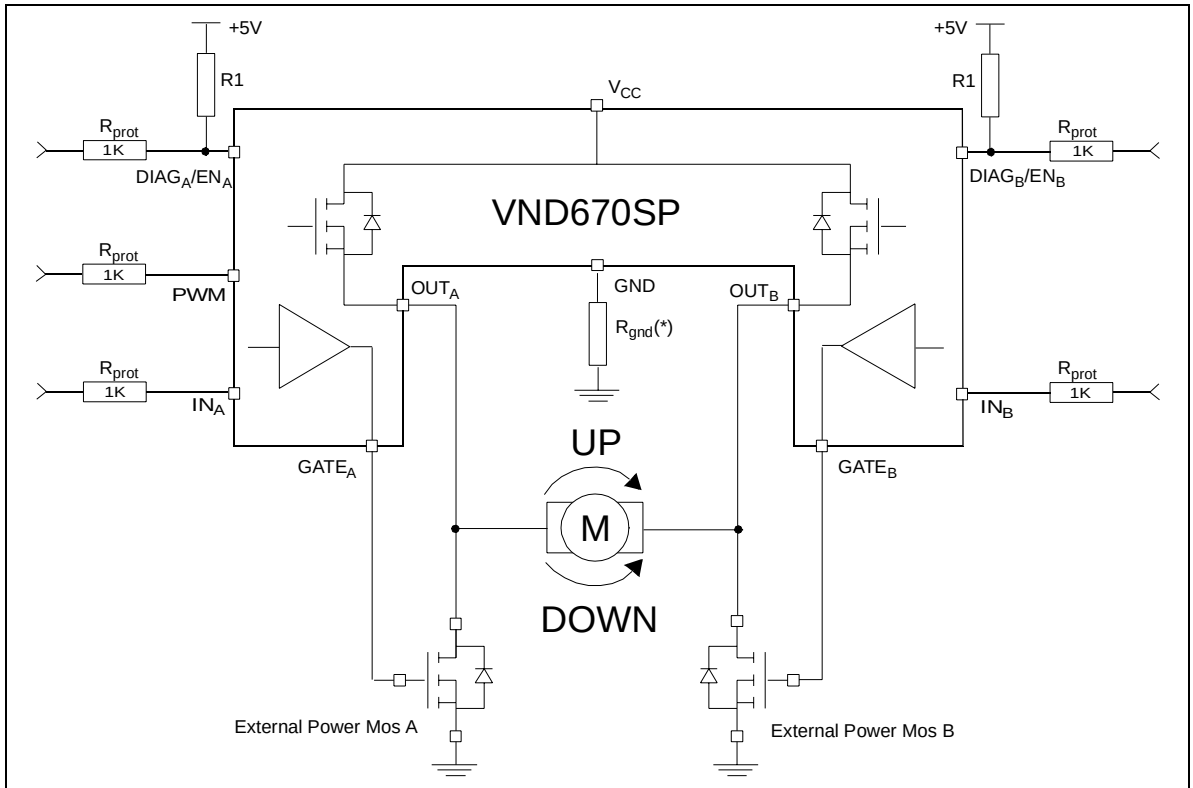
TRUTH TABLE IN NORMAL OPERATING CONDITIONS

In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	$GATE_A$	$GATE_B$	Comment
1	1	1	1	H	H	L	L	Brake to V_{CC}
1	0	1	1	H	L	L	H	Clockwise
0	1	1	1	L	H	H	L	Counter cw
0	0	1	1	L	L	H	H	Brake to GND
X	X	0	0	L	L	L	L	Stand by
1	X	1	0	H	L	L	L	HS_A only
0	X	1	0	L	L	H	L	MOS_A only
X	1	0	1	L	H	L	L	HS_B only
X	0	0	1	L	L	L	H	MOS_B only

PWM pin usage:
In all cases, a “0” on the PWM pin will turn-off both $GATE_A$ and $GATE_B$ outputs. When PWM rises back to “1”, $GATE_A$ or $GATE_B$ turn on again depending on the input pin state.

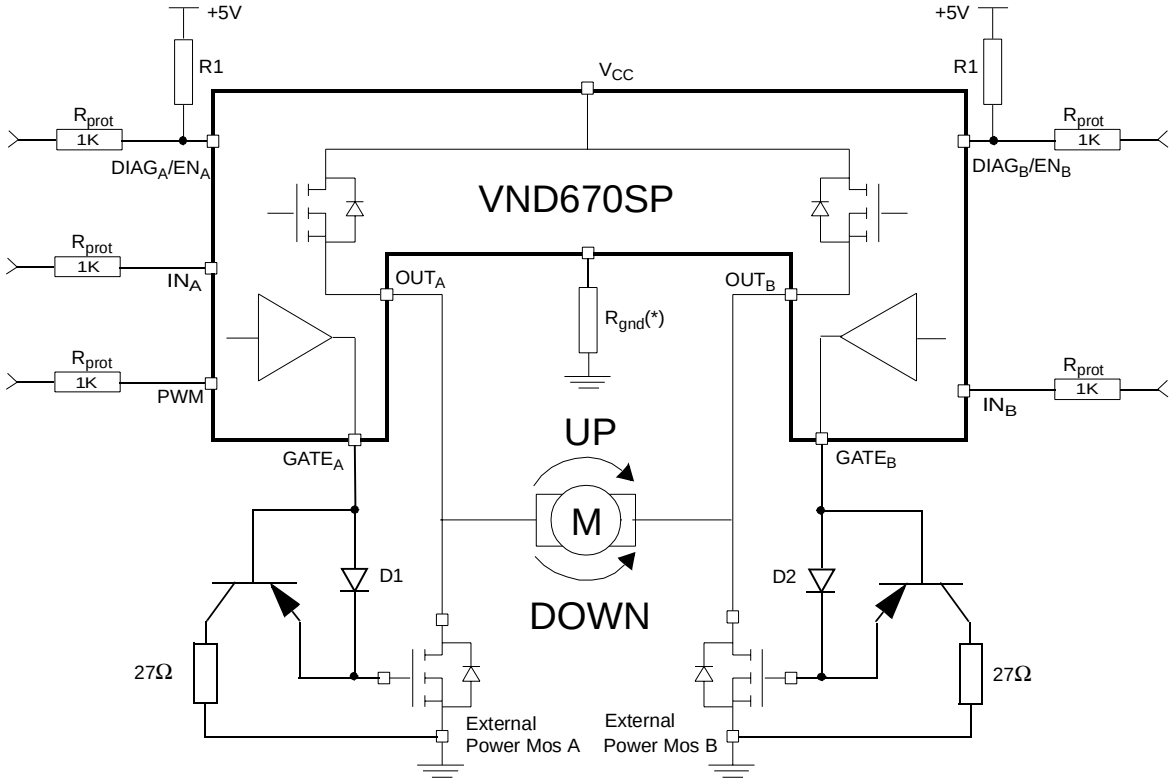
TYPICAL APPLICATION CIRCUIT FOR DC TO 10KHz PWM OPERATION



(*) Reverse battery protection:
- series relay in V_{CC} line: R_{gnd}=0 Ohms
- series fuse in V_{CC} line with antiparallel diode between ground and V_{CC}: R_{gnd}=10 Ohms.

Layout hints:
The connection between GND pin of the VN670SP and the Power MOSFET SOURCE connections should be kept short enough to ensure that the dynamic difference between these two points never exceed 1V for the bridge to operate properly.

TYPICAL APPLICATION CIRCUIT FOR A 20KHZ PWM OPERATION



(*) Reverse battery protection:

- series relay in V_{CC} line: R_{gnd}=0 Ohms
- series fuse in V_{CC} line with antiparallel diode between ground and V_{CC}: R_{gnd}=10 Ohms.

WAVEFORMS AND TRUTH TABLE (CONTINUED)

In case of a fault condition the $DIAG_X/EN_X$ pin is considered as an output pin by the device.
The fault conditions are:
- overtemperature on one or both high sides;
- short to battery condition on the output (saturation detection on the external connected Power MOSFET).

Possible origins of fault conditions may be:
OUT_A is shorted to ground ---> overtemperature detection on high side A.
OUT_A is shorted to V_{CC} ---> external Power MOSFET saturation detection (driven by $GATE_A$).
When a fault condition is detected, the user can know which power element is in fault by monitoring the IN_A, IN_B, $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins.
In any case, when a fault is detected, the faulty half bridge is latched off. To turn-on the respective output ($GATE_X$ or OUT_X) again, the input signal must rise from low to high level.

TRUTH TABLE IN FAULT CONDITIONS (detected on OUT_A)

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	$GATE_A$	$GATE_B$
1	1	0	1	OPEN	H	L	L
1	0	0	1	OPEN	OPEN	L	L
0	1	0	1	OPEN	H	L	L
0	0	0	1	OPEN	OPEN	L	L
X	X	0	0	OPEN	OPEN	L	L
1	X	0	0	OPEN	OPEN	L	L
0	X	0	0	OPEN	OPEN	L	L
X	1	0	1	OPEN	H	L	L
X	0	0	1	OPEN	OPEN	L	L

Fault Information

Protection Action

TEST MODE

The PWM pin allows to test the load connection between two half-bridges. In the test mode (V_{pwm}=-2V) the external Power Mos gate drivers are disabled. The IN_A or IN_B inputs allow to turn-on the High Side A or B, respectively, in order to connect one side of the load at V_{CC} voltage. The check of the voltage on the other side of the load allow to verify the continuity of the load connection. In case of load disconnection the $DIAD_X/EN_X$ pin corresponding to the faulty output is pulled down.

ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	Test Level I	Test Level II	Test Level III	Test Level IV	Test Levels Delays and Impedance
1	-25V	-50V	-75V	-100V	2ms, 10Ω
2	+25V	+50V	+75V	+100V	0.2ms, 10Ω
3a	-25V	-50V	-100V	-150V	0.1µs, 50Ω
3b	+25V	+50V	+75V	+100V	0.1µs, 50Ω
4	-4V	-5V	-6V	-7V	100ms, 0.01Ω
5	+26.5V	+46.5V	+66.5V	+86.5V	400ms, 2Ω

ISO T/R 7637/1 Test Pulse	Test Levels Result I	Test Levels Result II	Test Levels Result III	Test Levels Result IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 1: Test conditions for High Side switching times measurement.

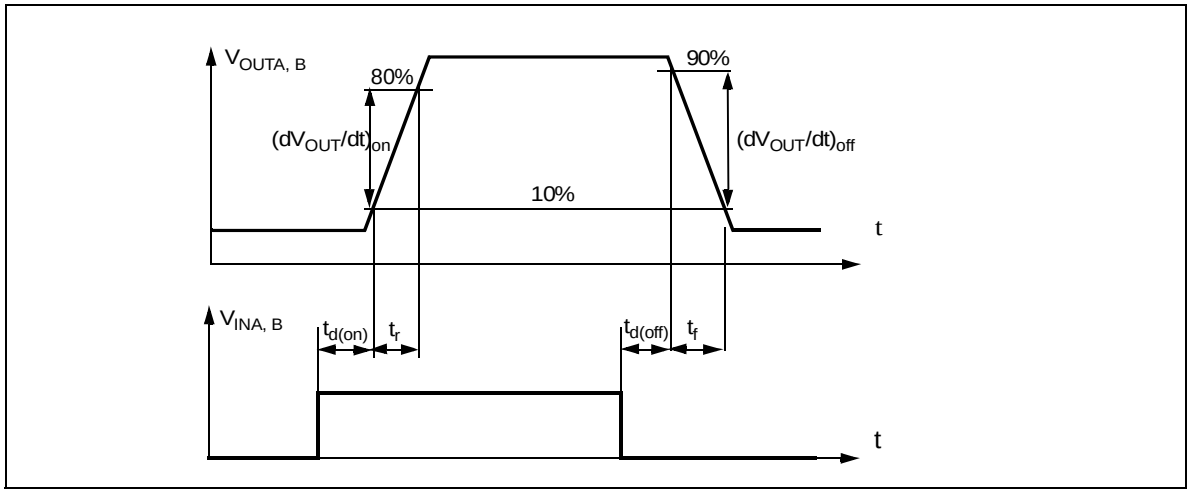


Figure 2: Test conditions for external Power MOSFET switching times measurement.

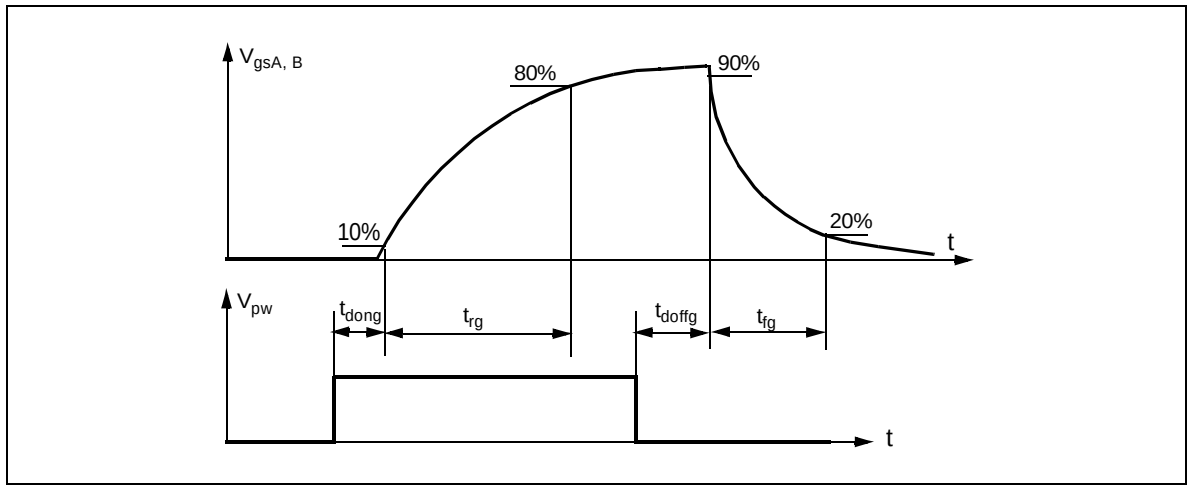
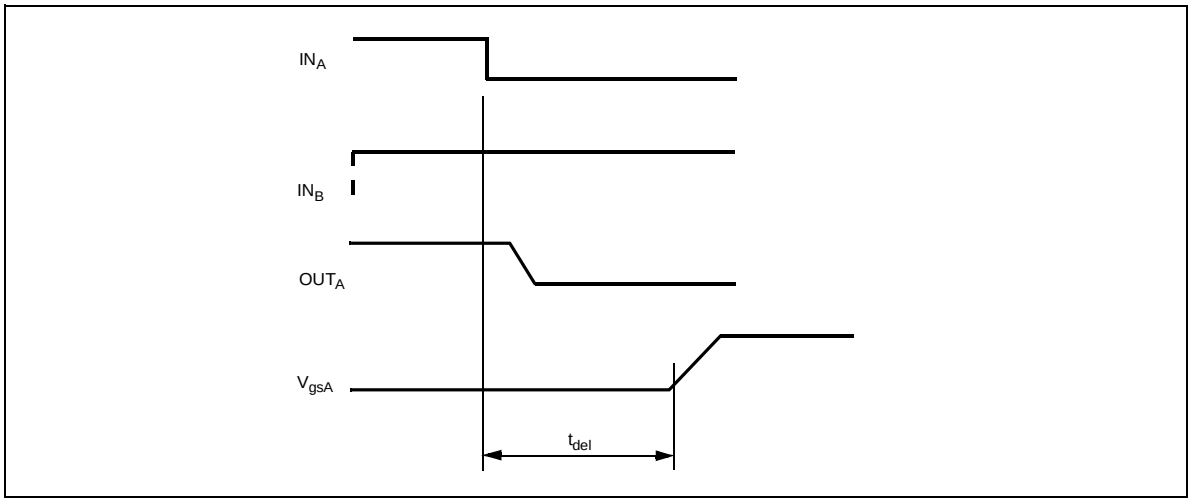
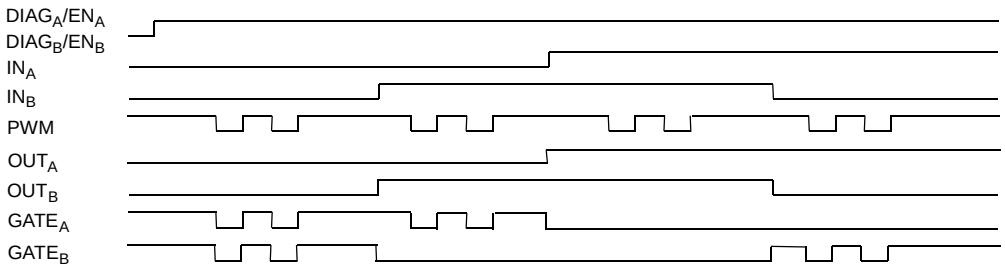


Figure 3: Definition of the external Power MOSFET turn-on dead time t_{del}

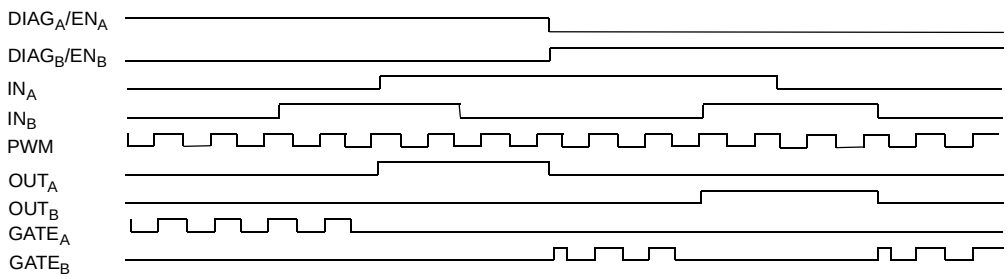


Waveforms

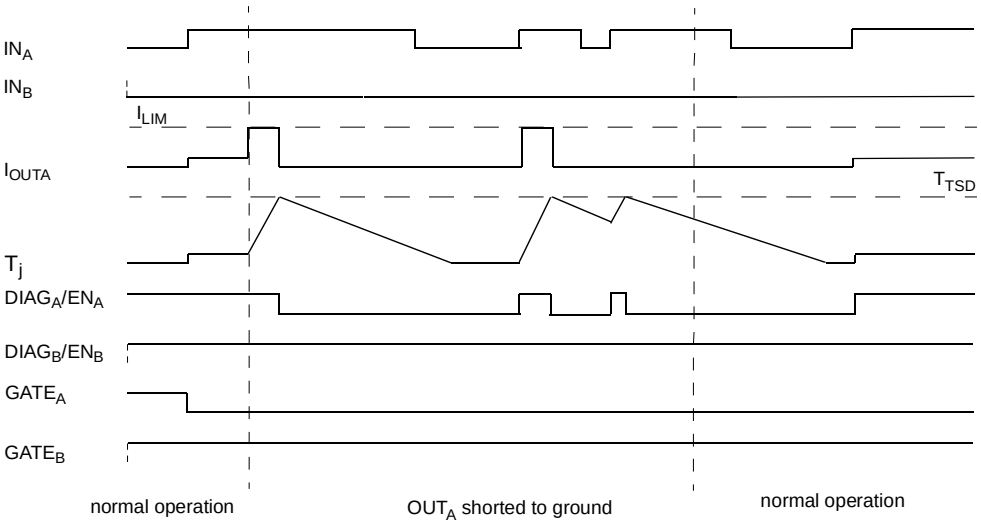
NORMAL OPERATION ($DIAG_A/EN_A$=1, $DIAG_B/EN_B$=1)



NORMAL OPERATION ($DIAG_A/EN_A$=1, $DIAG_B/EN_B$=0 and $DIAG_A/EN_A$=0, $DIAG_B/EN_B$=1)

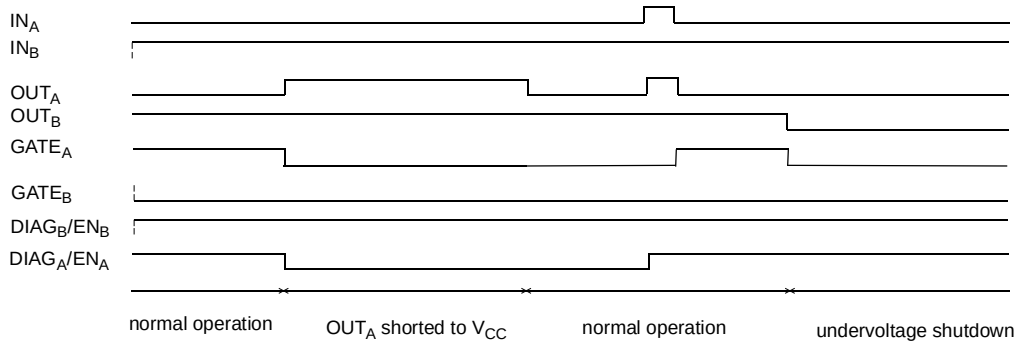


CURRENT LIMITATION/THERMAL SHUTDOWN or OUT_A SHORTED TO GROUND

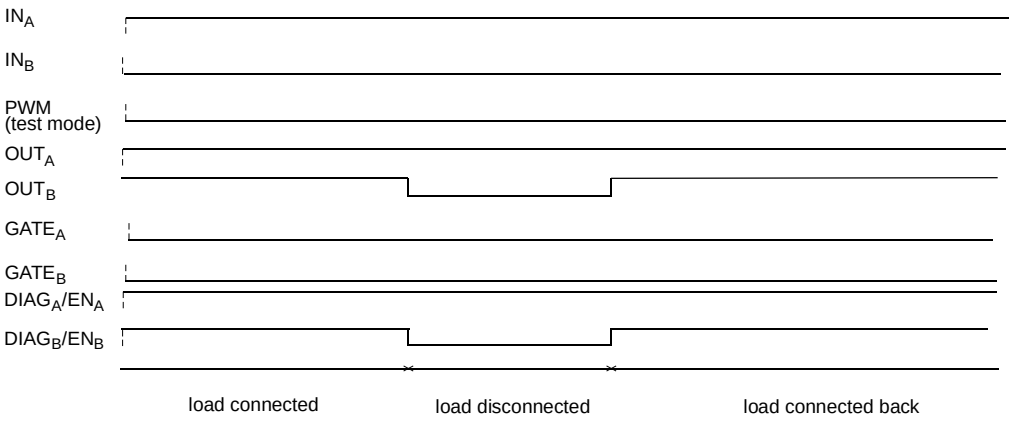


Waveforms (Continued)

OUT_A shorted to V_{CC} and undervoltage shutdown



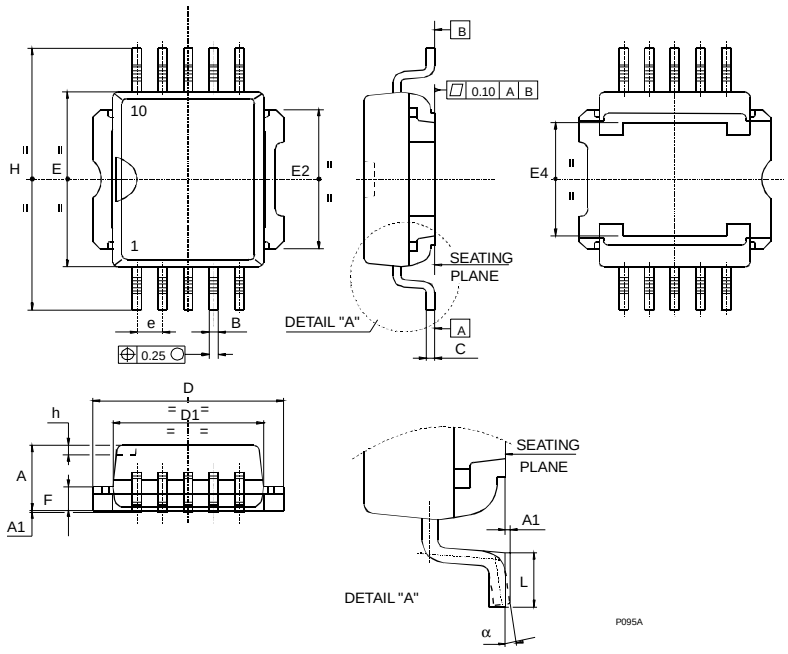
Load disconnection test (IN_A=1, PWM=-2V)



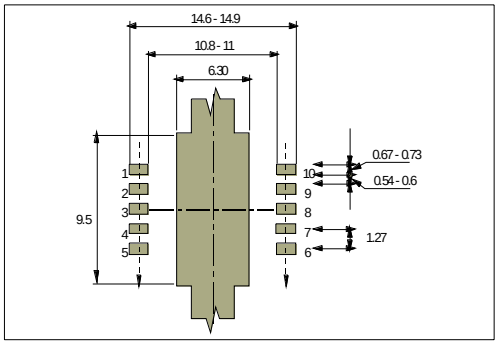
PowerSO-10™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0º		8º	0º		8º
α (*)	2º		8º	2º		8º

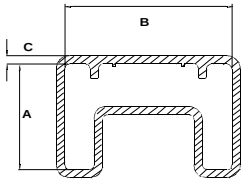
(*) Muar only POA P013P



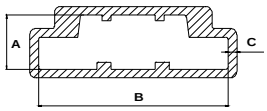
PowerSO-10™ SUGGESTED PAD LAYOUT



TUBE SHIPMENT (no suffix)



CASABLANCA

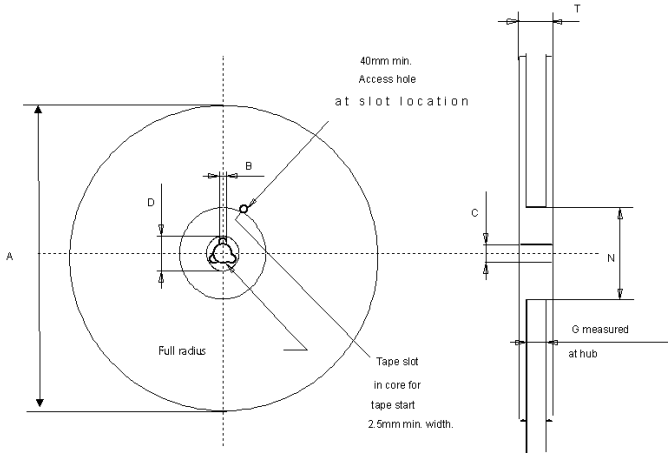


MUAR

All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.