

## 263/256-OUTPUT TFT-LCD GATE DRIVER

**DESCRIPTION**

The  $\mu$  PD16707 is a TFT-LCD gate driver equipped with 263/256-output lines. It can output a high-gate scanning voltage in response to CMOS level input because it provided with a level-shift circuit inside the IC circuit. It can also drive the XGA / SXGA / SXGA+, and since the input signal is placed symmetrically, this product can wire easily between gate drivers.

**FEATURES**

- CMOS level input (2.3 to 3.6V)
- 263/256 outputs
- High-output voltage ( $V_{DD2}$  to  $V_{EE}$  : 40 V MAX.)
- Capable of All-ON outputting (/AOR, /AOL)
- Input terminal symmetrical placement
- Adapted to COG and TCP

**Remark** /xxx indicates active low signal.

**ORDERING INFORMATION**

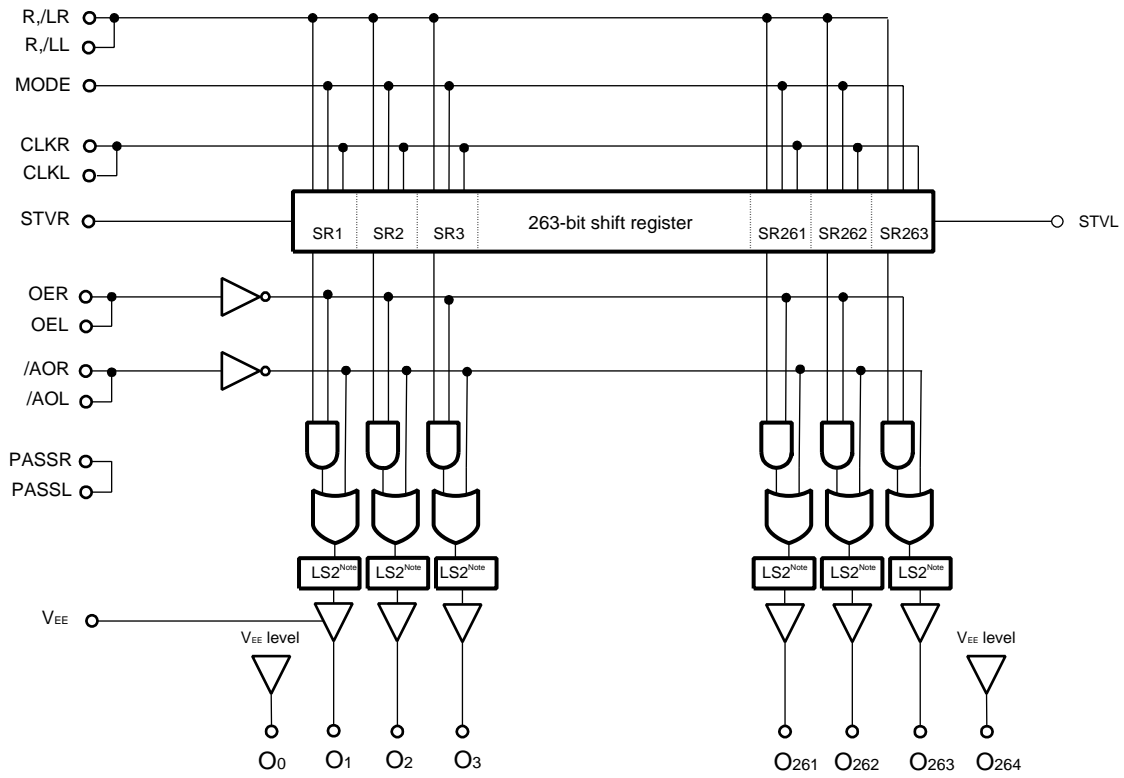
Part Number	Package
$\mu$ PD16707P	CHIP
$\mu$ PD16707N-xxx	TCP (TAB package)

**Remark** Purchasing the above chip entail the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

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1. BLOCK DIAGRAM



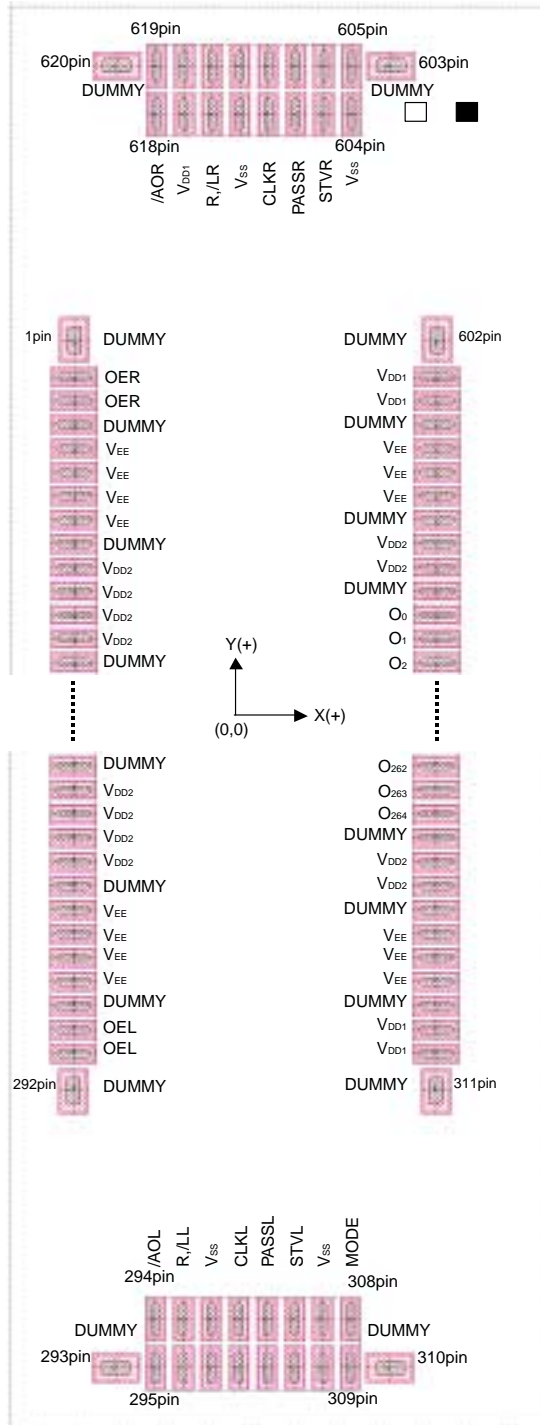
**Note** LS2 : shifts CMOS level and output level ( $V_{DD2}$  to  $V_{EE}$ ).

2. PIN CONFIGURATION

2.1 CHIP PACKAGE : μPD16707P Chip surface (Bump side)

Chip size : 1.06±0.02 x 16.01±0.02 [mm]

Chip thickness : 595±25 [μm]



Alignment Mark1

□ : 50 x 50 μm

coordinate : (267.5, -7785)  
(267.5, 7785)

Alignment Mark2

■ : 50 x 50 μm

coordinate : (387.5, -7785)  
(387.5, 7785)

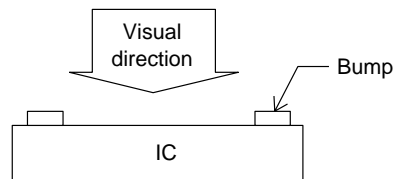


Table 2-1 Pad Coordinate Bump size (1/7)

PAD No.	PAD Name	(X:Y) [μm]		
		X	Y	Bump size
1	DUMMY	-404.0	7303.0	50:87
2	OER	-404.0	7225.0	83:33
3	OER	-404.0	7175.0	83:33
4	DUMMY	-404.0	7125.0	83:33
5	VEE	-404.0	7075.0	83:33
6	VEE	-404.0	7025.0	83:33
7	VEE	-404.0	6975.0	83:33
8	VEE	-404.0	6925.0	83:33
9	DUMMY	-404.0	6875.0	83:33
10	V <sub>DD2</sub>	-404.0	6825.0	83:33
11	V <sub>DD2</sub>	-404.0	6775.0	83:33
12	V <sub>DD2</sub>	-404.0	6725.0	83:33
13	V <sub>DD2</sub>	-404.0	6675.0	83:33
14	DUMMY	-404.0	6625.0	83:33
15	DUMMY	-404.0	6575.0	83:33
16	DUMMY	-404.0	6525.0	83:33
17	DUMMY	-404.0	6475.0	83:33
18	DUMMY	-404.0	6425.0	83:33
19	DUMMY	-404.0	6375.0	83:33
20	DUMMY	-404.0	6325.0	83:33
21	DUMMY	-404.0	6275.0	83:33
22	DUMMY	-404.0	6225.0	83:33
23	DUMMY	-404.0	6175.0	83:33
24	DUMMY	-404.0	6125.0	83:33
25	DUMMY	-404.0	6075.0	83:33
26	DUMMY	-404.0	6025.0	83:33
27	DUMMY	-404.0	5975.0	83:33
28	DUMMY	-404.0	5925.0	83:33
29	DUMMY	-404.0	5875.0	83:33
30	DUMMY	-404.0	5825.0	83:33
31	DUMMY	-404.0	5775.0	83:33
32	DUMMY	-404.0	5725.0	83:33
33	DUMMY	-404.0	5675.0	83:33
34	DUMMY	-404.0	5625.0	83:33
35	DUMMY	-404.0	5575.0	83:33
36	DUMMY	-404.0	5525.0	83:33
37	DUMMY	-404.0	5475.0	83:33
38	DUMMY	-404.0	5425.0	83:33
39	DUMMY	-404.0	5375.0	83:33
40	DUMMY	-404.0	5325.0	83:33
41	DUMMY	-404.0	5275.0	83:33
42	DUMMY	-404.0	5225.0	83:33
43	DUMMY	-404.0	5175.0	83:33
44	DUMMY	-404.0	5125.0	83:33
45	DUMMY	-404.0	5075.0	83:33
46	DUMMY	-404.0	5025.0	83:33
47	DUMMY	-404.0	4975.0	83:33
48	DUMMY	-404.0	4925.0	83:33
49	DUMMY	-404.0	4875.0	83:33
50	DUMMY	-404.0	4825.0	83:33

PAD No.	PAD Name	(X:Y) [μm]		
		X	Y	Bump size
51	DUMMY	-404.0	4775.0	83:33
52	DUMMY	-404.0	4725.0	83:33
53	DUMMY	-404.0	4675.0	83:33
54	DUMMY	-404.0	4625.0	83:33
55	DUMMY	-404.0	4575.0	83:33
56	DUMMY	-404.0	4525.0	83:33
57	DUMMY	-404.0	4475.0	83:33
58	DUMMY	-404.0	4425.0	83:33
59	DUMMY	-404.0	4375.0	83:33
60	DUMMY	-404.0	4325.0	83:33
61	DUMMY	-404.0	4275.0	83:33
62	DUMMY	-404.0	4225.0	83:33
63	DUMMY	-404.0	4175.0	83:33
64	DUMMY	-404.0	4125.0	83:33
65	DUMMY	-404.0	4075.0	83:33
66	DUMMY	-404.0	4025.0	83:33
67	DUMMY	-404.0	3975.0	83:33
68	DUMMY	-404.0	3925.0	83:33
69	DUMMY	-404.0	3875.0	83:33
70	DUMMY	-404.0	3825.0	83:33
71	DUMMY	-404.0	3775.0	83:33
72	DUMMY	-404.0	3725.0	83:33
73	DUMMY	-404.0	3675.0	83:33
74	DUMMY	-404.0	3625.0	83:33
75	DUMMY	-404.0	3575.0	83:33
76	DUMMY	-404.0	3525.0	83:33
77	DUMMY	-404.0	3475.0	83:33
78	DUMMY	-404.0	3425.0	83:33
79	DUMMY	-404.0	3375.0	83:33
80	DUMMY	-404.0	3325.0	83:33
81	DUMMY	-404.0	3275.0	83:33
82	DUMMY	-404.0	3225.0	83:33
83	DUMMY	-404.0	3175.0	83:33
84	DUMMY	-404.0	3125.0	83:33
85	DUMMY	-404.0	3075.0	83:33
86	DUMMY	-404.0	3025.0	83:33
87	DUMMY	-404.0	2975.0	83:33
88	DUMMY	-404.0	2925.0	83:33
89	DUMMY	-404.0	2875.0	83:33
90	DUMMY	-404.0	2825.0	83:33
91	DUMMY	-404.0	2775.0	83:33
92	DUMMY	-404.0	2725.0	83:33
93	DUMMY	-404.0	2675.0	83:33
94	DUMMY	-404.0	2625.0	83:33
95	DUMMY	-404.0	2575.0	83:33
96	DUMMY	-404.0	2525.0	83:33
97	DUMMY	-404.0	2475.0	83:33
98	DUMMY	-404.0	2425.0	83:33
99	DUMMY	-404.0	2375.0	83:33
100	DUMMY	-404.0	2325.0	83:33

Table 2-1 Pad Coordinate Bump size (2/7)

PAD No.	PAD Name	(X:Y) [μm]		
		X	Y	Bump size
101	DUMMY	-404.0	2275.0	83:33
102	DUMMY	-404.0	2225.0	83:33
103	DUMMY	-404.0	2175.0	83:33
104	DUMMY	-404.0	2125.0	83:33
105	DUMMY	-404.0	2075.0	83:33
106	DUMMY	-404.0	2025.0	83:33
107	DUMMY	-404.0	1975.0	83:33
108	DUMMY	-404.0	1925.0	83:33
109	DUMMY	-404.0	1875.0	83:33
110	DUMMY	-404.0	1825.0	83:33
111	DUMMY	-404.0	1775.0	83:33
112	DUMMY	-404.0	1725.0	83:33
113	DUMMY	-404.0	1675.0	83:33
114	DUMMY	-404.0	1625.0	83:33
115	DUMMY	-404.0	1575.0	83:33
116	DUMMY	-404.0	1525.0	83:33
117	DUMMY	-404.0	1475.0	83:33
118	DUMMY	-404.0	1425.0	83:33
119	DUMMY	-404.0	1375.0	83:33
120	DUMMY	-404.0	1325.0	83:33
121	DUMMY	-404.0	1275.0	83:33
122	DUMMY	-404.0	1225.0	83:33
123	DUMMY	-404.0	1175.0	83:33
124	DUMMY	-404.0	1125.0	83:33
125	DUMMY	-404.0	1075.0	83:33
126	DUMMY	-404.0	1025.0	83:33
127	DUMMY	-404.0	975.0	83:33
128	DUMMY	-404.0	925.0	83:33
129	DUMMY	-404.0	875.0	83:33
130	DUMMY	-404.0	825.0	83:33
131	DUMMY	-404.0	775.0	83:33
132	DUMMY	-404.0	725.0	83:33
133	DUMMY	-404.0	675.0	83:33
134	DUMMY	-404.0	625.0	83:33
135	DUMMY	-404.0	575.0	83:33
136	DUMMY	-404.0	525.0	83:33
137	DUMMY	-404.0	475.0	83:33
138	DUMMY	-404.0	425.0	83:33
139	DUMMY	-404.0	375.0	83:33
140	DUMMY	-404.0	325.0	83:33
141	DUMMY	-404.0	275.0	83:33
142	DUMMY	-404.0	225.0	83:33
143	DUMMY	-404.0	175.0	83:33
144	DUMMY	-404.0	125.0	83:33
145	DUMMY	-404.0	75.0	83:33
146	DUMMY	-404.0	25.0	83:33
147	DUMMY	-404.0	-25.0	83:33
148	DUMMY	-404.0	-75.0	83:33
149	DUMMY	-404.0	-125.0	83:33
150	DUMMY	-404.0	-175.0	83:33

PAD No.	PAD Name	(X:Y) [μm]		
		X	Y	Bump size
151	DUMMY	-404.0	-225.0	83:33
152	DUMMY	-404.0	-275.0	83:33
153	DUMMY	-404.0	-325.0	83:33
154	DUMMY	-404.0	-375.0	83:33
155	DUMMY	-404.0	-425.0	83:33
156	DUMMY	-404.0	-475.0	83:33
157	DUMMY	-404.0	-525.0	83:33
158	DUMMY	-404.0	-575.0	83:33
159	DUMMY	-404.0	-625.0	83:33
160	DUMMY	-404.0	-675.0	83:33
161	DUMMY	-404.0	-725.0	83:33
162	DUMMY	-404.0	-775.0	83:33
163	DUMMY	-404.0	-825.0	83:33
164	DUMMY	-404.0	-875.0	83:33
165	DUMMY	-404.0	-925.0	83:33
166	DUMMY	-404.0	-975.0	83:33
167	DUMMY	-404.0	-1025.0	83:33
168	DUMMY	-404.0	-1075.0	83:33
169	DUMMY	-404.0	-1125.0	83:33
170	DUMMY	-404.0	-1175.0	83:33
171	DUMMY	-404.0	-1225.0	83:33
172	DUMMY	-404.0	-1275.0	83:33
173	DUMMY	-404.0	-1325.0	83:33
174	DUMMY	-404.0	-1375.0	83:33
175	DUMMY	-404.0	-1425.0	83:33
176	DUMMY	-404.0	-1475.0	83:33
177	DUMMY	-404.0	-1525.0	83:33
178	DUMMY	-404.0	-1575.0	83:33
179	DUMMY	-404.0	-1625.0	83:33
180	DUMMY	-404.0	-1675.0	83:33
181	DUMMY	-404.0	-1725.0	83:33
182	DUMMY	-404.0	-1775.0	83:33
183	DUMMY	-404.0	-1825.0	83:33
184	DUMMY	-404.0	-1875.0	83:33
185	DUMMY	-404.0	-1925.0	83:33
186	DUMMY	-404.0	-1975.0	83:33
187	DUMMY	-404.0	-2025.0	83:33
188	DUMMY	-404.0	-2075.0	83:33
189	DUMMY	-404.0	-2125.0	83:33
190	DUMMY	-404.0	-2175.0	83:33
191	DUMMY	-404.0	-2225.0	83:33
192	DUMMY	-404.0	-2275.0	83:33
193	DUMMY	-404.0	-2325.0	83:33
194	DUMMY	-404.0	-2375.0	83:33
195	DUMMY	-404.0	-2425.0	83:33
196	DUMMY	-404.0	-2475.0	83:33
197	DUMMY	-404.0	-2525.0	83:33
198	DUMMY	-404.0	-2575.0	83:33
199	DUMMY	-404.0	-2625.0	83:33
200	DUMMY	-404.0	-2675.0	83:33

Table 2-1 Pad Coordinate Bump size (3/7)

PAD No.	PAD Name	(X:Y) [μm]		
		X	Y	Bump size
201	DUMMY	-404.0	-2725.0	83:33
202	DUMMY	-404.0	-2775.0	83:33
203	DUMMY	-404.0	-2825.0	83:33
204	DUMMY	-404.0	-2875.0	83:33
205	DUMMY	-404.0	-2925.0	83:33
206	DUMMY	-404.0	-2975.0	83:33
207	DUMMY	-404.0	-3025.0	83:33
208	DUMMY	-404.0	-3075.0	83:33
209	DUMMY	-404.0	-3125.0	83:33
210	DUMMY	-404.0	-3175.0	83:33
211	DUMMY	-404.0	-3225.0	83:33
212	DUMMY	-404.0	-3275.0	83:33
213	DUMMY	-404.0	-3325.0	83:33
214	DUMMY	-404.0	-3375.0	83:33
215	DUMMY	-404.0	-3425.0	83:33
216	DUMMY	-404.0	-3475.0	83:33
217	DUMMY	-404.0	-3525.0	83:33
218	DUMMY	-404.0	-3575.0	83:33
219	DUMMY	-404.0	-3625.0	83:33
220	DUMMY	-404.0	-3675.0	83:33
221	DUMMY	-404.0	-3725.0	83:33
222	DUMMY	-404.0	-3775.0	83:33
223	DUMMY	-404.0	-3825.0	83:33
224	DUMMY	-404.0	-3875.0	83:33
225	DUMMY	-404.0	-3925.0	83:33
226	DUMMY	-404.0	-3975.0	83:33
227	DUMMY	-404.0	-4025.0	83:33
228	DUMMY	-404.0	-4075.0	83:33
229	DUMMY	-404.0	-4125.0	83:33
230	DUMMY	-404.0	-4175.0	83:33
231	DUMMY	-404.0	-4225.0	83:33
232	DUMMY	-404.0	-4275.0	83:33
233	DUMMY	-404.0	-4325.0	83:33
234	DUMMY	-404.0	-4375.0	83:33
235	DUMMY	-404.0	-4425.0	83:33
236	DUMMY	-404.0	-4475.0	83:33
237	DUMMY	-404.0	-4525.0	83:33
238	DUMMY	-404.0	-4575.0	83:33
239	DUMMY	-404.0	-4625.0	83:33
240	DUMMY	-404.0	-4675.0	83:33
241	DUMMY	-404.0	-4725.0	83:33
242	DUMMY	-404.0	-4775.0	83:33
243	DUMMY	-404.0	-4825.0	83:33
244	DUMMY	-404.0	-4875.0	83:33
245	DUMMY	-404.0	-4925.0	83:33
246	DUMMY	-404.0	-4975.0	83:33
247	DUMMY	-404.0	-5025.0	83:33
248	DUMMY	-404.0	-5075.0	83:33
249	DUMMY	-404.0	-5125.0	83:33
250	DUMMY	-404.0	-5175.0	83:33

PAD No.	PAD Name	(X:Y) [μm]		
		X	Y	Bump size
251	DUMMY	-404.0	-5225.0	83:33
252	DUMMY	-404.0	-5275.0	83:33
253	DUMMY	-404.0	-5325.0	83:33
254	DUMMY	-404.0	-5375.0	83:33
255	DUMMY	-404.0	-5425.0	83:33
256	DUMMY	-404.0	-5475.0	83:33
257	DUMMY	-404.0	-5525.0	83:33
258	DUMMY	-404.0	-5575.0	83:33
259	DUMMY	-404.0	-5625.0	83:33
260	DUMMY	-404.0	-5675.0	83:33
261	DUMMY	-404.0	-5725.0	83:33
262	DUMMY	-404.0	-5775.0	83:33
263	DUMMY	-404.0	-5825.0	83:33
264	DUMMY	-404.0	-5875.0	83:33
265	DUMMY	-404.0	-5925.0	83:33
266	DUMMY	-404.0	-5975.0	83:33
267	DUMMY	-404.0	-6025.0	83:33
268	DUMMY	-404.0	-6075.0	83:33
269	DUMMY	-404.0	-6125.0	83:33
270	DUMMY	-404.0	-6175.0	83:33
271	DUMMY	-404.0	-6225.0	83:33
272	DUMMY	-404.0	-6275.0	83:33
273	DUMMY	-404.0	-6325.0	83:33
274	DUMMY	-404.0	-6375.0	83:33
275	DUMMY	-404.0	-6425.0	83:33
276	DUMMY	-404.0	-6475.0	83:33
277	DUMMY	-404.0	-6525.0	83:33
278	DUMMY	-404.0	-6575.0	83:33
279	DUMMY	-404.0	-6625.0	83:33
280	VDD2	-404.0	-6675.0	83:33
281	VDD2	-404.0	-6725.0	83:33
282	VDD2	-404.0	-6775.0	83:33
283	VDD2	-404.0	-6825.0	83:33
284	DUMMY	-404.0	-6875.0	83:33
285	VEE	-404.0	-6925.0	83:33
286	VEE	-404.0	-6975.0	83:33
287	VEE	-404.0	-7025.0	83:33
288	VEE	-404.0	-7075.0	83:33
289	DUMMY	-404.0	-7125.0	83:33
290	OEL	-404.0	-7175.0	83:33
291	OEL	-404.0	-7225.0	83:33
292	DUMMY	-404.0	-7303.0	50:87
293	DUMMY	-320.0	-7879.0	87:50
294	/AOL	-242.0	-7778.0	33:83
295	/AOL	-242.0	-7879.0	33:83
296	R,/LL	-187.0	-7778.0	33:83
297	R,/LL	-187.0	-7879.0	33:83
298	VSS	-132.0	-7778.0	33:83
299	VSS	-132.0	-7879.0	33:83
300	CLKL	-77.0	-7778.0	33:83

Table 2-1 Pad Coordinate Bump size (4/7)

(X:Y) [μm]				
PAD No.	PAD Name	X	Y	Bump size
301	CLKL	-77.0	-7879.0	33:83
302	PASSL	-22.0	-7778.0	33:83
303	PASSL	-22.0	-7879.0	33:83
304	STVL	33.0	-7778.0	33:83
305	STVL	33.0	-7879.0	33:83
306	VSS	88.0	-7778.0	33:83
307	VSS	88.0	-7879.0	33:83
308	MODE	143.0	-7778.0	33:83
309	MODE	143.0	-7879.0	33:83
310	DUMMY	221.0	-7879.0	87:50
311	DUMMY	312.0	-7303.0	50:87
312	VDD1	312.0	-7225.0	83:33
313	VDD1	312.0	-7175.0	83:33
314	DUMMY	312.0	-7125.0	83:33
315	VEE	312.0	-7075.0	83:33
316	VEE	312.0	-7025.0	83:33
317	VEE	312.0	-6975.0	83:33
318	DUMMY	312.0	-6925.0	83:33
319	VDD2	312.0	-6875.0	83:33
320	VDD2	312.0	-6825.0	83:33
321	DUMMY	312.0	-6775.0	83:33
322	O264	312.0	-6725.0	83:33
323	O263	312.0	-6675.0	83:33
324	O262	312.0	-6625.0	83:33
325	O261	312.0	-6575.0	83:33
326	O260	312.0	-6525.0	83:33
327	O259	312.0	-6475.0	83:33
328	O258	312.0	-6425.0	83:33
329	O257	312.0	-6375.0	83:33
330	O256	312.0	-6325.0	83:33
331	O255	312.0	-6275.0	83:33
332	O254	312.0	-6225.0	83:33
333	O253	312.0	-6175.0	83:33
334	O252	312.0	-6125.0	83:33
335	O251	312.0	-6075.0	83:33
336	O250	312.0	-6025.0	83:33
337	O249	312.0	-5975.0	83:33
338	O248	312.0	-5925.0	83:33
339	O247	312.0	-5875.0	83:33
340	O246	312.0	-5825.0	83:33
341	O245	312.0	-5775.0	83:33
342	O244	312.0	-5725.0	83:33
343	O243	312.0	-5675.0	83:33
344	O242	312.0	-5625.0	83:33
345	O241	312.0	-5575.0	83:33
346	O240	312.0	-5525.0	83:33
347	O239	312.0	-5475.0	83:33
348	O238	312.0	-5425.0	83:33
349	O237	312.0	-5375.0	83:33
350	O236	312.0	-5325.0	83:33

(X:Y) [μm]				
PAD No.	PAD Name	X	Y	Bump size
351	O235	312.0	-5275.0	83:33
352	O234	312.0	-5225.0	83:33
353	O233	312.0	-5175.0	83:33
354	O232	312.0	-5125.0	83:33
355	O231	312.0	-5075.0	83:33
356	O230	312.0	-5025.0	83:33
357	O229	312.0	-4975.0	83:33
358	O228	312.0	-4925.0	83:33
359	O227	312.0	-4875.0	83:33
360	O226	312.0	-4825.0	83:33
361	O225	312.0	-4775.0	83:33
362	O224	312.0	-4725.0	83:33
363	O223	312.0	-4675.0	83:33
364	O222	312.0	-4625.0	83:33
365	O221	312.0	-4575.0	83:33
366	O220	312.0	-4525.0	83:33
367	O219	312.0	-4475.0	83:33
368	O218	312.0	-4425.0	83:33
369	O217	312.0	-4375.0	83:33
370	O216	312.0	-4325.0	83:33
371	O215	312.0	-4275.0	83:33
372	O214	312.0	-4225.0	83:33
373	O213	312.0	-4175.0	83:33
374	O212	312.0	-4125.0	83:33
375	O211	312.0	-4075.0	83:33
376	O210	312.0	-4025.0	83:33
377	O209	312.0	-3975.0	83:33
378	O208	312.0	-3925.0	83:33
379	O207	312.0	-3875.0	83:33
380	O206	312.0	-3825.0	83:33
381	O205	312.0	-3775.0	83:33
382	O204	312.0	-3725.0	83:33
383	O203	312.0	-3675.0	83:33
384	O202	312.0	-3625.0	83:33
385	O201	312.0	-3575.0	83:33
386	O200	312.0	-3525.0	83:33
387	O199	312.0	-3475.0	83:33
388	O198	312.0	-3425.0	83:33
389	O197	312.0	-3375.0	83:33
390	O196	312.0	-3325.0	83:33
391	O195	312.0	-3275.0	83:33
392	O194	312.0	-3225.0	83:33
393	O193	312.0	-3175.0	83:33
394	O192	312.0	-3125.0	83:33
395	O191	312.0	-3075.0	83:33
396	O190	312.0	-3025.0	83:33
397	O189	312.0	-2975.0	83:33
398	O188	312.0	-2925.0	83:33
399	O187	312.0	-2875.0	83:33
400	O186	312.0	-2825.0	83:33

Table 2-1 Pad Coordinate Bump size (5/7)

PAD No.	PAD Name	(X:Y) [μm]		Bump size
		X	Y	
401	O185	312.0	-2775.0	83:33
402	O184	312.0	-2725.0	83:33
403	O183	312.0	-2675.0	83:33
404	O182	312.0	-2625.0	83:33
405	O181	312.0	-2575.0	83:33
406	O180	312.0	-2525.0	83:33
407	O179	312.0	-2475.0	83:33
408	O178	312.0	-2425.0	83:33
409	O177	312.0	-2375.0	83:33
410	O176	312.0	-2325.0	83:33
411	O175	312.0	-2275.0	83:33
412	O174	312.0	-2225.0	83:33
413	O173	312.0	-2175.0	83:33
414	O172	312.0	-2125.0	83:33
415	O171	312.0	-2075.0	83:33
416	O170	312.0	-2025.0	83:33
417	O169	312.0	-1975.0	83:33
418	O168	312.0	-1925.0	83:33
419	O167	312.0	-1875.0	83:33
420	O166	312.0	-1825.0	83:33
421	O165	312.0	-1775.0	83:33
422	O164	312.0	-1725.0	83:33
423	O163	312.0	-1675.0	83:33
424	O162	312.0	-1625.0	83:33
425	O161	312.0	-1575.0	83:33
426	O160	312.0	-1525.0	83:33
427	O159	312.0	-1475.0	83:33
428	O158	312.0	-1425.0	83:33
429	O157	312.0	-1375.0	83:33
430	O156	312.0	-1325.0	83:33
431	O155	312.0	-1275.0	83:33
432	O154	312.0	-1225.0	83:33
433	O153	312.0	-1175.0	83:33
434	O152	312.0	-1125.0	83:33
435	O151	312.0	-1075.0	83:33
436	O150	312.0	-1025.0	83:33
437	O149	312.0	-975.0	83:33
438	O148	312.0	-925.0	83:33
439	O147	312.0	-875.0	83:33
440	O146	312.0	-825.0	83:33
441	O145	312.0	-775.0	83:33
442	O144	312.0	-725.0	83:33
443	O143	312.0	-675.0	83:33
444	O142	312.0	-625.0	83:33
445	O141	312.0	-575.0	83:33
446	O140	312.0	-525.0	83:33
447	O139	312.0	-475.0	83:33
448	O138	312.0	-425.0	83:33
449	O137	312.0	-375.0	83:33
450	O136	312.0	-325.0	83:33

PAD No.	PAD Name	(X:Y) [μm]		Bump size
		X	Y	
451	O135	312.0	-275.0	83:33
452	O134	312.0	-225.0	83:33
453	O133	312.0	-175.0	83:33
454	O132	312.0	-125.0	83:33
455	DUMMY	312.0	-75.0	83:33
456	DUMMY	312.0	-25.0	83:33
457	DUMMY	312.0	25.0	83:33
458	DUMMY	312.0	75.0	83:33
459	DUMMY	312.0	125.0	83:33
460	O131	312.0	175.0	83:33
461	O130	312.0	225.0	83:33
462	O129	312.0	275.0	83:33
463	O128	312.0	325.0	83:33
464	O127	312.0	375.0	83:33
465	O126	312.0	425.0	83:33
466	O125	312.0	475.0	83:33
467	O124	312.0	525.0	83:33
468	O123	312.0	575.0	83:33
469	O122	312.0	625.0	83:33
470	O121	312.0	675.0	83:33
471	O120	312.0	725.0	83:33
472	O119	312.0	775.0	83:33
473	O118	312.0	825.0	83:33
474	O117	312.0	875.0	83:33
475	O116	312.0	925.0	83:33
476	O115	312.0	975.0	83:33
477	O114	312.0	1025.0	83:33
478	O113	312.0	1075.0	83:33
479	O112	312.0	1125.0	83:33
480	O111	312.0	1175.0	83:33
481	O110	312.0	1225.0	83:33
482	O109	312.0	1275.0	83:33
483	O108	312.0	1325.0	83:33
484	O107	312.0	1375.0	83:33
485	O106	312.0	1425.0	83:33
486	O105	312.0	1475.0	83:33
487	O104	312.0	1525.0	83:33
488	O103	312.0	1575.0	83:33
489	O102	312.0	1625.0	83:33
490	O101	312.0	1675.0	83:33
491	O100	312.0	1725.0	83:33
492	O99	312.0	1775.0	83:33
493	O98	312.0	1825.0	83:33
494	O97	312.0	1875.0	83:33
495	O96	312.0	1925.0	83:33
496	O95	312.0	1975.0	83:33
497	O94	312.0	2025.0	83:33
498	O93	312.0	2075.0	83:33
499	O92	312.0	2125.0	83:33
500	O91	312.0	2175.0	83:33



Table 2-1 Pad Coordinate Bump size (6/7)

PAD No.	PAD Name	(X:Y) [μm]		
		X	Y	Bump size
501	O <sub>90</sub>	312.0	2225.0	83:33
502	O <sub>89</sub>	312.0	2275.0	83:33
503	O <sub>88</sub>	312.0	2325.0	83:33
504	O <sub>87</sub>	312.0	2375.0	83:33
505	O <sub>86</sub>	312.0	2425.0	83:33
506	O <sub>85</sub>	312.0	2475.0	83:33
507	O <sub>84</sub>	312.0	2525.0	83:33
508	O <sub>83</sub>	312.0	2575.0	83:33
509	O <sub>82</sub>	312.0	2625.0	83:33
510	O <sub>81</sub>	312.0	2675.0	83:33
511	O <sub>80</sub>	312.0	2725.0	83:33
512	O <sub>79</sub>	312.0	2775.0	83:33
513	O <sub>78</sub>	312.0	2825.0	83:33
514	O <sub>77</sub>	312.0	2875.0	83:33
515	O <sub>76</sub>	312.0	2925.0	83:33
516	O <sub>75</sub>	312.0	2975.0	83:33
517	O <sub>74</sub>	312.0	3025.0	83:33
518	O <sub>73</sub>	312.0	3075.0	83:33
519	O <sub>72</sub>	312.0	3125.0	83:33
520	O <sub>71</sub>	312.0	3175.0	83:33
521	O <sub>70</sub>	312.0	3225.0	83:33
522	O <sub>69</sub>	312.0	3275.0	83:33
523	O <sub>68</sub>	312.0	3325.0	83:33
524	O <sub>67</sub>	312.0	3375.0	83:33
525	O <sub>66</sub>	312.0	3425.0	83:33
526	O <sub>65</sub>	312.0	3475.0	83:33
527	O <sub>64</sub>	312.0	3525.0	83:33
528	O <sub>63</sub>	312.0	3575.0	83:33
529	O <sub>62</sub>	312.0	3625.0	83:33
530	O <sub>61</sub>	312.0	3675.0	83:33
531	O <sub>60</sub>	312.0	3725.0	83:33
532	O <sub>59</sub>	312.0	3775.0	83:33
533	O <sub>58</sub>	312.0	3825.0	83:33
534	O <sub>57</sub>	312.0	3875.0	83:33
535	O <sub>56</sub>	312.0	3925.0	83:33
536	O <sub>55</sub>	312.0	3975.0	83:33
537	O <sub>54</sub>	312.0	4025.0	83:33
538	O <sub>53</sub>	312.0	4075.0	83:33
539	O <sub>52</sub>	312.0	4125.0	83:33
540	O <sub>51</sub>	312.0	4175.0	83:33
541	O <sub>50</sub>	312.0	4225.0	83:33
542	O <sub>49</sub>	312.0	4275.0	83:33
543	O <sub>48</sub>	312.0	4325.0	83:33
544	O <sub>47</sub>	312.0	4375.0	83:33
545	O <sub>46</sub>	312.0	4425.0	83:33
546	O <sub>45</sub>	312.0	4475.0	83:33
547	O <sub>44</sub>	312.0	4525.0	83:33
548	O <sub>43</sub>	312.0	4575.0	83:33
549	O <sub>42</sub>	312.0	4625.0	83:33
550	O <sub>41</sub>	312.0	4675.0	83:33

PAD No.	PAD Name	(X:Y) [μm]		
		X	Y	Bump size
551	O <sub>40</sub>	312.0	4725.0	83:33
552	O <sub>39</sub>	312.0	4775.0	83:33
553	O <sub>38</sub>	312.0	4825.0	83:33
554	O <sub>37</sub>	312.0	4875.0	83:33
555	O <sub>36</sub>	312.0	4925.0	83:33
556	O <sub>35</sub>	312.0	4975.0	83:33
557	O <sub>34</sub>	312.0	5025.0	83:33
558	O <sub>33</sub>	312.0	5075.0	83:33
559	O <sub>32</sub>	312.0	5125.0	83:33
560	O <sub>31</sub>	312.0	5175.0	83:33
561	O <sub>30</sub>	312.0	5225.0	83:33
562	O <sub>29</sub>	312.0	5275.0	83:33
563	O <sub>28</sub>	312.0	5325.0	83:33
564	O <sub>27</sub>	312.0	5375.0	83:33
565	O <sub>26</sub>	312.0	5425.0	83:33
566	O <sub>25</sub>	312.0	5475.0	83:33
567	O <sub>24</sub>	312.0	5525.0	83:33
568	O <sub>23</sub>	312.0	5575.0	83:33
569	O <sub>22</sub>	312.0	5625.0	83:33
570	O <sub>21</sub>	312.0	5675.0	83:33
571	O <sub>20</sub>	312.0	5725.0	83:33
572	O <sub>19</sub>	312.0	5775.0	83:33
573	O <sub>18</sub>	312.0	5825.0	83:33
574	O <sub>17</sub>	312.0	5875.0	83:33
575	O <sub>16</sub>	312.0	5925.0	83:33
576	O <sub>15</sub>	312.0	5975.0	83:33
577	O <sub>14</sub>	312.0	6025.0	83:33
578	O <sub>13</sub>	312.0	6075.0	83:33
579	O <sub>12</sub>	312.0	6125.0	83:33
580	O <sub>11</sub>	312.0	6175.0	83:33
581	O <sub>10</sub>	312.0	6225.0	83:33
582	O <sub>9</sub>	312.0	6275.0	83:33
583	O <sub>8</sub>	312.0	6325.0	83:33
584	O <sub>7</sub>	312.0	6375.0	83:33
585	O <sub>6</sub>	312.0	6425.0	83:33
586	O <sub>5</sub>	312.0	6475.0	83:33
587	O <sub>4</sub>	312.0	6525.0	83:33
588	O <sub>3</sub>	312.0	6575.0	83:33
589	O <sub>2</sub>	312.0	6625.0	83:33
590	O <sub>1</sub>	312.0	6675.0	83:33
591	O <sub>0</sub>	312.0	6725.0	83:33
592	DUMMY	312.0	6775.0	83:33
593	V <sub>DD2</sub>	312.0	6825.0	83:33
594	V <sub>DD2</sub>	312.0	6875.0	83:33
595	DUMMY	312.0	6925.0	83:33
596	V <sub>EE</sub>	312.0	6975.0	83:33
597	V <sub>EE</sub>	312.0	7025.0	83:33
598	V <sub>EE</sub>	312.0	7075.0	83:33
599	DUMMY	312.0	7125.0	83:33
600	V <sub>DD1</sub>	312.0	7175.0	83:33

Table 2-1 Pad Coordinate Bump size (7/7)

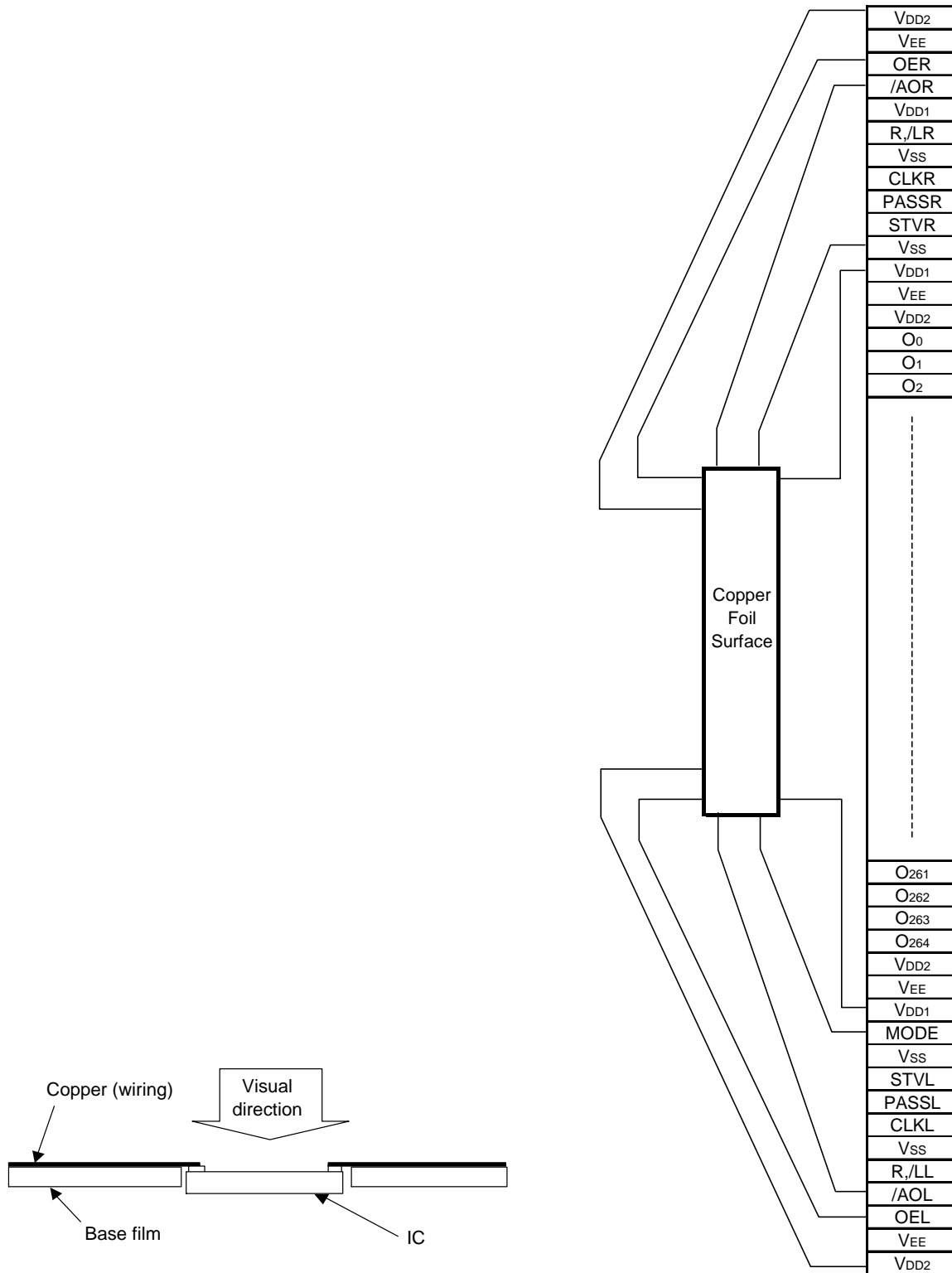
(X:Y) [ $\mu$ m]

PAD No.	PAD Name	X	Y	Bump size
601	V <sub>DD1</sub>	312.0	7225.0	83:33
602	DUMMY	312.0	7303.0	50:87
603	DUMMY	221.0	7879.0	87:50
604	V <sub>SS</sub>	143.0	7778.0	33:83
605	V <sub>SS</sub>	143.0	7879.0	33:83
606	STVR	88.0	7778.0	33:83
607	STVR	88.0	7879.0	33:83
608	PASSR	33.0	7778.0	33:83
609	PASSR	33.0	7879.0	33:83
610	CLKR	-22.0	7778.0	33:83
611	CLKR	-22.0	7879.0	33:83
612	V <sub>SS</sub>	-77.0	7778.0	33:83
613	V <sub>SS</sub>	-77.0	7879.0	33:83
614	R,/LR	-132.0	7778.0	33:83
615	R,/LR	-132.0	7879.0	33:83
616	V <sub>DD1</sub>	-187.0	7778.0	33:83
617	V <sub>DD1</sub>	-187.0	7879.0	33:83
618	/AOR	-242.0	7778.0	33:83
619	/AOR	-242.0	7879.0	33:83
620	DUMMY	-320.0	7879.0	87:50

**Bump Specs (Standard reference value)**

Parameter	Specifications
Bump size tolerance	$\pm 5 \mu\text{m}$
Bump height (design center value)	$15 \mu\text{m}$
Bump height tolerance (within lot)	$\pm 4 \mu\text{m}$
Bump height tolerance (within chip)	Range : $3 \mu\text{m}$
Bump hardness	$50 \pm 20 \text{ Hv}$

2.2 PIN CONFIGURATION : μPD16707N-xxx (Copper foil surface, face-up)



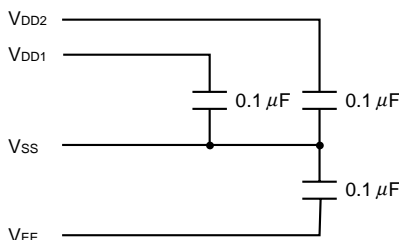
**Remark** This figure does not specify the TCP package.

3. PIN FUNCTIONS

Pin Symbol	Pin Name	I/O	Description
O <sub>1</sub> to O <sub>263</sub>	Driver output	Output	These pins output scan signals that drive the vertical direction (gate lines) of a TFT-LCD. The output signals change in synchronization with the rising edge of shift clock CLK. The driver output amplitude is V <sub>DD2</sub> to V <sub>EE</sub> .
O <sub>0</sub> , O <sub>264</sub>	Driver output	Output	The signal of V <sub>EE</sub> level is outputted by fixation.
R,/LR, R,/LL	Shift direction control	Input	The shift direction control pin of shift register. The shift directions of shift register are as follows. R,/LR, R,/LL = H : right shift : STVR → O <sub>1</sub> → O <sub>263</sub> → STVL R,/LR, R,/LL = L : left shift : STVL → O <sub>263</sub> → O <sub>1</sub> → STVR R,/LR and R,/LL are connected inside IC.
STVR, STVL	Start pulse input/output	I/O	This is the I/O of the internal shift register. The start pulse is read at the rising edge of shift clock CLK (CLKR,CLKL), and scan signals are output from the driver output pins. The input level is a V <sub>DD1</sub> to V <sub>SS</sub> (logic level). When in MODE = H, the start pulse is output at the falling edge of the 263rd clock of shift clock CLK, and is cleared at the falling edge of the 264th clock. The output level is V <sub>DD1</sub> to V <sub>SS</sub> (logic level).
CLKR, CLKL	Shift clock input	Input	This pin inputs a shift clock to the internal shift register. The shift operation is performed in synchronization with the rising edge of this input. CLKR and CLKL are connected inside IC.
OER,OEL	Output enable input	Input	When this pin goes high level, the driver output is fixed to V <sub>EE</sub> level. The shift register is not cleared. CLK is asynchronous in the clock. OER and OEL are connected inside IC.
/AOR, /AOL	All-on control	Input	When this pin goes low level, all driver output = V <sub>DD2</sub> level. The shift register is not cleared. This pin has priority over OER,OEL. This pin is pulled up to V <sub>DD1</sub> power supply inside IC. CLK is asynchronous in the clock. /AOR and /AOL are connected inside IC.
MODE	Selection of Number of outputs	Input	MODE = V <sub>DD1</sub> or open: 263 outputs MODE = V <sub>SS</sub> : 256 outputs (Driver pins O <sub>129</sub> to O <sub>135</sub> are invalid.) Input level is V <sub>DD1</sub> to V <sub>SS</sub> (logic level) This pin is pulled up to V <sub>DD1</sub> power supply inside IC.
PASSR, PASSL	Pass line	Input	PASSR and PASSL are connected inside IC.
V <sub>DD1</sub>	Logic power supply	–	2.3 to 3.6 V
V <sub>DD2</sub>	Driver positive power supply	–	15 to 25 V. The driver output: high level
V <sub>SS</sub>	Logic ground	–	Connect this pin to the ground of the system.
V <sub>EE</sub>	Negative Power supply for internal operation	–	–15 to –5 V. The driver output: low level
DUMMY <sup>Note</sup>	Dummy	–	No dummy pins are connected with other pins inside IC.

**Note** DUMMY pins are adapted only for chip product. (There is no DUMMY pin in TCP product.)

- Cautions**
1. To prevent latch-up, turn on power to V<sub>DD1</sub> → logic input → V<sub>EE</sub> → V<sub>DD2</sub> in this order. Turn off power in the reverse order. These power up/down sequence must be observed also during transition period.
  2. Insert a capacitor of about 0.1 μF between each power line, as shown below, to secure noise margin such as V<sub>IH</sub> and V<sub>IL</sub>.

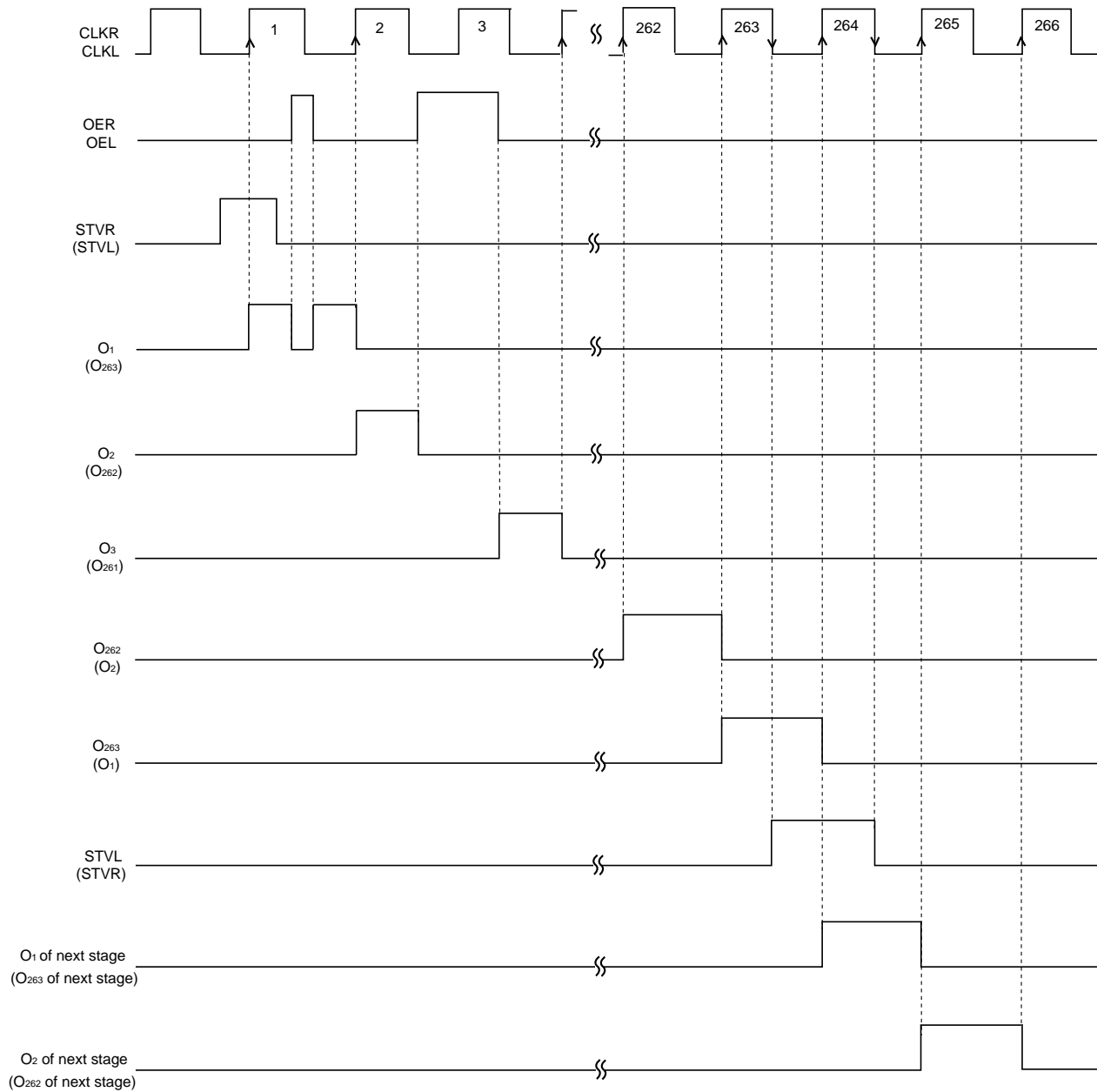


4. RELATIONS OF ENABLE INPUT AND OUTPUT TERMINAL

Switching is possible for 263/256 with μ PD16707 by the MODE pin.

MODE = H or open	MODE = L
263 out Mode	256 out Mode
O <sub>1</sub>	O <sub>1</sub>
O <sub>2</sub>	O <sub>2</sub>
O <sub>3</sub>	O <sub>3</sub>
O <sub>4</sub>	O <sub>4</sub>
O <sub>5</sub>	O <sub>5</sub>
O <sub>6</sub>	O <sub>6</sub>
↓	↓
O <sub>127</sub>	O <sub>127</sub>
O <sub>128</sub>	O <sub>128</sub>
O <sub>129</sub>	V <sub>OUT</sub> = V <sub>EE</sub>
O <sub>130</sub>	V <sub>OUT</sub> = V <sub>EE</sub>
O <sub>131</sub>	V <sub>OUT</sub> = V <sub>EE</sub>
O <sub>132</sub>	V <sub>OUT</sub> = V <sub>EE</sub>
O <sub>133</sub>	V <sub>OUT</sub> = V <sub>EE</sub>
O <sub>134</sub>	V <sub>OUT</sub> = V <sub>EE</sub>
O <sub>135</sub>	V <sub>OUT</sub> = V <sub>EE</sub>
O <sub>136</sub>	O <sub>136</sub>
O <sub>137</sub>	O <sub>137</sub>
↓	↓
O <sub>259</sub>	O <sub>259</sub>
O <sub>260</sub>	O <sub>260</sub>
O <sub>261</sub>	O <sub>261</sub>
O <sub>262</sub>	O <sub>262</sub>
O <sub>263</sub>	O <sub>263</sub>

5. TIMING CHART (R,/LR = R,/LL = H, MODE = H, /AOR = /AOL = H)



**Remark** The signal name in parenthesis is it at the time of R,/LR = R,/LL = L.

6. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings (T<sub>A</sub> = 25°C, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V <sub>DD1</sub>	-0.5 to +7.0	V
Driver Positive Supply Voltage	V <sub>DD2</sub>	-0.5 to +28	V
Power Supply Voltage	V <sub>DD2-V<sub>EE</sub></sub>	-0.5 to +42	V
Internal Operation Negative Supply Voltage	V <sub>EE</sub>	-16 to + 0.5	V
Input Voltage	V <sub>I</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Operating Ambient Temperature	T <sub>A</sub>	-20 to +75	°C
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C

**Caution** Product qualify may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Recommended Operating Range (T<sub>A</sub> = -20 to +75°C, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V <sub>DD1</sub>	2.3	3.0	3.6	V
Driver Positive Supply Voltage	V <sub>DD2</sub>	15	23	25	V
Internal Operation Negative Supply Voltage	V <sub>EE</sub>	-15	-10	-5.0	V
Power Supply Voltage	V <sub>DD2-V<sub>EE</sub></sub>	20	33	40	V
Clock Frequency	f <sub>CLK</sub>			500	kHz

**Electrical Characteristics (T<sub>A</sub> = -20 to +75°C, V<sub>DD1</sub> = 2.3V to 3.6V, V<sub>DD2</sub> = 23 V, V<sub>EE</sub> = -10 V, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP. <sup>Note</sup>	MAX.	Unit
High level Input Voltage	V <sub>IH</sub>	CLKR, CLKL, STVR, STVL,	0.8 V <sub>DD1</sub>		V <sub>DD1</sub>	V
Low level Input Voltage	V <sub>IL</sub>	R <sub>1</sub> /LR, R <sub>2</sub> /LL, OER, OEL, MODE	V <sub>SS</sub>		0.2 V <sub>DD1</sub>	V
High level Output Voltage	V <sub>OH</sub>	STVR (STVL), I <sub>OH</sub> = -40 μA	V <sub>DD1</sub> - 0.4		V <sub>DD1</sub>	V
Low level Output Voltage	V <sub>OL</sub>	STVR (STVL), I <sub>OL</sub> = +40 μA	V <sub>SS</sub>		V <sub>SS</sub> + 0.4	V
LCD Driver Output ON Resistance	R <sub>ON</sub>	V <sub>OUT</sub> = V <sub>EE</sub> + 1.0 V or V <sub>DD2</sub> - 1.0 V		0.3	1.0	kΩ
Pull-up Resistance	R <sub>PU</sub>	V <sub>DD1</sub> = 3.0 V, /AOR, /AOL, MODE	10	50	100	kΩ
Input Leak Current	I <sub>IL</sub>	V <sub>I</sub> = 0 V or 3.6 V, except for /AOR, /AOL, MODE			±1.0	μA
Static Current Dissipation	I <sub>DD1</sub>	V <sub>DD1</sub> , f <sub>CLK</sub> = 50 kHz, OER = OEL = L, f <sub>STV</sub> = 60 Hz, no load		20	200	μA
	I <sub>DD2</sub>	V <sub>DD2</sub> , f <sub>CLK</sub> = 50 kHz, OER = OEL = L, f <sub>STV</sub> = 60 Hz, no load		10	100	μA
	I <sub>EE</sub>	V <sub>EE</sub> , f <sub>CLK</sub> = 50 kHz, OER = OEL = L, f <sub>STV</sub> = 60 Hz, no load	-300	-30		μA

**Remark** STV : STVR (STVL)

**Note** The TYP.value refers to the measured values in V<sub>DD1</sub> = 3.0 V, T<sub>A</sub> = 25°C.



**Switching Characteristics (T<sub>A</sub> = -20 to +75°C, V<sub>DD1</sub> = 2.3V to 3.6V, V<sub>DD2</sub> = 23 V, V<sub>EE</sub> = -10 V, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cascade Output Delay Time	t <sub>PHL1</sub>	C <sub>L</sub> = 55 pF,			500	ns
	t <sub>PLH1</sub>	CLKR (CLKL) → STVL (STVR)			500	ns
Driver Output Delay Time	t <sub>PHL2</sub>	C <sub>L</sub> = 300 pF,			500	ns
	t <sub>PLH2</sub>	CLKR (CLKL) → O <sub>n</sub>			500	ns
	t <sub>PHL3</sub>	C <sub>L</sub> = 300 pF,			500	ns
	t <sub>PLH3</sub>	OER (OEL) → O <sub>n</sub>			500	ns
Output Rise Time	t <sub>TLH</sub>	C <sub>L</sub> = 300 pF			800	ns
Output Fall Time	t <sub>THL</sub>				800	ns
Input Capacitance	C <sub>i</sub>	T <sub>A</sub> = 25°C			50	pF

**Timing Requirements (T<sub>A</sub> = -20 to +75°C, V<sub>DD1</sub> = 2.3 to 3.6 V, V<sub>DD2</sub> = 23 V, V<sub>EE</sub> = -10 V, V<sub>SS</sub> = 0 V)**

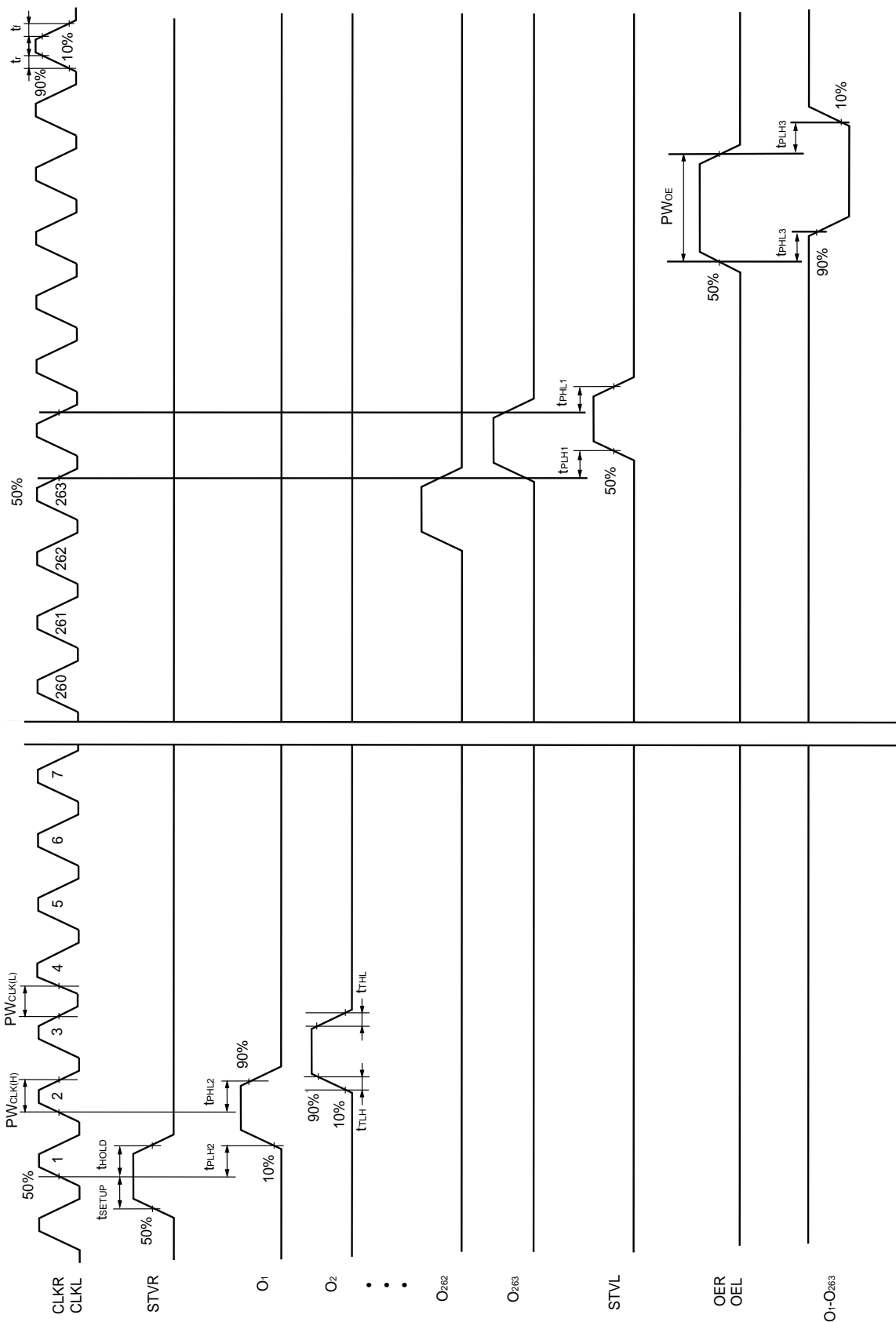
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse High Width	PW <sub>CLK(H)</sub>		500			ns
Clock Pulse Low Width	PW <sub>CLK(L)</sub>		500			ns
Enable Pulse Width	PW <sub>OE</sub>		1000			ns
Data Setup Time	t <sub>SETUP</sub>	STVR (STVL) ↑ → CLKR, CLKL ↑	200			ns
Data Hold Time	t <sub>HOLD</sub>	CLKR, CLKL ↑ → STVR (STVL) ↓	200			ns

**Remark** Unless otherwise specified, the input level is defined to be V<sub>IH</sub> = V<sub>IL</sub> = 0.5 V<sub>DD1</sub>.

**Caution** Keep the time and fall time of the logic input to t<sub>r</sub> = t<sub>f</sub> = 20 ns (10 to 90% of the rated values).

**SWITCHING CHARACTERISTICS WAVEFORM (R,/LR = R,/LL = H, MODE = H)**

Unless otherwise specified, the input level is defined to be  $V_{IH} = V_{IL} = 0.5 V_{DD1}$ .



**7. RECOMMENDED MOUNTING CONDITIONS**

The μPD16707 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Recommended Soldering Conditions for Surface Mounting Soldering Conditions.

**μPD16707N-xxx: TCP (TAB Package)**

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds : pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm <sup>2</sup> : time 3 to 5 sec. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm <sup>2</sup> : time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

**Caution** To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**Reference Documents****NEC Semiconductor Device Reliability/Quality Control System (C10983E)****Quality Grades On NEC Semiconductor Devices (C11531E)**

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