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TSC367/368
Schmitt Trigger
- Quad (Active Pullup)
- Quad (Open Collector)

Features

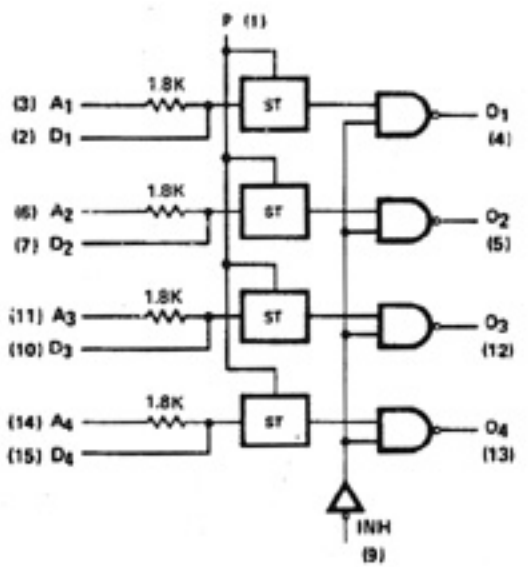
- 4.5V TYPICAL HYSTERESIS – 2.5V WORST CASE NOISE IMMUNITY, EVEN WHILE SWITCHING!
- 5.5V TYPICAL DC NOISE IMMUNITY – 4.5V WORST CASE
- OPTIONAL HOOKUP DOES NOT RECOGNIZE OPEN CIRCUITS – ELIMINATES FALSE COUNTS DUE TO CONTACT BOUNCE FROM SWITCHES AND RELAYS
- DELAY PINS ALLOW THE USE OF EXTERNAL SLOW-DOWN CAPACITORS – PROPAGATION DELAY INCREASES 2.5 ms/μF
- IDEAL FOR USE AS A LINE RECEIVER
- INHIBIT INPUT PERMITS INFORMATION TO BE ACCEPTED ONLY DURING PERIODS OF LOW NOISE IN THE SYSTEM CYCLE
- OVERVOLTAGE INPUT PROTECTION – WITHSTANDS ±100V, 1μSEC NOISE SPIKE OR −5V TO V_{CC} +5V STEADY-STATE

367 – DIRECTLY INTERFACES WITH HiNIL AND CMOS
368 – DIRECTLY INTERFACES WITH TTL

General Description

The Teledyne Semiconductor 367/368 Quad Schmitt Trigger has been designed as a universal input port for HiNIL logic blocks. Its unique truth table completely eliminates false counts due to contact bounce on switches, relays, etc. At the same time, its 6.5V DC noise immunity and the 4.5V dead zone provided by the Schmitt Trigger action totally eliminates noise problems occurring on long lines. Delay pins can be used with slowdown capacitors to slow the circuit down as far as needed, and still maintain 2.5V guaranteed noise immunity. An inhibit input can be used to accept input information only at certain times in the system cycle.

Logic Diagram

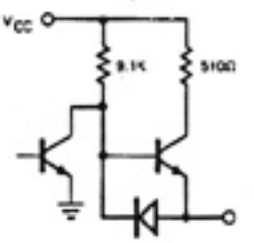


GRD – 8
V_{CC} – 16

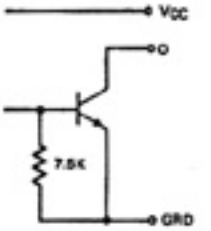
A – DATA INPUT
D – DELAY PIN
O – OUTPUT
INH – INHIBIT
P – PULL-UP

Equivalent Circuits

TYPICAL OUTPUT
367



TYPICAL OUTPUT
368



Truth Tables

367/368
PIN P OPEN

INPUTS		OUTPUT
A	INH	O
0	0	1
OPEN (was 0)	0	1
1	0	0
OPEN (was 1)	0	0
0	1	1
1	1	1
OPEN (was 0)	1	1
OPEN (was 1)	1	1

367/368
PIN P CONNECTED TO V_{CC}

INPUTS		OUTPUT
A	INH	O
0	0	1
1	0	0
0	1	1
1	1	1

Specifications

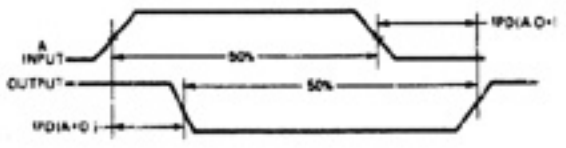
367

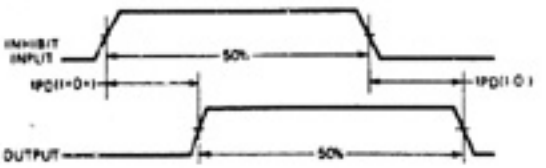
t_{PD} (Pull-up Open)	340ns	360ns	250ns	230ns
t_{PD} (Pull-up Closed)	300ns	400ns	250ns	230ns
I/O function for t_{PD}	A+O−	A−O+	I+O+	I−O−

368 WITH 10K PULLUP ON OUTPUT

t_{PD} (Pull-up Open)	340ns	550ns	450ns	300ns
t_{PD} (Pull-up Closed)	300ns	600ns	450ns	300ns

Switching Time Waveforms





Loading Table

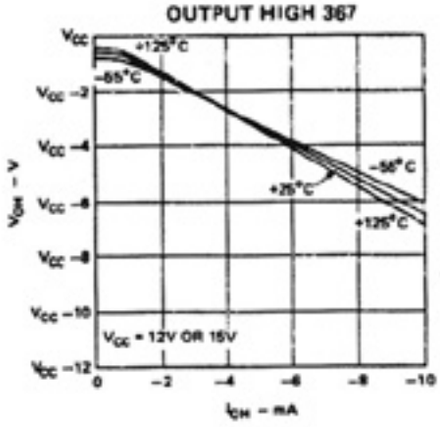
367/368

PINS	FUNCTION	LOADING
Inhibit	Inhibit	1 UL
O_1, O_2, O_3, O_4	Outputs	5 UL

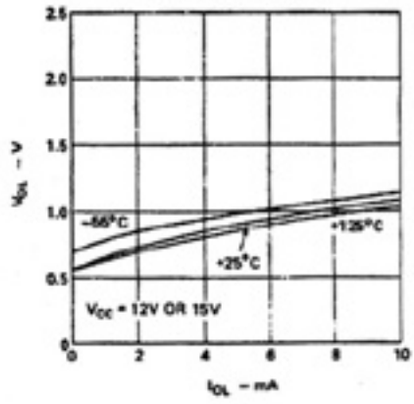
Typical Performance Characteristics

OUTPUT CURRENT VS. OUTPUT VOLTAGE

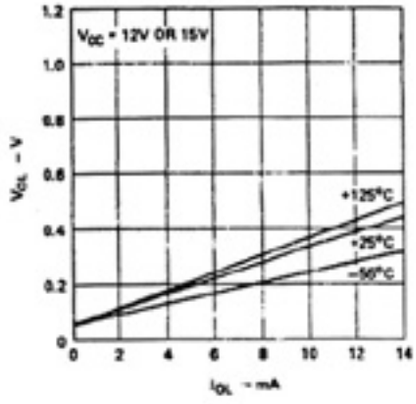
OUTPUT HIGH 367



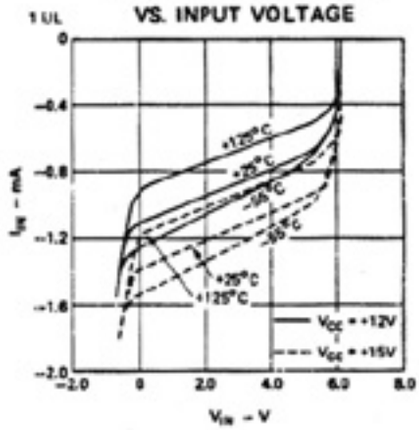
OUTPUT LOW 367



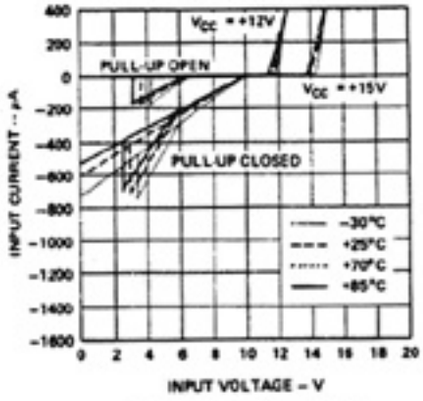
OUTPUT LOW 368



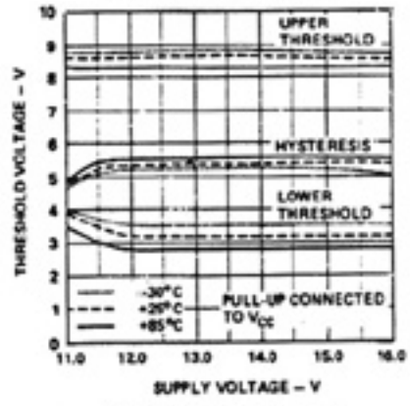
INHIBIT INPUT CURRENT VS. INPUT VOLTAGE



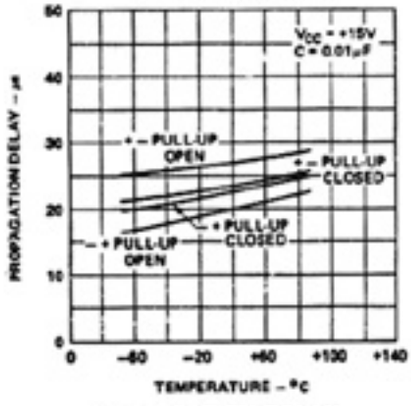
INPUT CURRENT VS. INPUT VOLTAGE



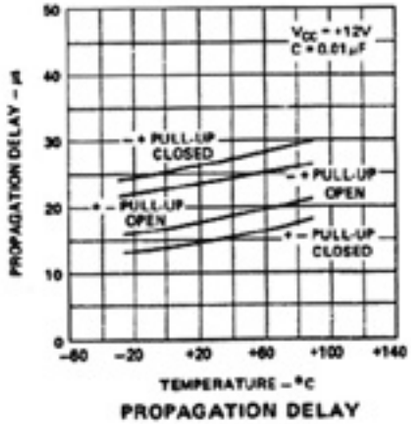
THRESHOLDS AND HYSTERESIS VS. SUPPLY VOLTAGE



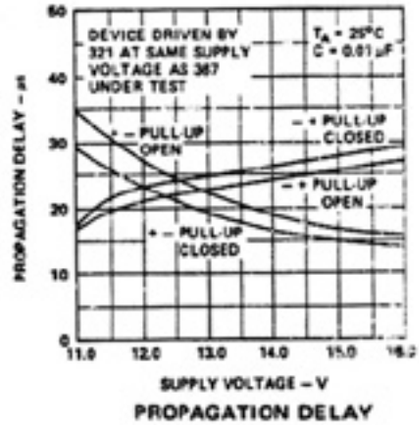
PROPAGATION DELAY VS. TEMPERATURE



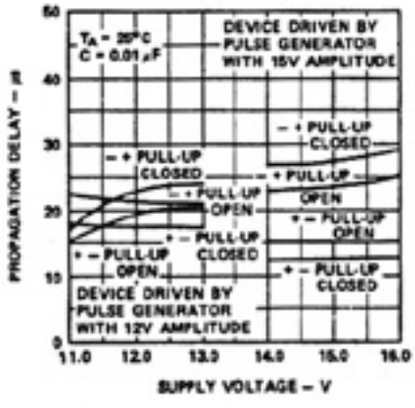
PROPAGATION DELAY VS. TEMPERATURE



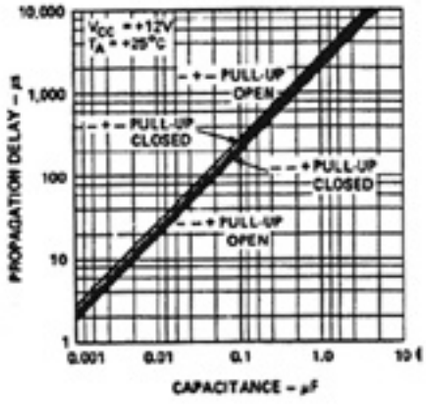
PROPAGATION DELAY VS. SUPPLY VOLTAGE



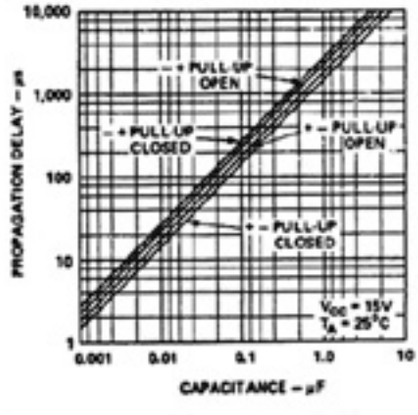
PROPAGATION DELAY VS. SUPPLY VOLTAGE



PROPAGATION DELAY VS. CAPACITANCE



PROPAGATION DELAY VS. CAPACITANCE



Electrical Characteristics

Parameter	Definition	$-30°C \leq T_A \leq +85°C$ Type C (V_{CC} = +12V ± 1V)	$-30°C \leq T_A \leq +70°C$ Type A (V_{CC} = +15V ± 1V)	Test Conditions
V_{INL} (Inhibit)	Input threshold voltage, low	5.0V min.	5.0V min.	Guaranteed input low threshold for Inhibit
V_{INH} (Inhibit)	Input threshold voltage, high	6.5V max.	6.5V max.	Guaranteed input high threshold for Inhibit
I_{INL} (Inhibit)	Input current, low	−2.1mA	−2.6mA	At V_{CC} max. with $V_{IN} = V_{OL1}$
I_{INH} (Inhibit)	Input leakage current	10μA	10μA	At V_{CC} max. with $V_{IN} = V_{CC}$ max.
V_T + (Data input-A) (pull-up open)	Positive going threshold voltage	8.0V min. 10.0V max.	7.5V min. 10.0V max.	Guaranteed positive going threshold for Data input (pull-up open)
V_T − (Data input-A) (pull-up open)	Negative going threshold voltage	2.0V min. 5.5V max.	2.0V min. 5.0V max.	Guaranteed negative going threshold for Data input (pull-up open)
V_T + (Data input-A) (pull-up closed)	Positive going threshold voltage	7.5V min. 9.5V max.	7.5V min. 9.5V max.	Guaranteed positive going threshold for Data input (pull-up closed)
V_T − (Data input-A) (pull-up closed)	Negative going threshold voltage	1.5V min. 5.0V max.	1.0V min. 4.5V max.	Guaranteed negative going threshold for Data input (pull-up closed)
I_T + (Data input-A) (pull-up open)	Input current at positive going threshold	40μA max.	40μA max.	Guaranteed input leakage current V_{IN} + 10V (pull-up open)
I_T − (Data input-A) (pull-up open)	Input current at negative going threshold	−1.0mA max.	−1.2mA max.	Guaranteed input low current. V_{IN} = 1.5V for C device and 1.8V for A device (pull-up open)
I_T + (Data input-A) (pull-up closed)	Input current at positive going threshold	40μA max.	40μA max.	Guaranteed input leakage current V_{IN} = 10V (pull-up closed)
I_T − (Data input-A) (pull-up closed)	Input current at negative going threshold	−2.1mA	−2.6mA	Guaranteed input low current V_{IN} = 1.5V for C device and 1.8V for A device (pull-up closed)
I_T (max)	Maximum input current	1.0mA	1.5mA	V_{IN} = 13V, V_{CC} = 13V for C device, V_{IN} = 15V, V_{CC} = 16V for A device
V_{OL}	Output low voltage	1.5V max.	1.8V max.	I_{OL} = 5 UL (1 UL = 2.1mA for C grade and 2.6mA for A grade)
V_{OL3} (368 only)	Output low voltage	0.4V max.	0.4V max.	At $V_{CC} = V_{CC}$ min, I_{OL} = 6.4mA (4 TTL UL)
V_{OH} (367 only)	Output high voltage	10.0V min.	13.0V min.	I_{OH} = 5 UL (1 UL = 10μA)
V_{OHL} (367 only)	Output high voltage loaded	7.0V min.	9.5V min.	At V_{CC} nominal I_{OH} = −5mA
I_{CC}	Power supply current (367) (368)	 36mA max. 33mA max.	 54mA max. 50mA max.	At V_{CC} maximum. Unit tested under worst case conditions
I_{CEX}	Output high leakage current (368)	25μA max.	25μA max.	At V_{CC} maximum, V_{INL} = 5.0V, $V_{CEX} = V_{CC}$ max
V_{MAX} (368 only)	Output high breakdown voltage	13.0V min.	16.5V min.	At I_{max} = 1.0mA, V_{INL} = 5.0V with I_{max} forced into output

Typical Applications

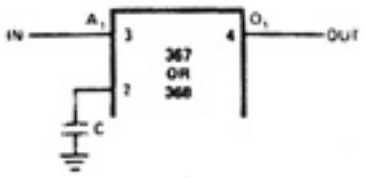
The HiNIL 367/368 Quad Schmitt Trigger has been designed to be a universal input port into HiNIL logic blocks. Its active outputs (367) are fully compatible with the rest of the HiNIL logic family and 12 or 15V CMOS. Although its inputs are not standard HiNIL, they can be used either with other HiNIL logic elements or with switch and relay contacts. The device is unique in that the user is presented with a choice of two truth tables, determined by whether an internal pullup resistor (pin P) is left open or is connected to V_{CC}. If Pin P is left open, the device will not recognize open circuits. By this we mean that the input will continue to see the logic state that was at the input before the connection was broken. It is this characteristic that eliminates errors due to contact bounce on relay or switch contacts. If Pin P is tied to V_{CC}, the device acts like a standard HiNIL circuit and considers an open input connection to be a logic one.

Occasionally a system is expected to be operable in extremely noisy environments where short noise pulses are expected in excess of 4.5V noise immunity. This problem can be eliminated by adding slow-down capacitors to special delay pins provided for this purpose. For each μF of capacitance added between the delay pin and ground the propagation delay will be increased by 2.5 ms.

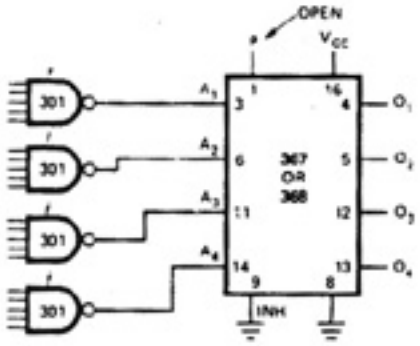
Typical Applications (contd.)

An inhibit pin is provided that forces all outputs high whenever it is high. This can be used to restrict the 367/368 so that it accepts input information only at certain points in the machine cycle. When used with pullup resistors, the open collector 368 allows direct interface to TTL, RTL, and low voltage CMOS, NMOS, or PMOS.

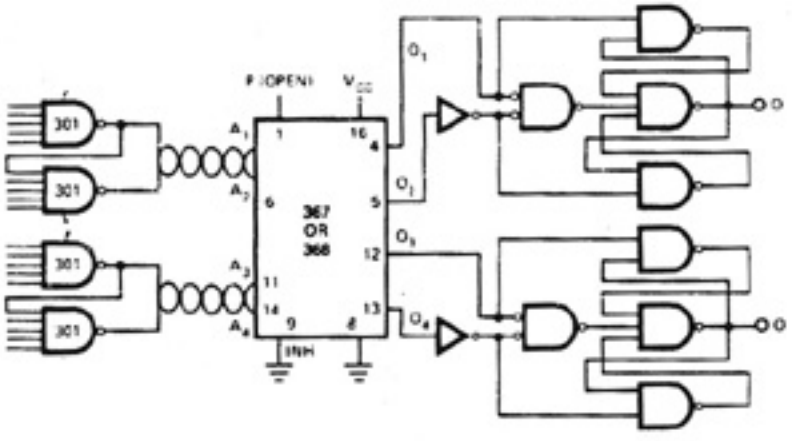
PULSE DELAY



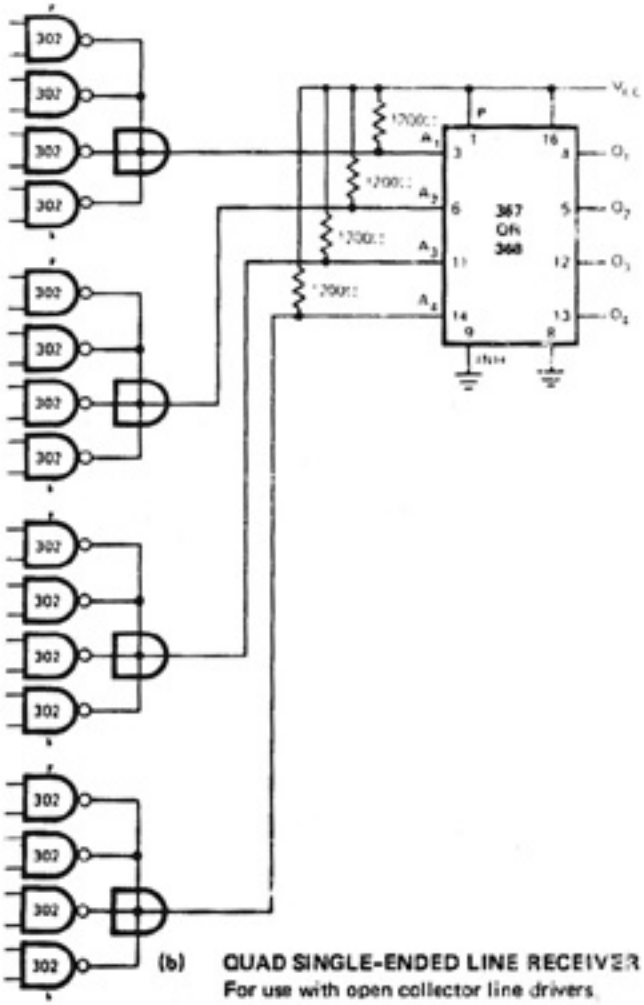
LINE RECEIVERS



(a) **QUAD SINGLE-ENDED LINE RECEIVER**
Slow down capacitors may be added to the delay inputs to improve noise-immunity.



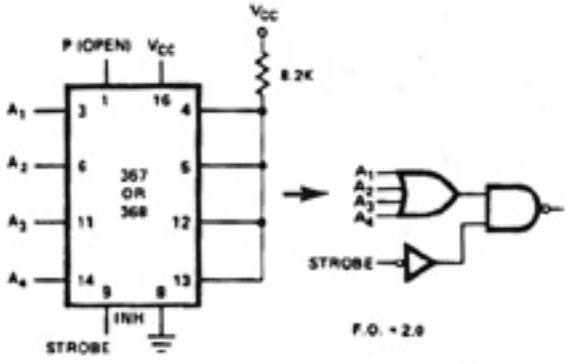
(c) **DUAL DIFFERENTIAL LINE-RECEIVER**
Slow down capacitors may be added to the delay inputs to improve noise immunity.



(b) **QUAD SINGLE-ENDED LINE RECEIVER**
For use with open collector line drivers. Slow down capacitors may be added to the delay inputs to improve noise immunity.

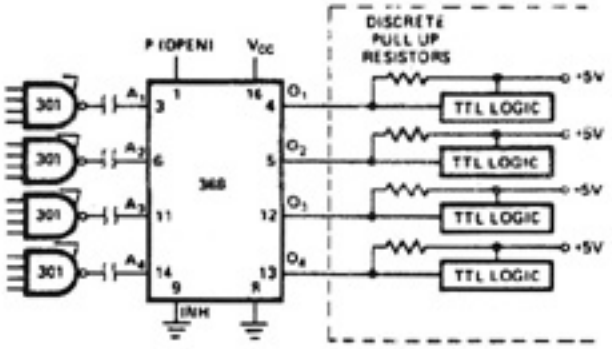
4 INPUT STROBED NOR GATE

The 368 can be used as a strobed 4 input NOR gate by tying all output pins (collector-ORing) to a common pull-up resistor, and connecting the strobe input to the INHIBIT line.



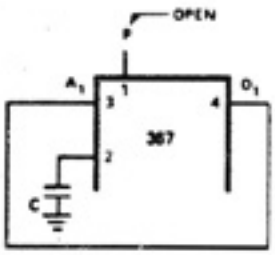
Typical Applications (contd.)

QUAD LINE RECEIVER/TTL INTERFACE



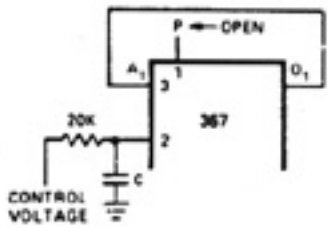
The 368 with open collector output allows direct drive interface to TTL logic.

FREE-RUNNING OSCILLATOR



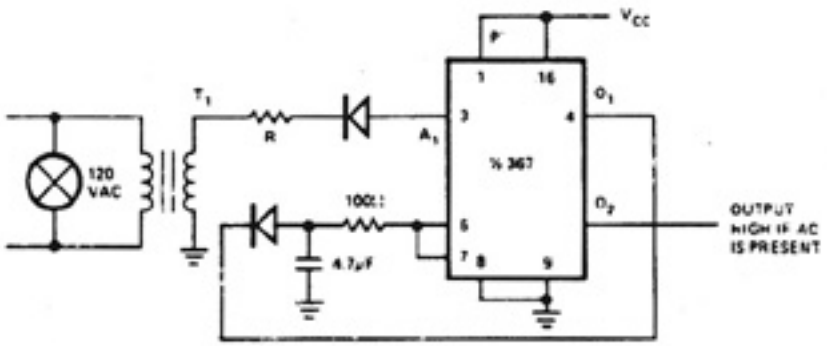
The 367 can be used to make four independent free-running oscillators. The frequency is set by the value of C tied to each delay input. The oscillators can all be started and stopped by using the inhibit input.

VOLTAGE CONTROLLED OSCILLATOR



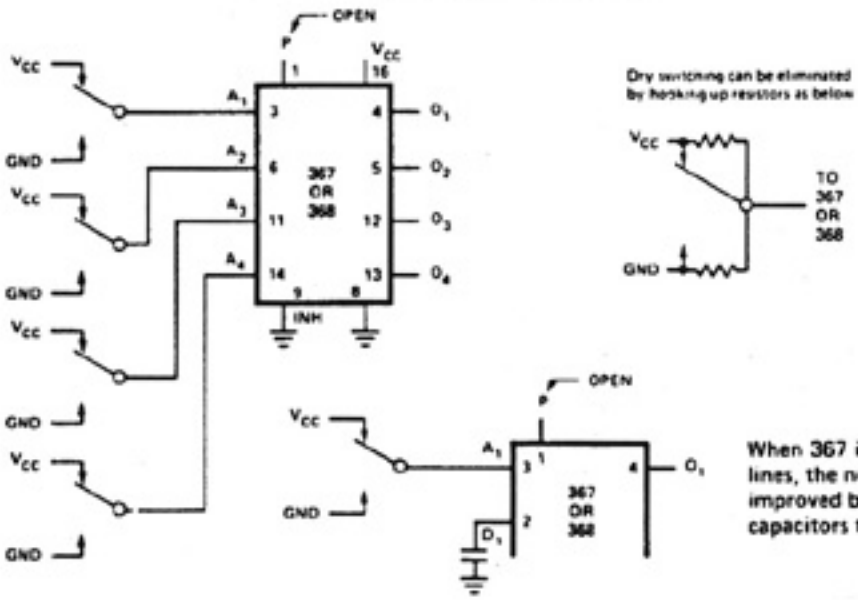
The 367 can be used to make four, independent voltage controlled oscillators.

AC LINE VOLTAGE DETECTOR



This circuit delivers logic one's whenever 120 VAC is present on the solenoid valve. Since only 1/2 of the 367 is used, two such circuits can be built with each device.

BOUNCE-FREE SWITCH



Dry switching can be eliminated by hooking up resistors as below

When 367 is being used with long lines, the noise immunity may be improved by adding slow-down capacitors to the delay input.