SiGe HBT MMIC
POWER AMPLIFIER

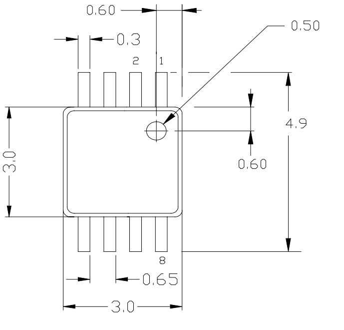
Description

A monolithic, high-efficiency, silicon-germanium power amplifier IC, the THM1001TE is designed for 2.4GHz wireless applications including Bluetooth[tm] Class 1 wireless technology and 2.4GHz cordless telephone applications. It delivers +23 dBm output power, making it capable of overcoming insertion losses of up to 3.0dB between amplifier output and antenna.

The silicon-germanium structure of the THM1001TE, and its exposed-die-pad package, soldered to the system PCB, provide high thermal conductivity and a subsequently low junction temperature.

Features

- **+23 dBm at 44% Power Added Efficiency**
- **Temperature stability better than 1dB**
- **Power-control and Power-down modes**
- **Single 3.3 V Supply Operation**
- **Temperature Rating: -40C to +85C**
- **8 lead Exposed Pad MSOP8 Plastic Package**

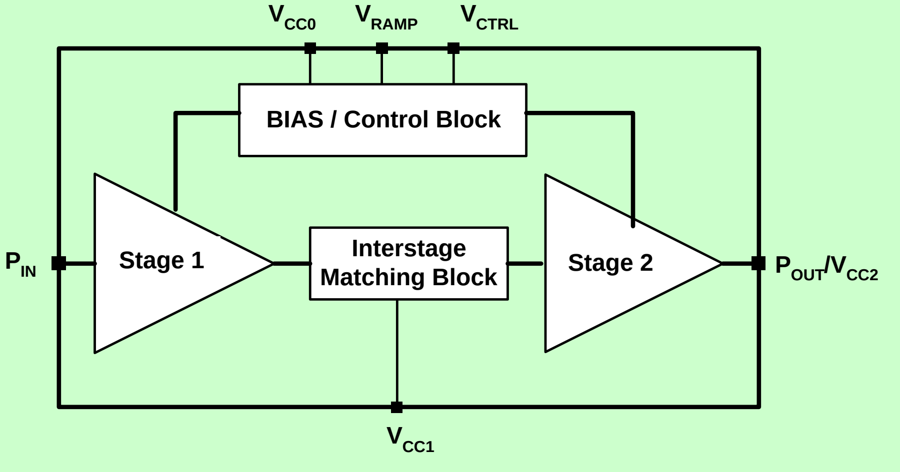


E_PAD MSOP8

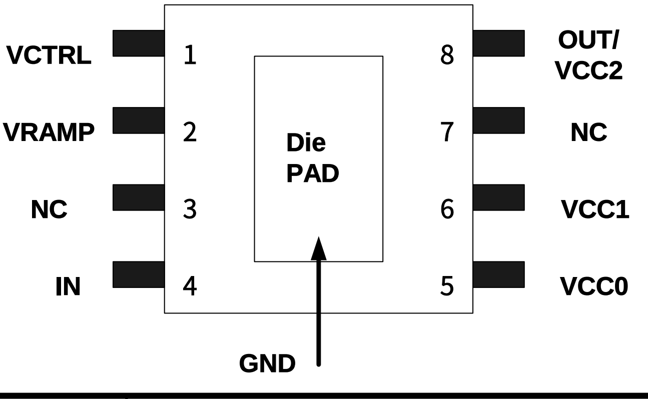
Applications

- **Bluetooth[tm] Wireless Technology (Class 1)**
- **USB Dongles, modules**
- **PCMCIA, Flash cards**
- **Access Points**
- **2.4GHz cordless telephone**

Function Block Diagram



Pin Configuration



Pin Description

Pin No	Name	Description
1	V_{CTL}	Controls the output level of the power amplifier.
2	V_{RAMP}	Power amplifier enable pin.
3	NC	No connection.
4	IN	Power amplifier RF input.
5	V_{CC0}	Bias supply voltage.
6	V_{CC1}	Stage 1 collector supply voltage.
7	NC	No connection.
8	OUT/V_{CC2}	Power Amplifier Output and Stage 2 collector supply voltage.
Die Pad	GND	Heatslug Die Pad is ground.

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Supply Voltage	Vcc	V	-0.3	+3.6
Control Voltage	V_{CTL}	V	-0.3	Vcc
Ramping Voltage	V_{RAMP}	V	-0.3	Vcc
IN	RF Input Power	dBm		+8
T_A	Operating Temperature Range	°C	-40	+85
T_{STG}	Storage Temperature Range	°C	-40	+150
Tj	Maximum Junction Temperature	°C		+150

Operation in excess of any one of above Absolute Maximum Ratings may result in permanent damage.
Handling and assembly of this device should be at ESD protected workstations.

DC Electrical Characteristics

Condition : V_{CC0}=V_{CC1}=V_{CC2}=V_{RAMP}=3.3V, T_A=25℃,
Input and Output externally matched to 50 Ω unless otherwise noted.

Symbol	Note	Parameter	Min.	Typ.	Max.	Unit
Vcc		Supply Voltage		3.3		V
Icc	1	Supply Current (Icc=Ivcc0+Ivcc2), V_{CTL}=3.3V		90	150	mA
△ICCtemp	3	Supply Current Variation over Temperature from T_A=25℃ (-40℃<T_A<+85℃)		TBD		%
V_{CTL}		PA Output Power Control Voltage Range		0 ~ VCC		V
I_{CTL}	1	Current sunk by V_{CTL} Pin		130		μA
V_{RAMP}	3	Logic High Voltage		2.4		V
	3	Logic Low Voltage		0.4		V
Istby	1	Leakage Current when Vramp=0V, Vctl=high		3	10	μA

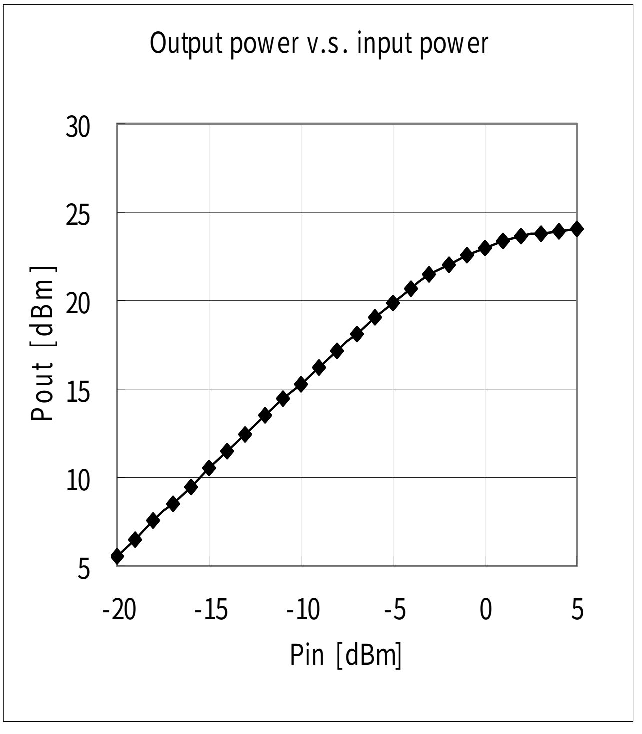
AC Electrical Characteristics

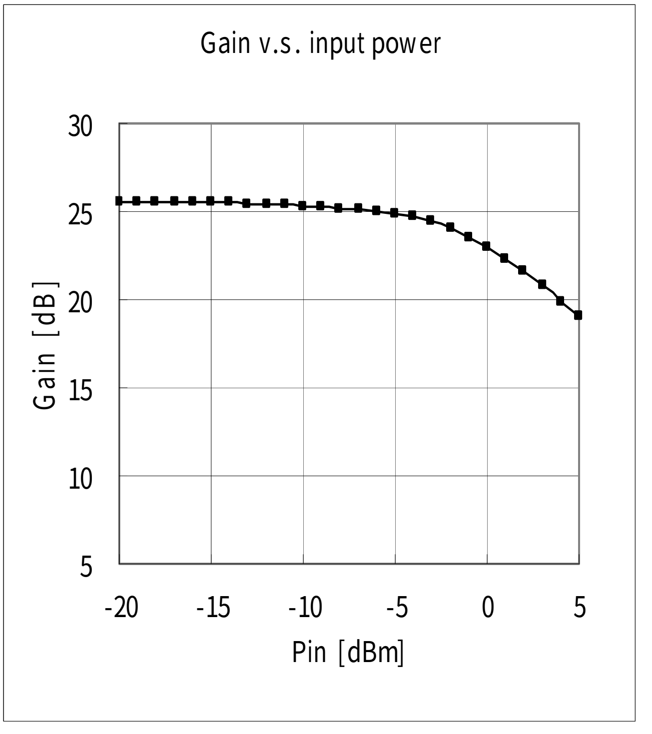
Condition : $V_{CC0}=V_{CC1}=V_{CC2}=V_{RAMP}$=3.3V, PIN=+2dBm, T_A=25℃, f=2.45GHz,
Input and Output externally matched to 50 Ω unless otherwise noted.

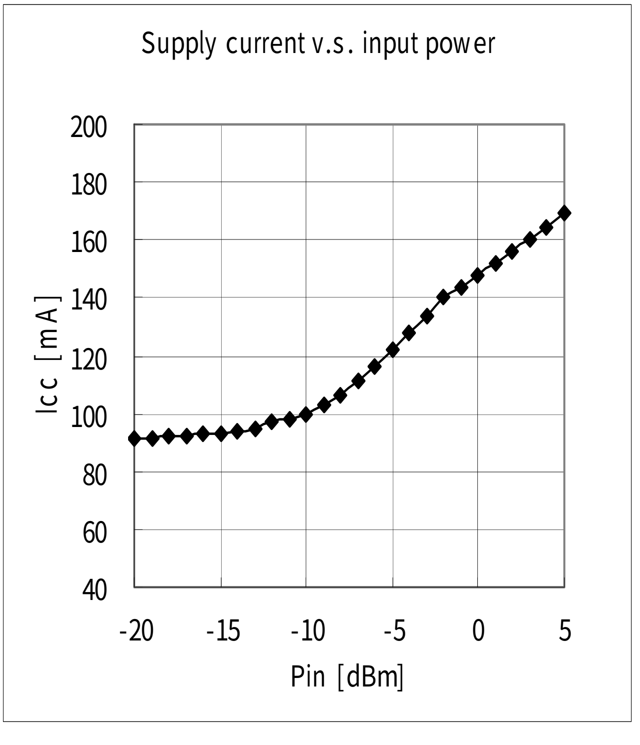
Symbol	Note	Parameter	Min.	Typ.	Max.	Unit
fL-U	3	Frequency Range	2400 ~ 2500			MHz
Pout	1	Output Power @P_{IN} = +2dBm, V_{CTL}=3.3V	22	23		dBm
	1	Output Power @P_{IN} = +2dBm, V_{CTL}=0.4V		-20	-10	dBm
ΔPtemp	3	Output Power Variation over temperature (-40℃<TA<+85℃)		TBD		dB
dP_{OUT}/dV_{CTL}	3	Control Voltage Sensitivity			120	dBm/V
PAE		Power Added Efficiency at +23dBm Output Power		44		%
G	3	Gain @ P_{IN}= -20dBm Gain @ P_{IN}= -10dBm	25 24	26 25		dB dB
G_{VAR}	3	Gain Variation over band (2400-2500 MHz)		0.7	1.0	dB
2f,3f,4f,5f	3, 4	Harmonics		35	30	dBc
$\|S_{21}\|_{OFF}$	2	Isolation in “OFF” State, P_{IN}=+2dBm, V_{RAMP}=0V		35		dB
$\|S_{12}\|$	2	Reverse Isolation		34		dB
STAB	2	Stability (P_{IN}=+2dBm, Load VSWR=6:1)	All non-harmonically Related outputs less than –50dBc			

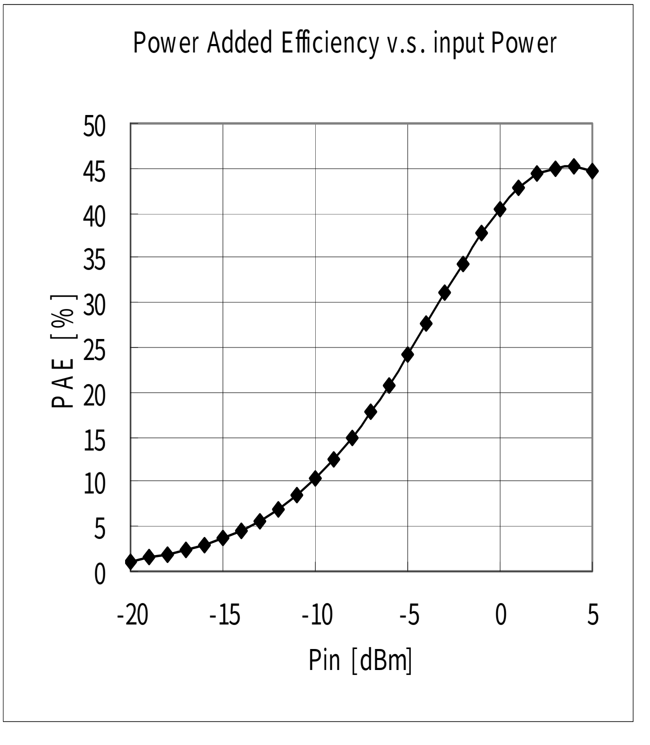
Notes : (1) Guaranteed by production test at T_A=25℃.
(2) Guaranteed by design only
(3) Guaranteed by design and characterization
(4) Harmonic levels are greatly affected by topology of external matching networks.

Typical Characteristics

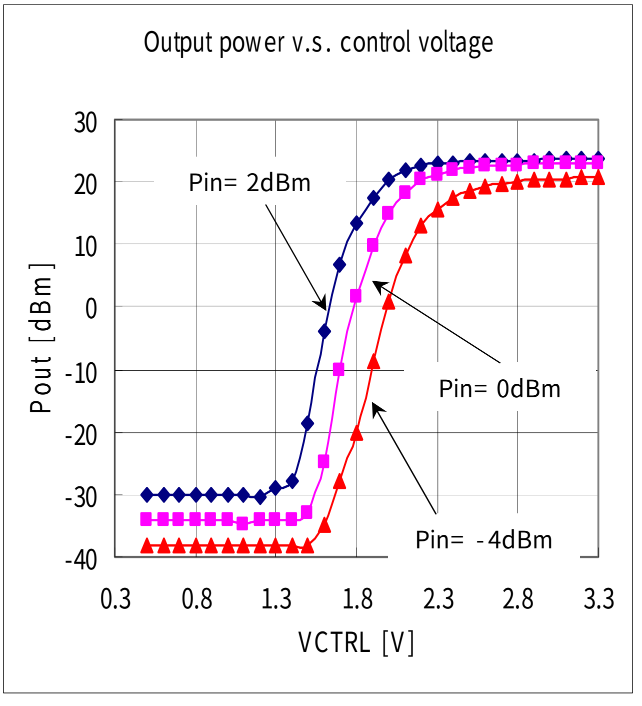


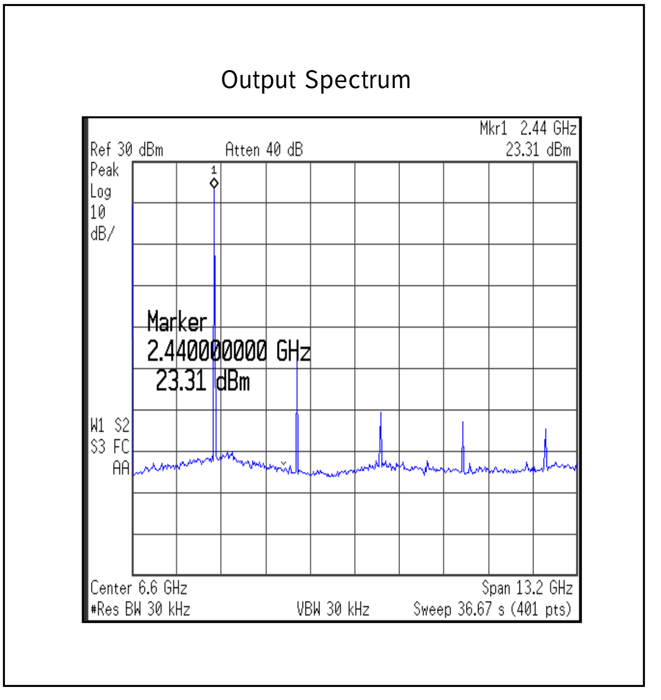


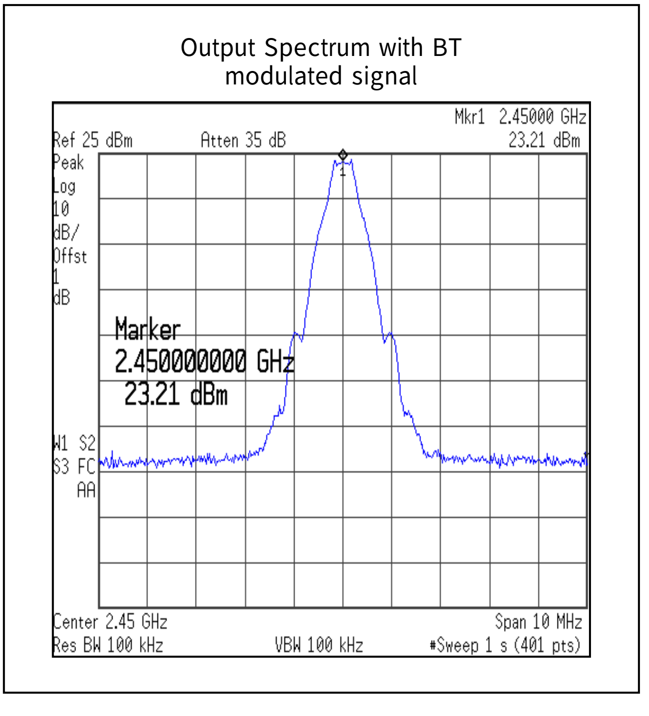




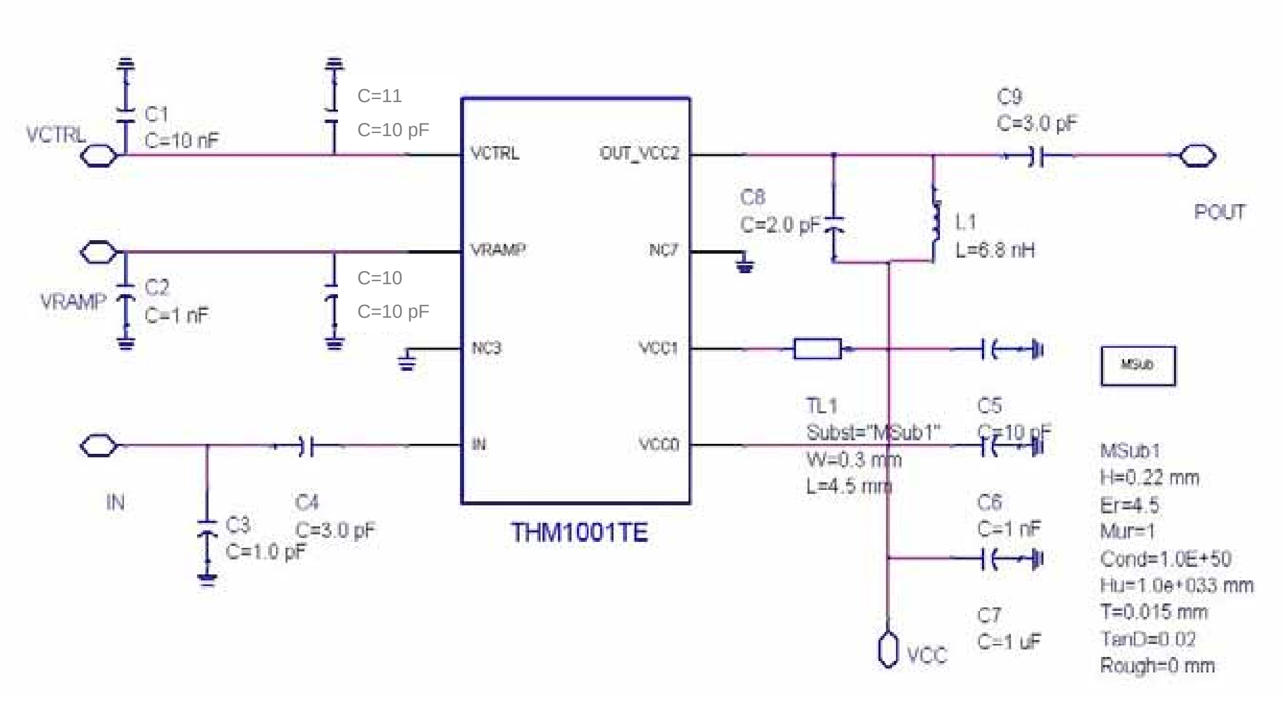
Typical Characteristics







Evaluation Board Schematic



Component List

Designation	Description	Part Number
C1	Cap 10 nF DC50V Chip Monolithic Ceramic	muRata #GRM36X7R103K16
C2, C6	Cap 1 nF DC50V Chip Monolithic Ceramic	muRata #GRM36X7R102K50
C3	Cap 1 pF DC50V Chip Monolithic Ceramic	muRata #GRM36C0G010C50
C4, C9	Cap 3 pF DC50V Chip Monolithic Ceramic	muRata #GRM36C0G030C50
C5, C10, C11	Cap 10 pF DC50V Chip Monolithic Ceramic	muRata #GRM36C0G100D50
C7	Cap 1 uF Chip Monolithic Ceramic	muRata #GRM36Y5V105Z6.3
C8	Cap 2 pF DC50V Chip Monolithic Ceramic	muRata #GRM36C0G020C50
L1		muRata #LQG15HN6N8J02

Evaluation Board Layout

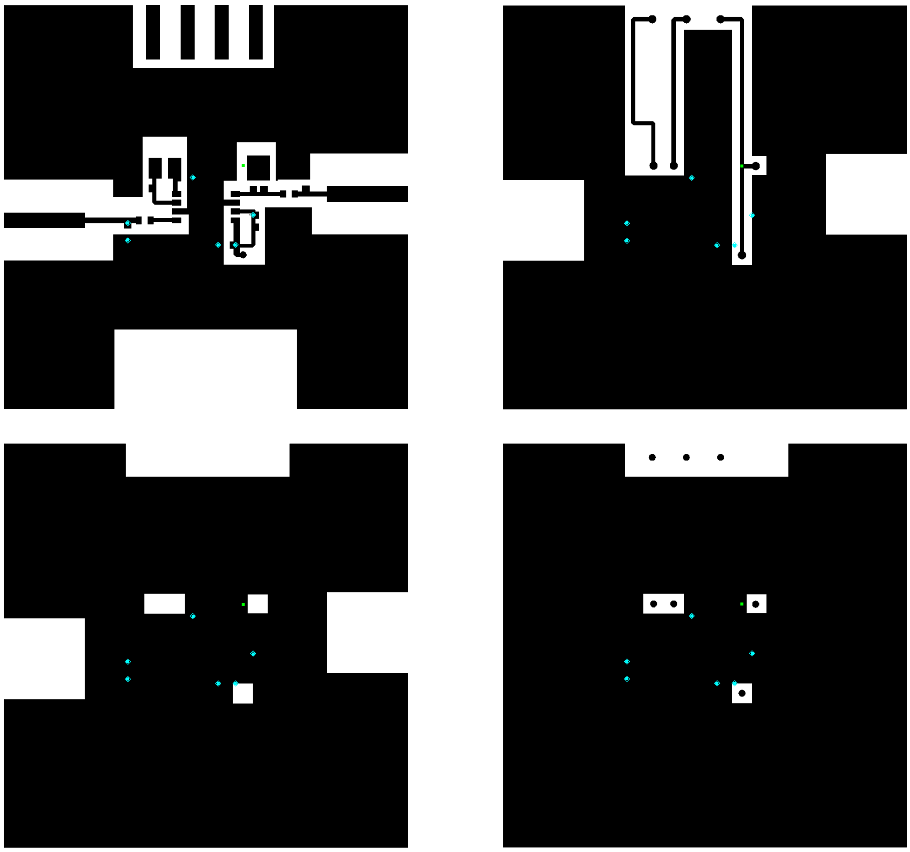
Board Size 30 x 30 mm^2

1. Top layer

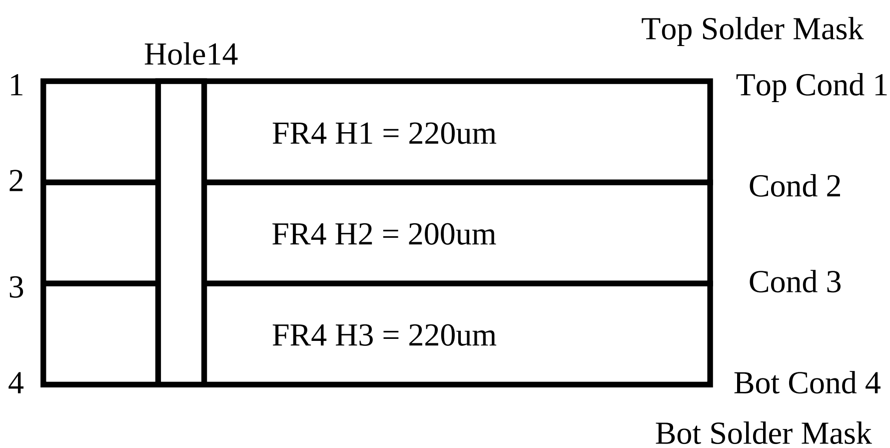
3. Middle2 layer
   DC Path

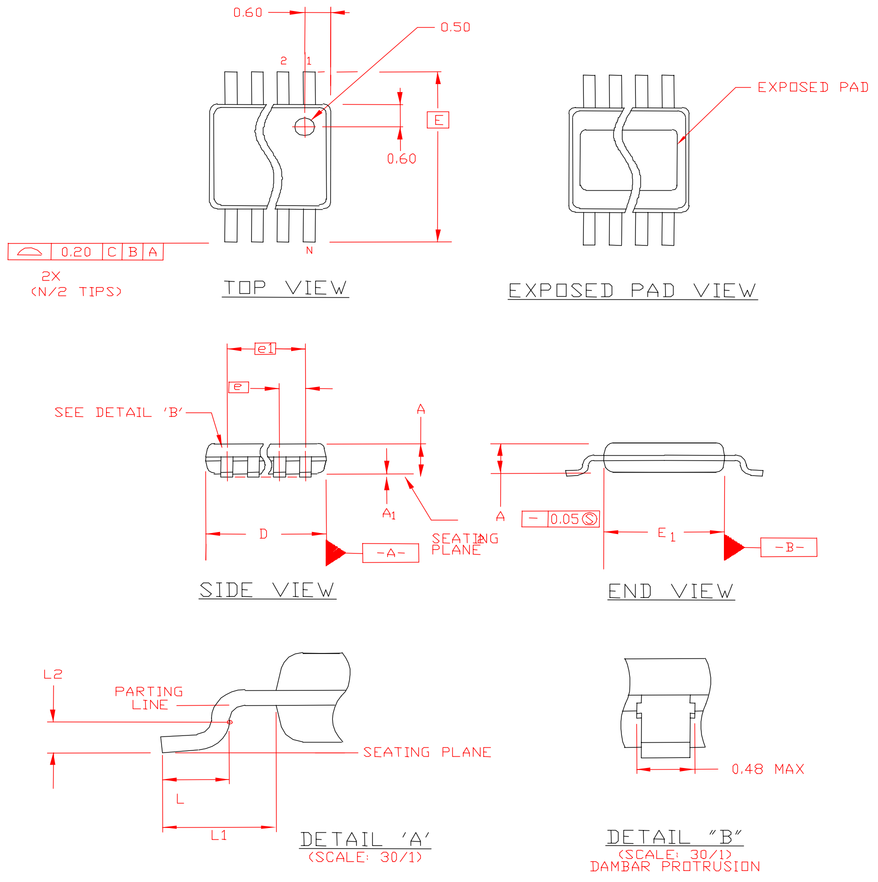
2. Middle1 Layer
   Inner GND

4. Bottom layer
   Ground Plane



Material & Structure of PCB





Symbol	Dimension in mm			Note
	Min	Typ	Max	
A	-	-	1.10	
A1	0.05	0.10	0.15	
A2	0.75	0.85	0.95	
b	0.25	-	0.38	
C	0.13	-	0.23	
D	3.00 BSC			
E	4.90 BSC			
E1	3.00 BSC			
e	0.65 BSC			
e1	1.95 BSC			
L	0.40	0.55	0.70	
L1	0.95 BSC			
L2	0.25 BSC			