**TENTATIVE**   TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT   SILICON GATE CMOS

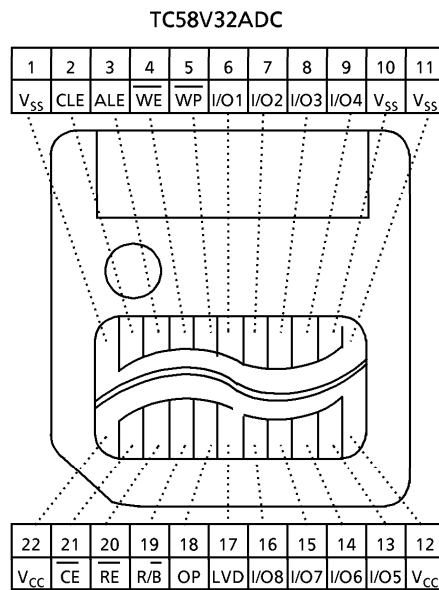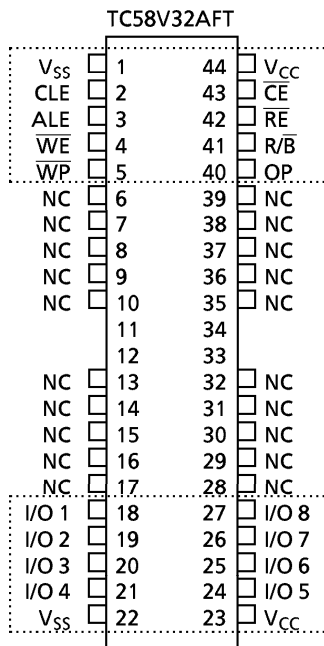## 32 Mbit (4 M × 8 bit) CMOS NAND E²PROM

### DESCRIPTION

The TC58V32AFT/ADC device is a single volt 32 M (34,603,008) bit NAND Electrically Erasable and Programmable Read Only Memory (NAND EEPROM) organized as 528 bytes × 16 pages × 512 blocks. The device has a 528 byte static register which allows the program and read data to be transferred between the register and the memory cell array in 528 byte increments. The erase operation is implemented in a single block unit (8K bytes + 256 bytes : 528 bytes × 16 pages).

The TC58V32AFT/ADC is a serial type of memory device which utilizes the I/O pins for both address and data input / output as well as command inputs. The erase and program operations are automatically executed making the device most suitable for applications such as Solid State File Storage, Voice Recording, Image File Memory for still cameras and other systems which require large density, non-volatile memory data storage.

### FEATURES

- Organization
  | | |
  |---|---|
  | Memory cell array | 528 × 8 K × 8 |
  | Register | 528 × 8 |
  | Page size | 528 bytes |
  | Block size | (8 K + 256) bytes |
- Mode
  - Read
  - Reset, Auto page program
  - Auto block erase, Status read
- Mode control
  - Serial input/output
  - Command control

- Power supply
  - TC58V32AFT : $V_{CC} = 3.0\,V$ to $5.5\,V$
  - TC58V32ADC : $V_{CC} = 3.3\,V \pm 0.3\,V$
- Access time
  | | |
  |---|---|
  | Cell array - Register | 10 $\mu s$ max |
  | Serial Read Cycle | 50 ns min |
- Operating current
  | | |
  |---|---|
  | Read (50ns cycle) | 10 mA typ |
  | Program (ave.) | 10 mA typ |
  | Erase (ave.) | 10 mA typ |
  | Standby | 100 $\mu A$ |
- Package
  - TC58V32AFT : TSOP II 44/40 - P - 400 - 0.80B (Weight : 0.48 g Typ.)
  - TC58V32ADC : FDC - 22A (Weight : 1.8 g Typ.)

### PIN ASSIGNMENT (TOP VIEW)

**TC58V32AFT**

| | | | |
|---|---|---|---|
| Vss | 1 | 44 | Vcc |
| CLE | 2 | 43 | $\overline{CE}$ |
| ALE | 3 | 42 | $\overline{RE}$ |
| $\overline{WE}$ | 4 | 41 | R/$\overline{B}$ |
| $\overline{WP}$ | 5 | 40 | OP |
| NC | 6 | 39 | NC |
| NC | 7 | 38 | NC |
| NC | 8 | 37 | NC |
| NC | 9 | 36 | NC |
| NC | 10 | 35 | NC |
| | 11 | 34 | |
| | 12 | 33 | |
| NC | 13 | 32 | NC |
| NC | 14 | 31 | NC |
| NC | 15 | 30 | NC |
| NC | 16 | 29 | NC |
| NC | 17 | 28 | NC |
| I/O 1 | 18 | 27 | I/O 8 |
| I/O 2 | 19 | 26 | I/O 7 |
| I/O 3 | 20 | 25 | I/O 6 |
| I/O 4 | 21 | 24 | I/O 5 |
| Vss | 22 | 23 | Vcc |

**TC58V32ADC**

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|
| Vss | CLE | ALE | $\overline{WE}$ | $\overline{WP}$ | I/O1 | I/O2 | I/O3 | I/O4 | Vss | Vss |



| 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|
| Vcc | $\overline{CE}$ | $\overline{RE}$ | R/$\overline{B}$ | OP | LVD | I/O8 | I/O7 | I/O6 | I/O5 | Vcc |

### PIN ASSIGNMENT

| I/O$_{1\,to\,8}$ | I/O port |
|---|---|
| $\overline{CE}$ | Chip enable |
| $\overline{WE}$ | Write enable |
| $\overline{RE}$ | Read enable |
| CLE | Command latch enable |
| ALE | Address latch enable |
| $\overline{WP}$ | Write protect |
| R/$\overline{B}$ | Ready / Busy |
| OP | Option Pin |
| LVD | Low Voltage Detect |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |

OP : GND Input : 528 Byte / Page Operation
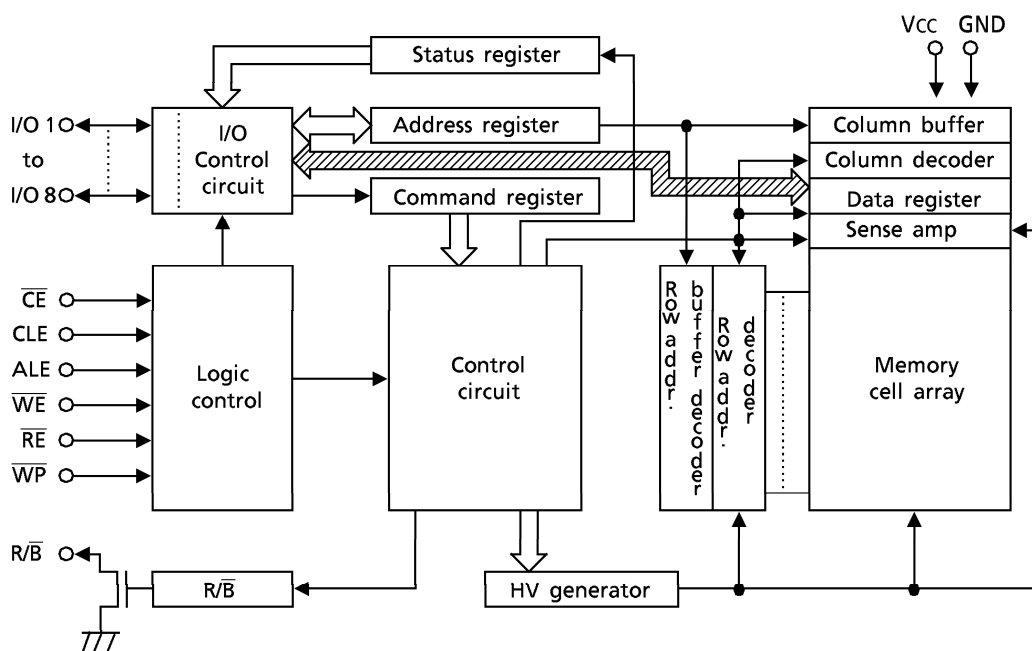Vcc Input : 512 Byte / Page Operation

961001EBA1

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | RATING | VALUE | | UNIT |
|---|---|---|---|---|
| | | TC58V32AFT | TC58V32ADC | |
| $V_{CC}$ | Power supply Voltage | $-0.6$ to $6.0$ | $-0.6$ to $4.6$ | V |
| $V_{IN}$ | Input Voltage | $-0.6$ to $6.0$ | $-0.6$ to $4.6$ | V |
| $V_{I/O}$ | Input / Output Voltage | $-0.6V$ to $Vcc + 0.3V (\leqq 6.0V)$ | $-0.6V$ to $Vcc + 0.3V (\leqq 4.6V)$ | V |
| $P_D$ | Power Dissipation | $0.5$ | $0.5$ | W |
| $T_{SOLDER}$ | Soldering Temperature (10 s) | $260$ | $-$ | °C |
| $T_{STG}$ | Storage Temperature | $-55$ to $150$ | $-20$ to $65$ | °C |
| $T_{OPR}$ | Operating Temperature | $0$ to $70$ | $0$ to $55$ | °C |

## CAPACITANCE *(Ta = 25°C, f = 1 MHz)

| SYMBOL | PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $C_{IN}$ | Input | $V_{IN} = 0 V$ | $-$ | $10$ | pF |
| $C_{OUT}$ | Output | $V_{OUT} = 0 V$ | $-$ | $10$ | pF |

* This parameter is periodically sampled and is not tested for every component.

## VALID BLOCKS (1)

| SYMBOL | PARAMETER | TC58V32AFT/ADC | | | UNIT |
|--------|-----------|-----|-----|-----|------|
| | | MIN | TYP | MAX | |
| $N_{VB}$ | Valid Block Number | 502 | 508 | 512 | Blocks |

(1) The TC58V32AFT/ADC occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.

## DC RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | TC58V32AFT | | TC58V32ADC | | UNIT |
|--------|-----------|------|------|------|------|------|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Power Supply Voltage | 3.0 | 5.5 | 3.0 | 3.6 | V |
| $V_{IH}$ | High Level Input Voltage | 2.0*1/3.0*2 | $V_{CC} + 0.3$ | 2.0 | $V_{CC} + 0.3$ | V |
| $V_{IL}$ | Low Level Input Voltage | − 0.3 *3 | 0.8 | − 0.3 *3 | 0.8 | V |

*1 : $V_{CC} = 3.3V \pm 0.3V$

*2 : $V_{CC} > 3.6V$

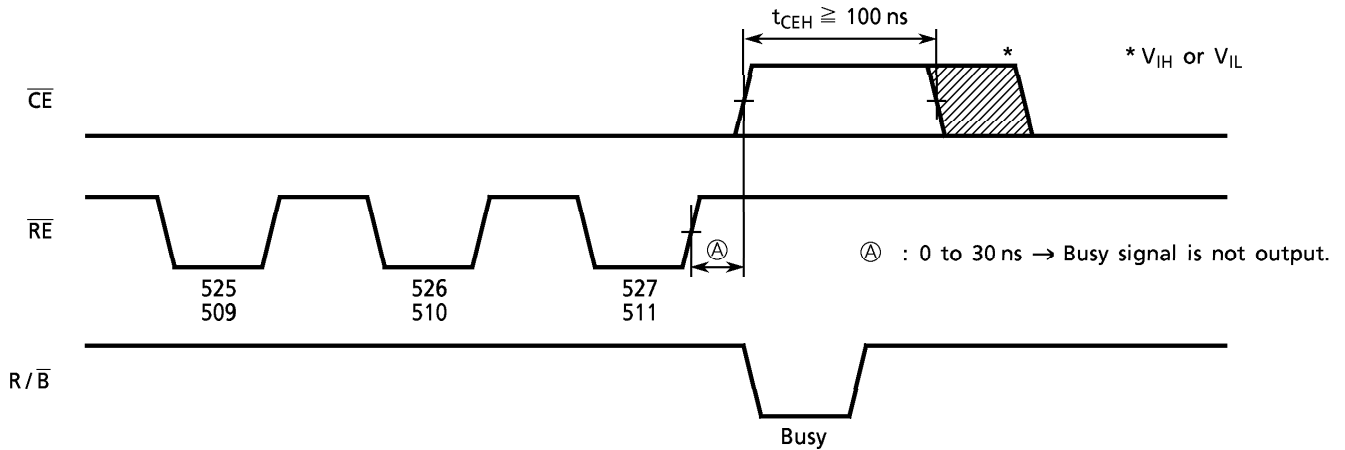*3 : − 2 V (pulse width $\leqq$ 20 ns)

## DC CHARACTERISTICS
(TC58V32AFT : Ta = 0° to 70°C, $V_{CC}$ = 3.0 V to 5.5 V
(TC58V32ADC    : Ta = 0° to 55 °C, $V_{CC}$ = 3.3 V ± 0.3 V)

| SYMBOL | PARAMETER | CONDITION | $V_{CC} = 3.3 V \pm 0.3 V$ | | | $V_{CC} > 3.6 V$ | | | UNIT |
|--------|-----------|-----------|-----|-----|-----|-----|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_{IL}$ | Input Leak Current | $V_{IN} = 0V \sim V_{CC}$ | – | – | ± 10 | – | – | ± 10 | $\mu$A |
| $I_{LO}$ | Output Leak Current | $V_{OUT} = 0.4V \sim V_{CC}$ | – | – | ± 10 | – | – | ± 10 | $\mu$A |
| $I_{CCO1}$ | Operating Current (Serial Read) | $\overline{CE} = V_{IL}$, Iout = 0mA, $t_{cycle} = 50$ ns | – | 10 | 20 | – | 15 | 30 | mA |
| $I_{CCO3}$ | Operating Current (Command Input) | $t_{cycle} = 50$ ns | – | 10 | 20 | – | 15 | 30 | mA |
| $I_{CCO4}$ | Operating Current (Data Input) | $t_{cycle} = 50$ ns | – | 10 | 20 | – | 15 | 30 | mA |
| $I_{CCO5}$ | Operating Current (Address Input) | $t_{cycle} = 50$ ns | – | 10 | 20 | – | 15 | 30 | mA |
| $I_{CCO7}$ | Programming Current | – | – | 10 | 20 | – | 15 | 30 | mA |
| $I_{CCO8}$ | Erasing Current | – | – | 10 | 20 | – | 15 | 30 | mA |
| $I_{CCS1}$ | Standby Current | $\overline{CE} = V_{IH}$ | – | – | 1 | – | – | 1 | mA |
| $I_{CCS2}$ | Standby Current | $\overline{CE} = V_{CC} - 0.2$ V | – | – | 100 | – | – | 100 | $\mu$A |
| $V_{OH}$ | High Level Output Voltage | $I_{OH} = -400 \mu$A | 2.4 | – | – | 2.4 | – | – | V |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL} = 2.1$ mA | – | – | 0.4 | – | – | 0.4 | V |
| $I_{OL} (R/\overline{B})$ | Output Current of (R/$\overline{B}$) Pin | $V_{OL} = 0.4$ V | – | 8 | – | – | 8 | – | mA |

## AC CHARACTERISTICS AND OPERATING CONDITIONS

(TC58V32AFT : Ta = 0° to 70°C, $V_{CC}$ = 3.0 V to 5.5 V)
(TC58V32ADC : Ta = 0° to 55°C, $V_{CC}$ = 3.3 V ± 0.3 V)

| SYMBOL | PARAMETER | MIN | MAX | UNIT | NOTE |
|---|---|---|---|---|---|
| $t_{CLS}$ | CLE Set-Up Time | 0 | – | ns | |
| $t_{CLH}$ | CLE Hold Time | 10 | – | ns | |
| $t_{CS}$ | $\overline{CE}$ Set-Up Time | 0 | – | ns | |
| $t_{CH}$ | $\overline{CE}$ Hold Time | 10 | – | ns | |
| $t_{WP}$ | Write Pulse Width | 25 | – | ns | |
| $t_{ALS}$ | ALE Set-Up Time | 0 | – | ns | |
| $t_{ALH}$ | ALE Hold Time | 10 | – | ns | |
| $t_{DS}$ | Data Set-Up Time | 20 | – | ns | |
| $t_{DH}$ | Data Hold Time | 10 | – | ns | |
| $t_{WC}$ | Write Cycle Time | 50 | – | ns | |
| $t_{WH}$ | $\overline{WE}$ High Hold Time | 15 | – | ns | |
| $t_{WW}$ | $\overline{WP}$ High to $\overline{WE}$ Low | 100 | – | ns | |
| $t_{RR}$ | Ready to $\overline{RE}$ Falling Edge | 20 | – | ns | |
| $t_{RP}$ | Read Pulse Width | 35 | – | ns | |
| $t_{RC}$ | Read Cycle Time | 50 | – | ns | |
| $t_{REA}$ | $\overline{RE}$ Access Time (Serial Data Access) | – | 35 | ns | |
| $t_{CEH}$ | $\overline{CE}$ High Time for the Last Address in Serial Read Cycle | 100 | – | ns | (3) |
| $t_{REAID}$ | $\overline{RE}$ Access Time (ID Read) | – | 35 | ns | |
| $t_{OH}$ | Data Output Hold Time | 10 | – | ns | |
| $t_{RHZ}$ | $\overline{RE}$ High to Output High Impedance | – | 30 | ns | |
| $t_{CHZ}$ | $\overline{CE}$ High to Output High Impedance | – | 20 | ns | |
| $t_{REH}$ | $\overline{RE}$ High Hold Time | 15 | – | ns | |
| $t_{IR}$ | Output High Impedance to $\overline{RE}$ Rising Edge | 0 | – | ns | |
| $t_{RSTO}$ | $\overline{RE}$ Access Time (Status Read) | – | 35 | ns | |
| $t_{CSTO}$ | $\overline{CE}$ Access Time (Status Read) | – | 45 | ns | |
| $t_{RHW}$ | $\overline{RE}$ High to $\overline{WE}$ Low | 0 | – | ns | |
| $t_{WHC}$ | $\overline{WE}$ High to $\overline{CE}$ Low | 30 | – | ns | |
| $t_{WHR}$ | $\overline{WE}$ High to $\overline{RE}$ Low | 30 | – | ns | |
| $t_{AR1}$ | ALE Low to $\overline{RE}$ Low (ID Read) | 100 | – | ns | |
| $t_{CR}$ | $\overline{CE}$ Low to $\overline{RE}$ Low (ID Read) | 100 | – | ns | |
| $t_R$ | Memory Cell Array to Starting Address | – | 10 | $\mu s$ | |
| $t_{WB}$ | $\overline{WE}$ High to Busy | – | 200 | ns | |
| $t_{AR2}$ | ALE Low to $\overline{RE}$ Low (Read Cycle) | 50 | – | ns | |
| $t_{RB}$ | $\overline{RE}$ Last Clock Rising Edge to Busy (in Sequential Read) | – | 200 | ns | |
| $t_{CRY}$ | $\overline{CE}$ High to Ready (in Case of Interception by $\overline{CE}$ in Read Mode) | – | 50 + tr (R/$\overline{B}$) | ns | (2) |
| $t_{RST}$ | Device Resetting Time (Read/Program/Erase) | – | 6/10/500 | $\mu s$ | |

## AC TEST CONDITIONS

| | | |
|---|---|---|
| Input level | : | 2.4V/0.4V($V_{CC}$=3.3V±0.3V) |
| | | 3.4V/0.4V($V_{CC}$>3.6V) |
| Input comparison level | : | 1.5 V / 1.5 V |
| Output data comparison level | : | 1.5 V / 1.5 V |
| Output load | : | 1TTL & $C_L$ (100 pF) |

(1) Transition time ($t_T$) = 5 ns

(2) $\overline{CE}$ High to Ready time depends on the pull-up resistor tied to the R/$\overline{B}$ pin. (Refer to Application Note (10) toward the end of this document.)

(3) If the delay between $\overline{RE}$ and $\overline{CE}$ is less than 200 ns and $t_{CEH}$ is greater than or equal to 100 ns, reading will stop.
If the $\overline{RE}$-to-$\overline{CE}$ delay is less than 30 ns, the device will not turn to the Busy state.



## PROGRAMMING AND ERASING CHARACTERISTICS
(TC58V32AFT : Ta = 0° to 70 °C, $V_{CC}$ = 3.0 V to 5.5 V)
(TC58V32ADC　　: Ta = 0° to 55 °C, $V_{CC}$ = 3.3 V ± 0.3 V)

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|
| $t_{PROG}$ | Average Programming Time | | 300 | 1000 | $\mu s$ | |
| N | Number of Programming Cycles on Same Page | | | 10 | | (1) |
| $t_{BERASE}$ | Block Erasing Time | | 2 | 30 | ms | |
| P/E | Number of Program/Erase Cycles | | | $1 \times 10^6$ | | (2) |

(1) Refer to Application Note (11) toward the end of this document.
(2) Refer to Application Note (14) toward the end of this document.

## TIMING DIAGRAMS

Latch Timing Diagram for Command/Address/Data
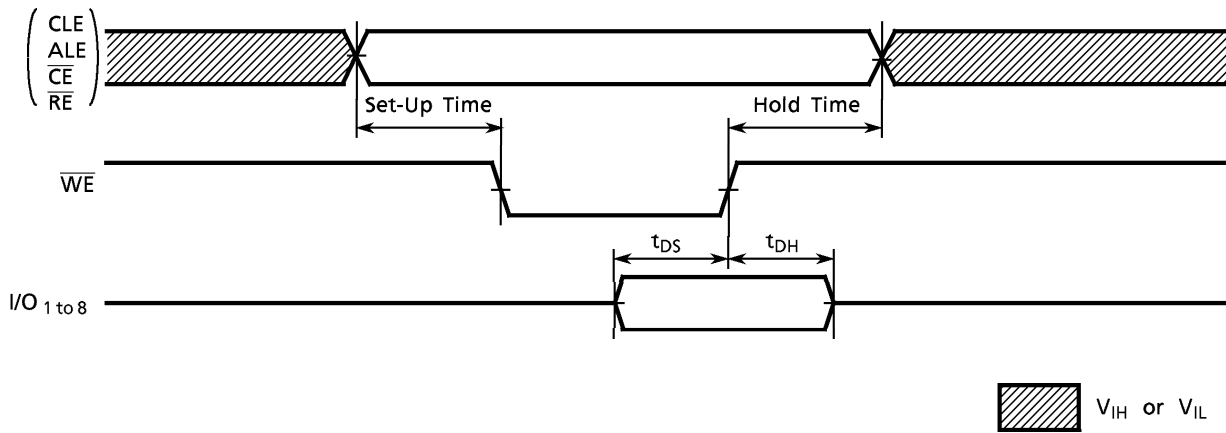


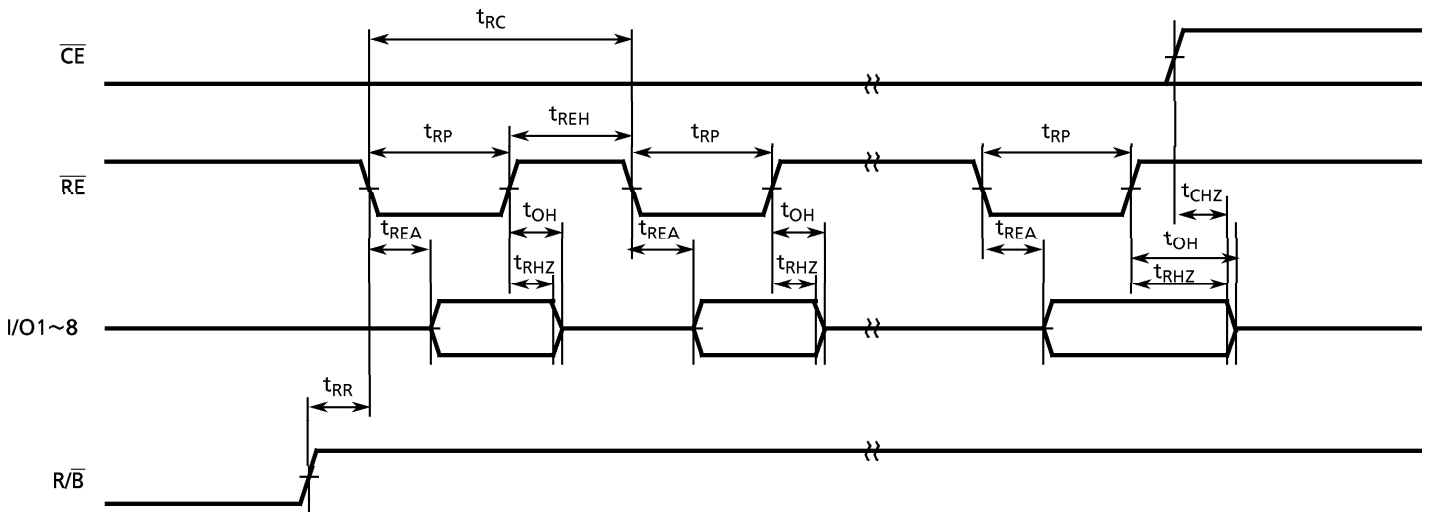Command Input Cycle Timing Diagram
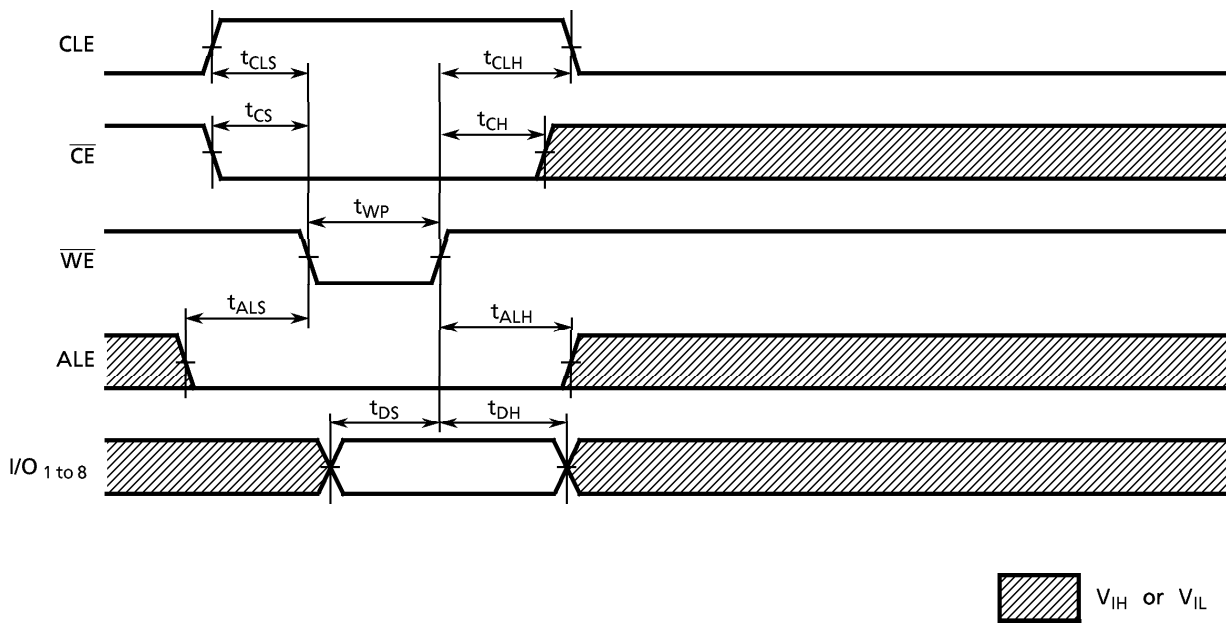
## Address Input Cycle Timing Diagram



$$V_{IH} \text{ or } V_{IL}$$
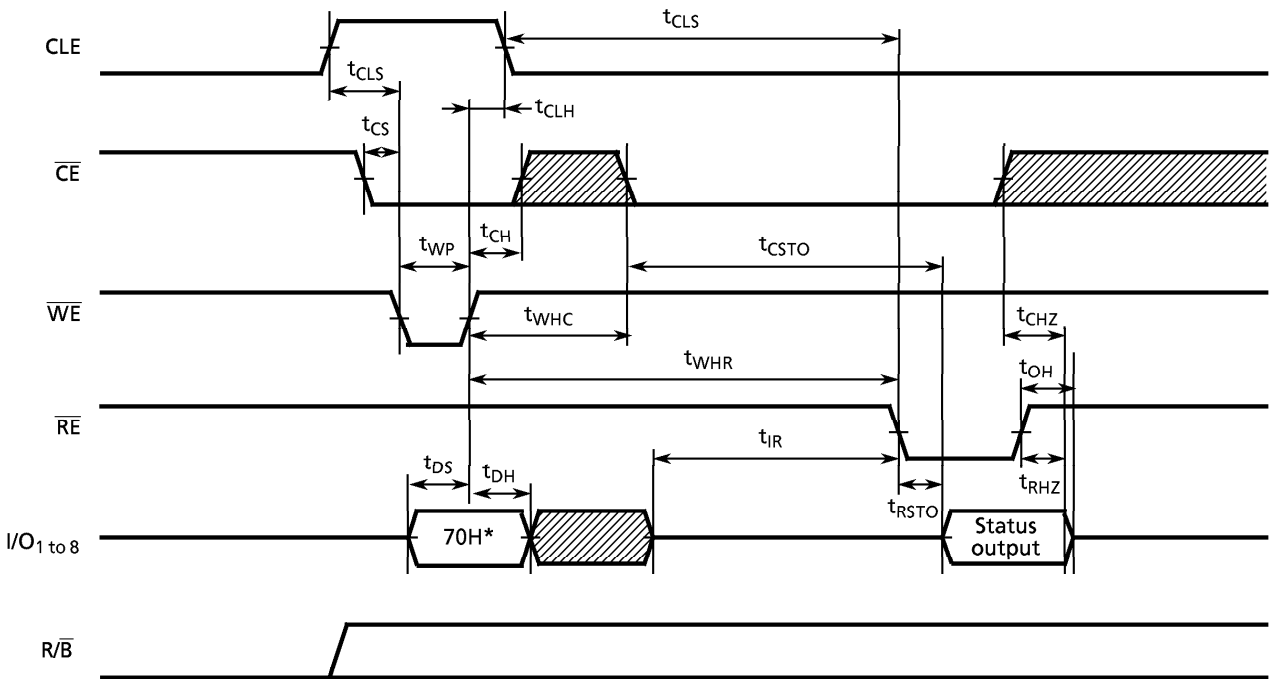
## Data Input Cycle Timing Diagram



*OP = GND input: $D_{IN}$ 527
= $V_{CC}$ input : $D_{IN}$ 511
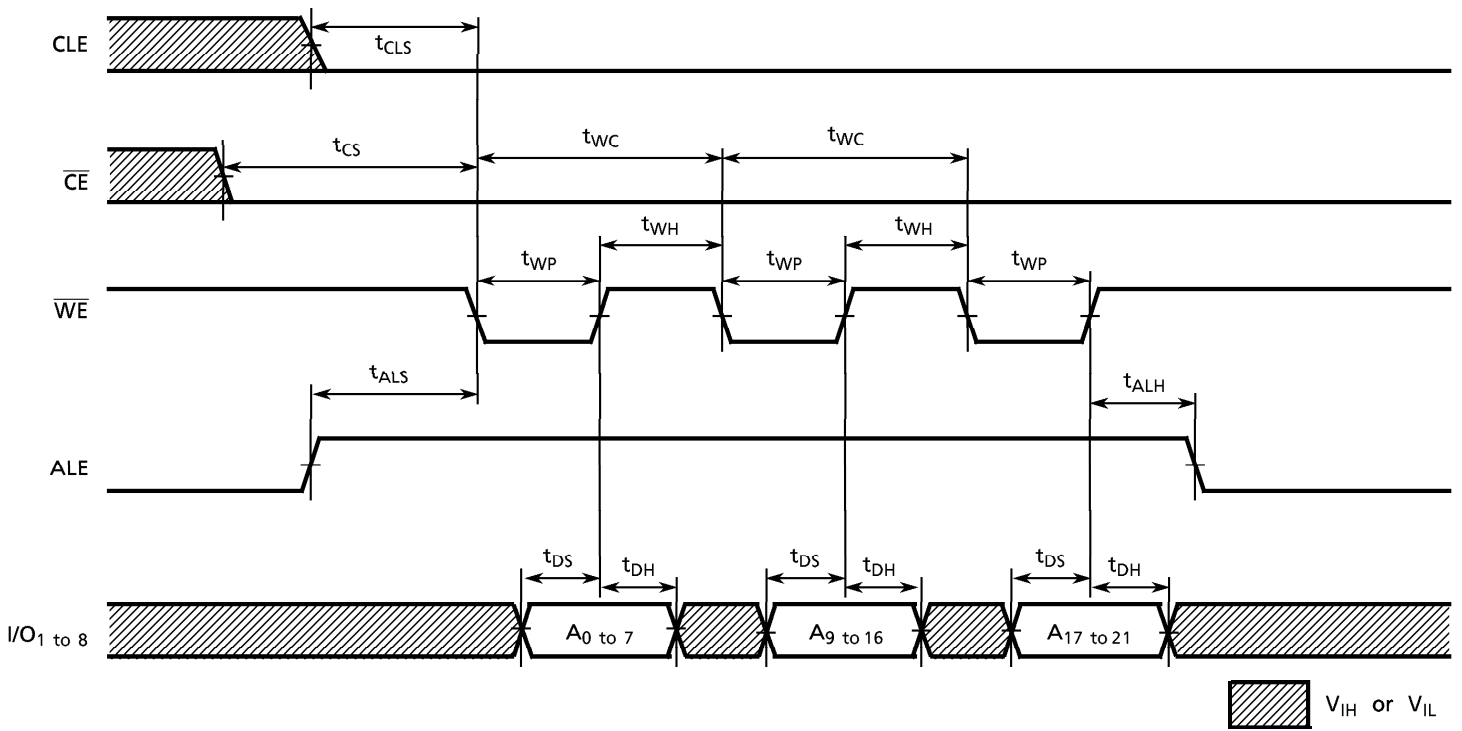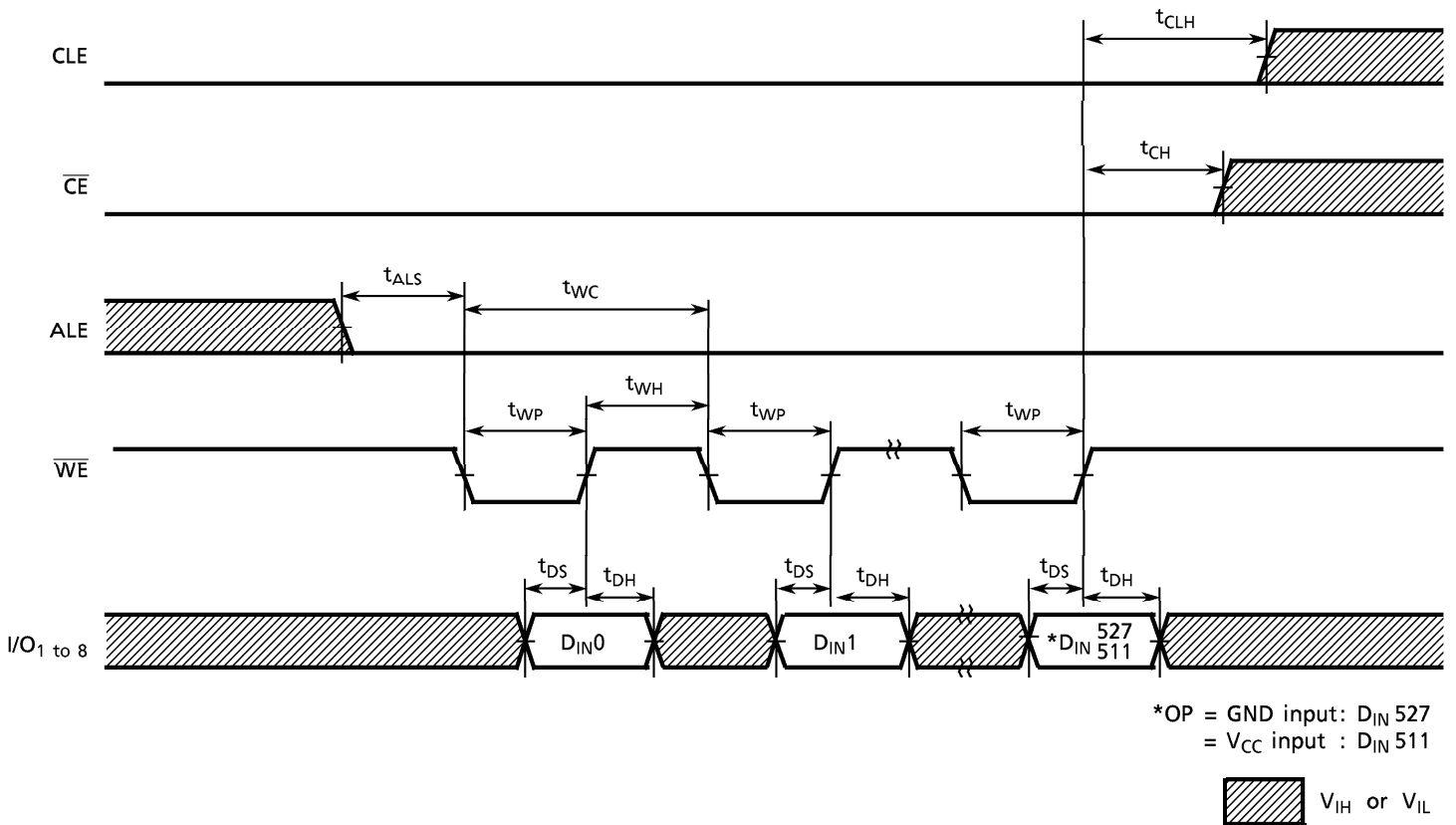
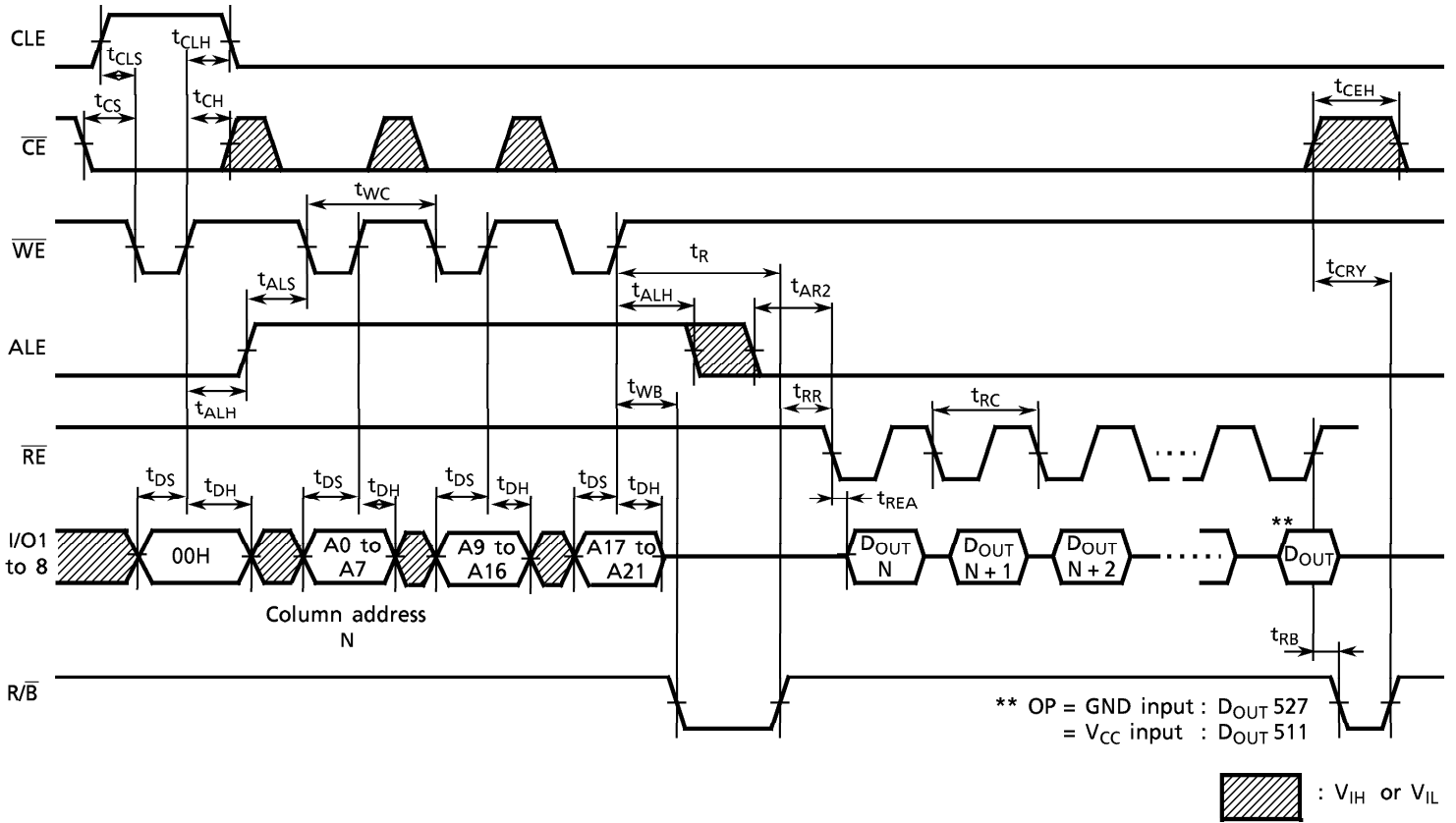$$V_{IH} \text{ or } V_{IL}$$

Serial Read Cycle Timing Diagram



Status Read Cycle Timing Diagram



* 70H - 70 in HEX data

: $V_{IH}$ or $V_{IL}$

## Read Cycle (1) Timing Diagram



** OP = GND input : $D_{OUT}$ 527
= $V_{CC}$ input : $D_{OUT}$ 511

□ : $V_{IH}$ or $V_{IL}$

## Read Cycle (1) Timing Diagram: Interrupted by $\overline{CE}$



*** Read Operation using 00H Command    N: 0 to 255
Read Operation using 01H Command    N: 256 to 511

□ : $V_{IH}$ or $V_{IL}$
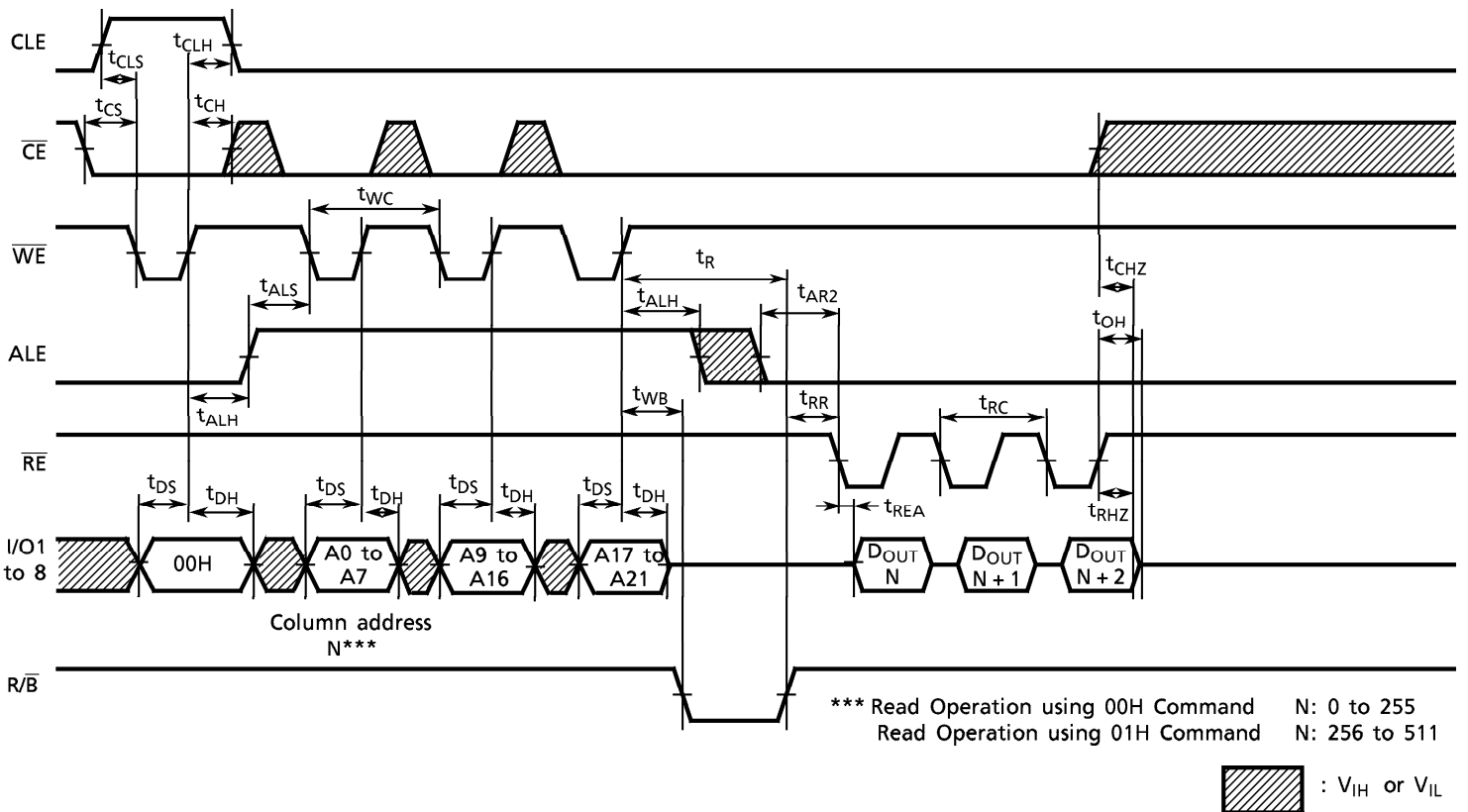
## Read Cycle (2) Timing Diagram



**OP = GND input: $D_{OUT}$ 527
= $V_{CC}$ input : $D_{OUT}$ 511

: $V_{IH}$ or $V_{IL}$
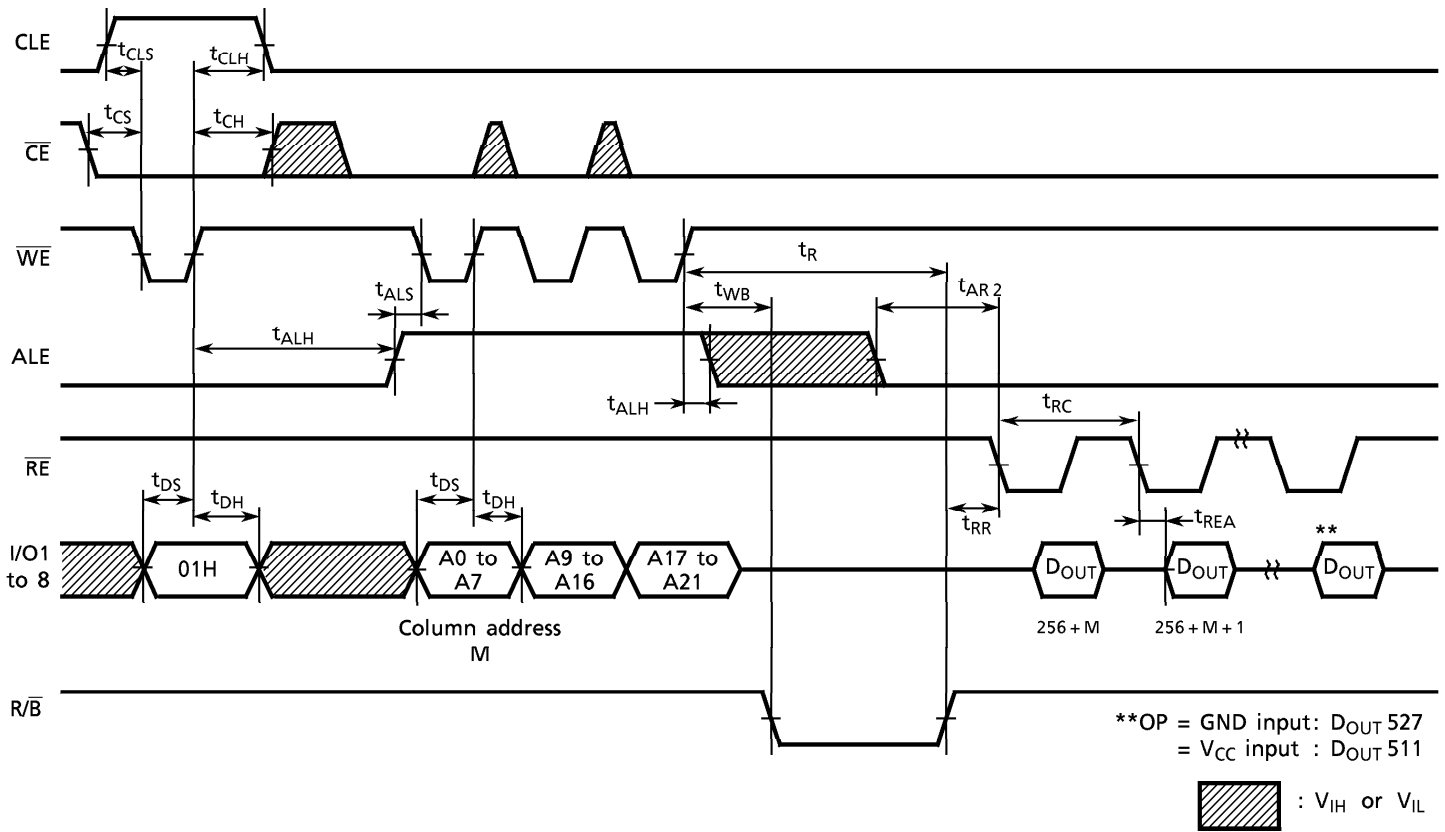
## Read Cycle (3) Timing Diagram



**OP = GND input: $D_{OUT}$ 527
Do not input $V_{CC}$

: $V_{IH}$ or $V_{IL}$
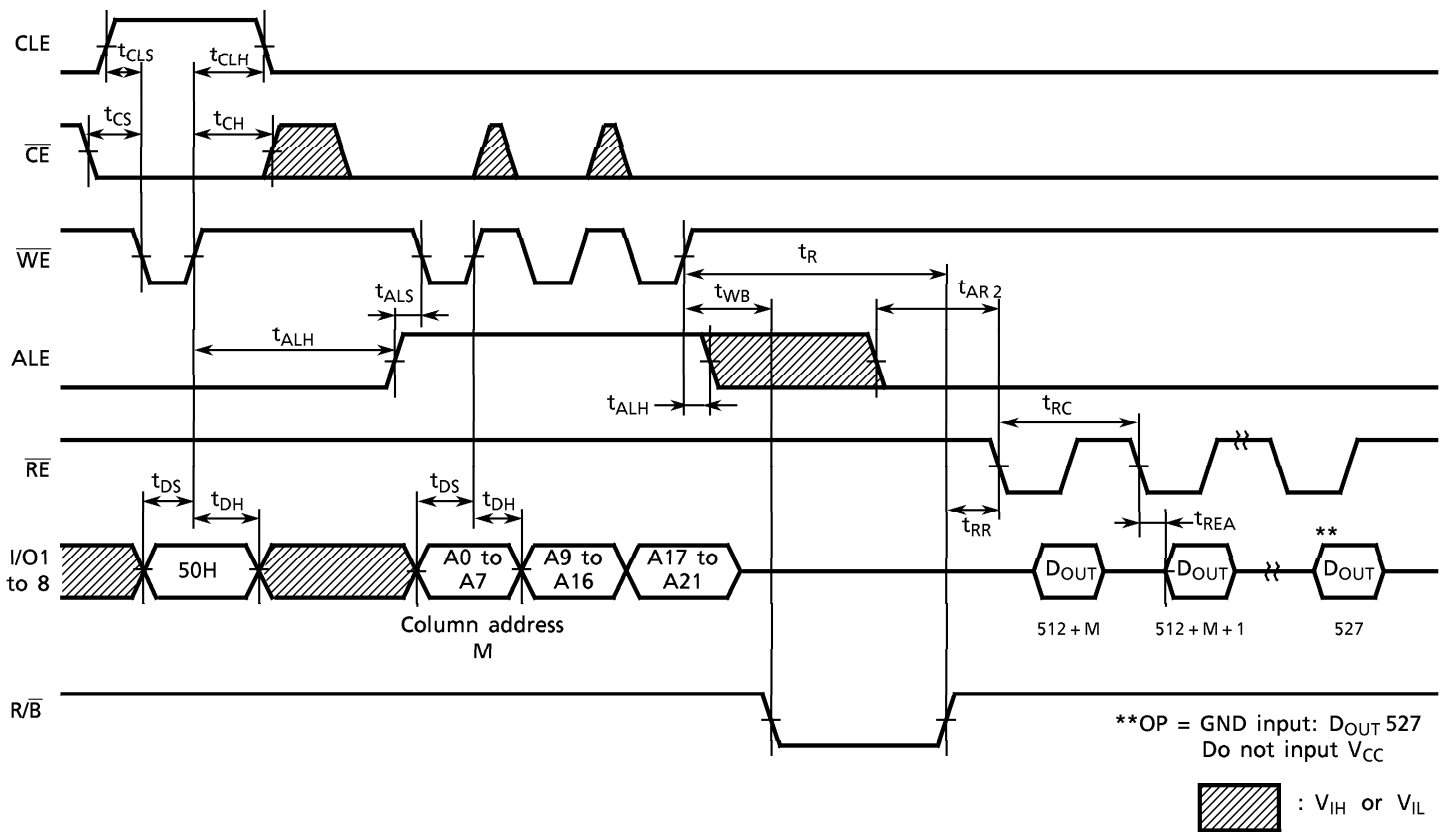
## Sequential Read (1) Timing Diagram

CLE

CE

WE

ALE

RE

I/O1 to 8

00H · A0 to A7 · A9 to A16 · A17 to A21 · N · N+1 · N+2 · ** · 0 · 1 · 2 · **

Column address N

Page address M

$t_R$

$t_R$

R/B

Page M access

Page M+1 access

**OP = GND input : $D_{OUT}$ 527
= $V_{CC}$ input : $D_{OUT}$ 511

: $V_{IH}$ or $V_{IL}$
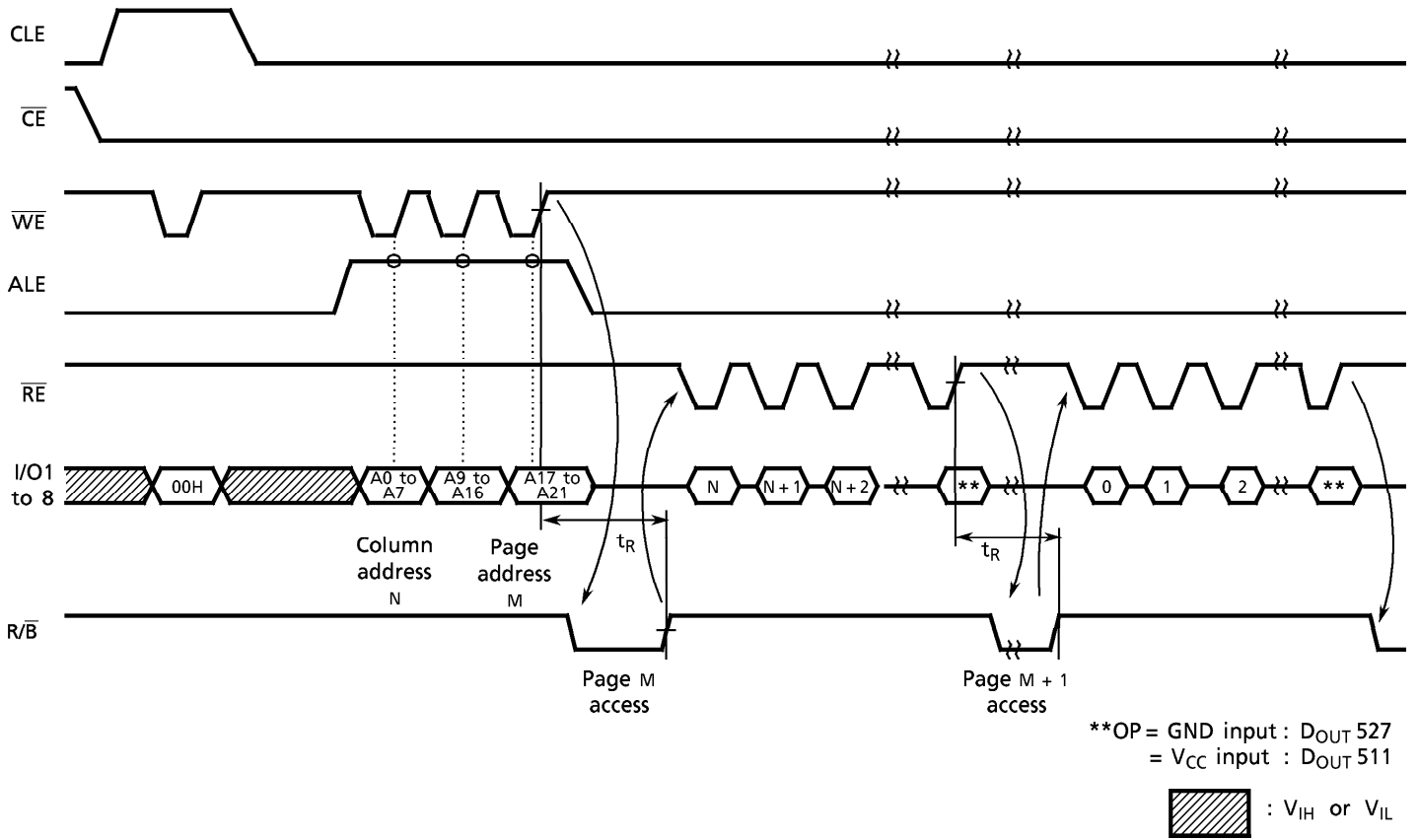
## Sequential Read (2) Timing Diagram

CLE

CE

WE

ALE

RE

I/O1 to 8

01H · A0 to A7 · A9 to A16 · A17 to A21 · ** · 0 · 1 · 2 · **

Column address N

Page address M

$t_R$

$t_R$

256 + N · 256 + N+1 · 256 + N+2

R/B

Page M access

Page M+1 access

**OP = GND input : $D_{OUT}$ 527
= $V_{CC}$ input : $D_{OUT}$ 511

: $V_{IH}$ or $V_{IL}$
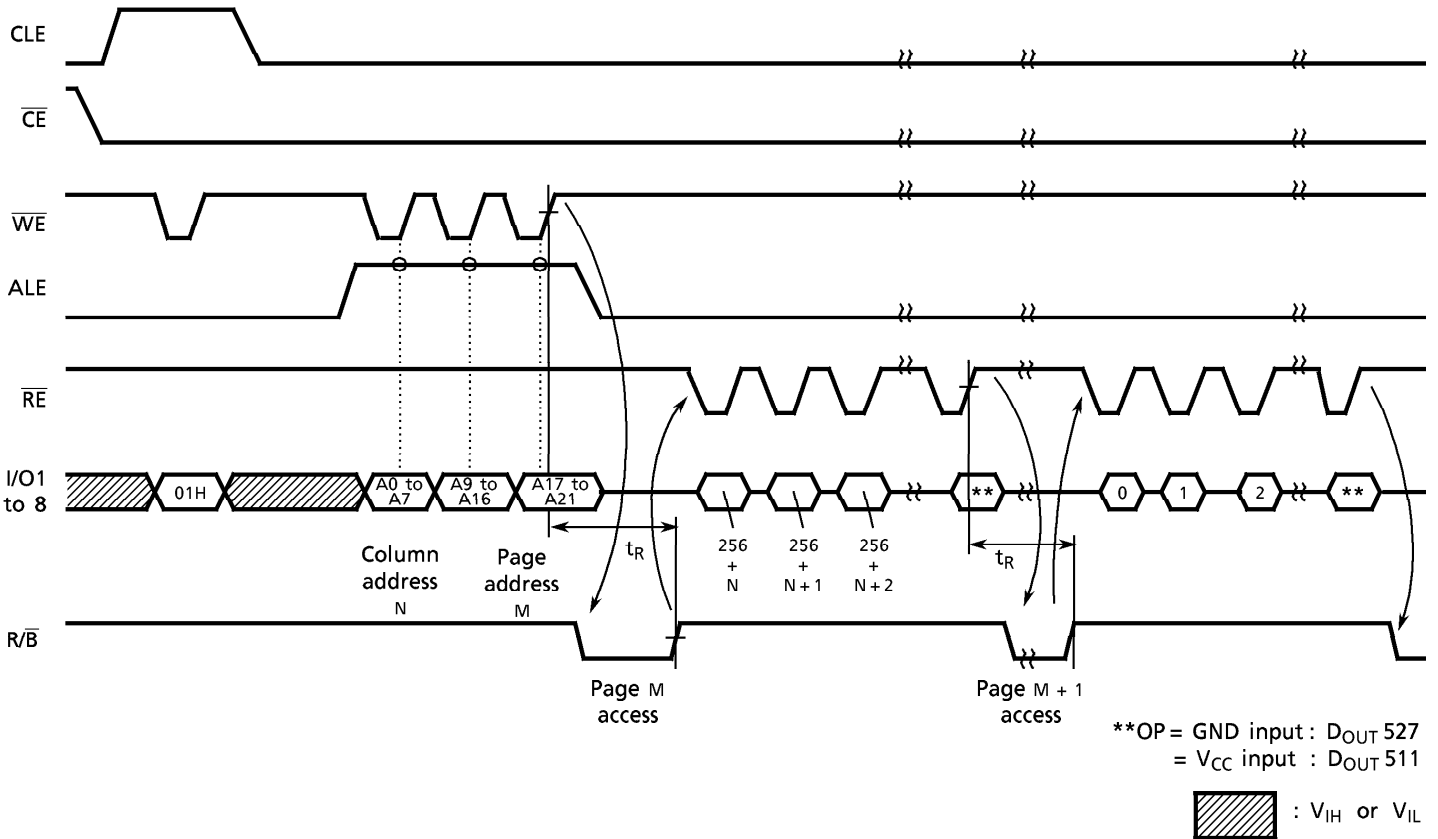
Sequential Read (3) Timing Diagram



**OP = GND input : $D_{OUT}$ 527
= Do not input $V_{CC}$

: $V_{IH}$ or $V_{IL}$
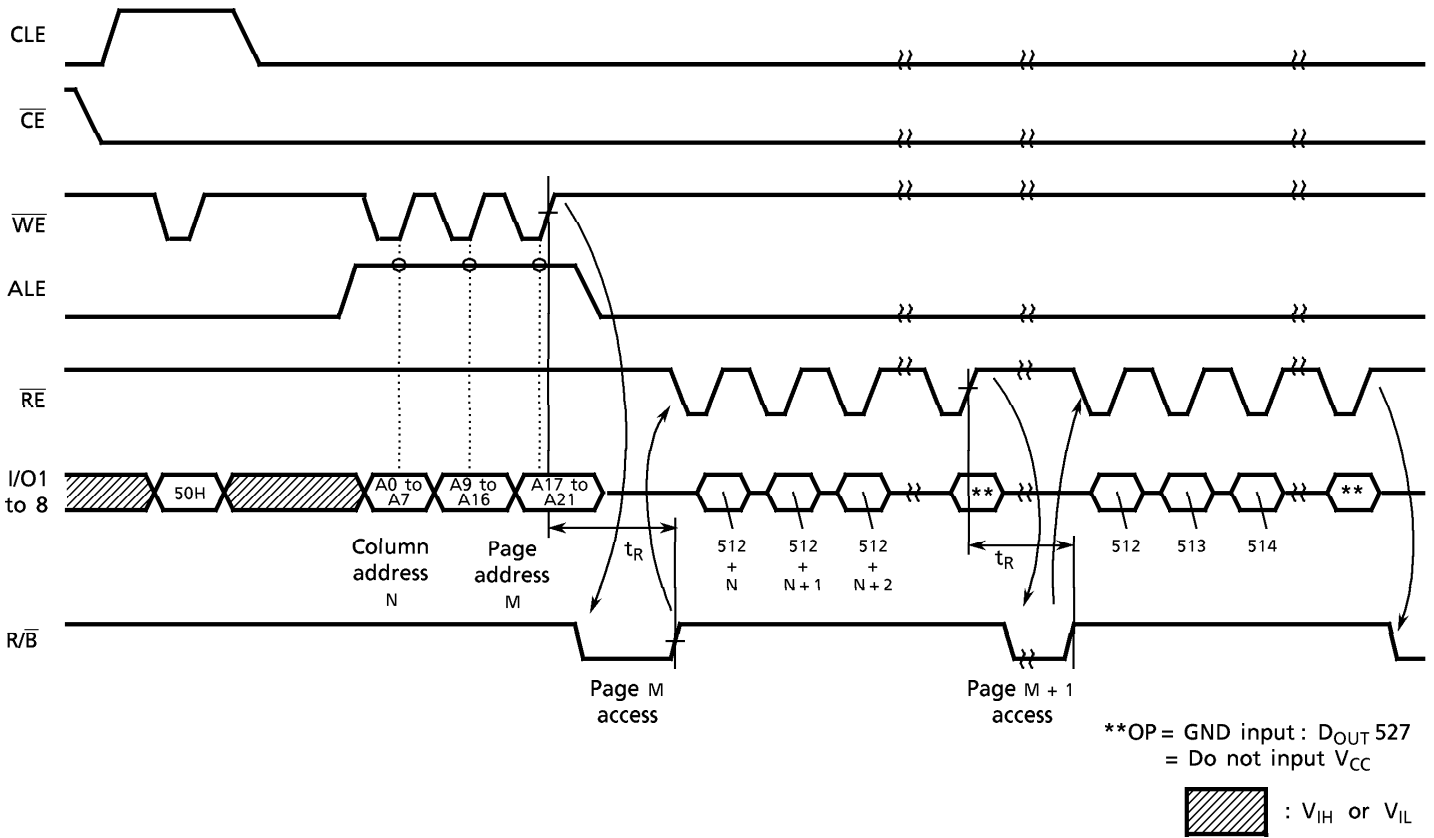
## Auto Program Operation Timing Diagram



*OP = GND input: $D_{IN}$ 527
= $V_{CC}$ input : $D_{IN}$ 511

▨ : $V_{IH}$ or $V_{IL}$    ▦ : If data is being output, do not allow any input.
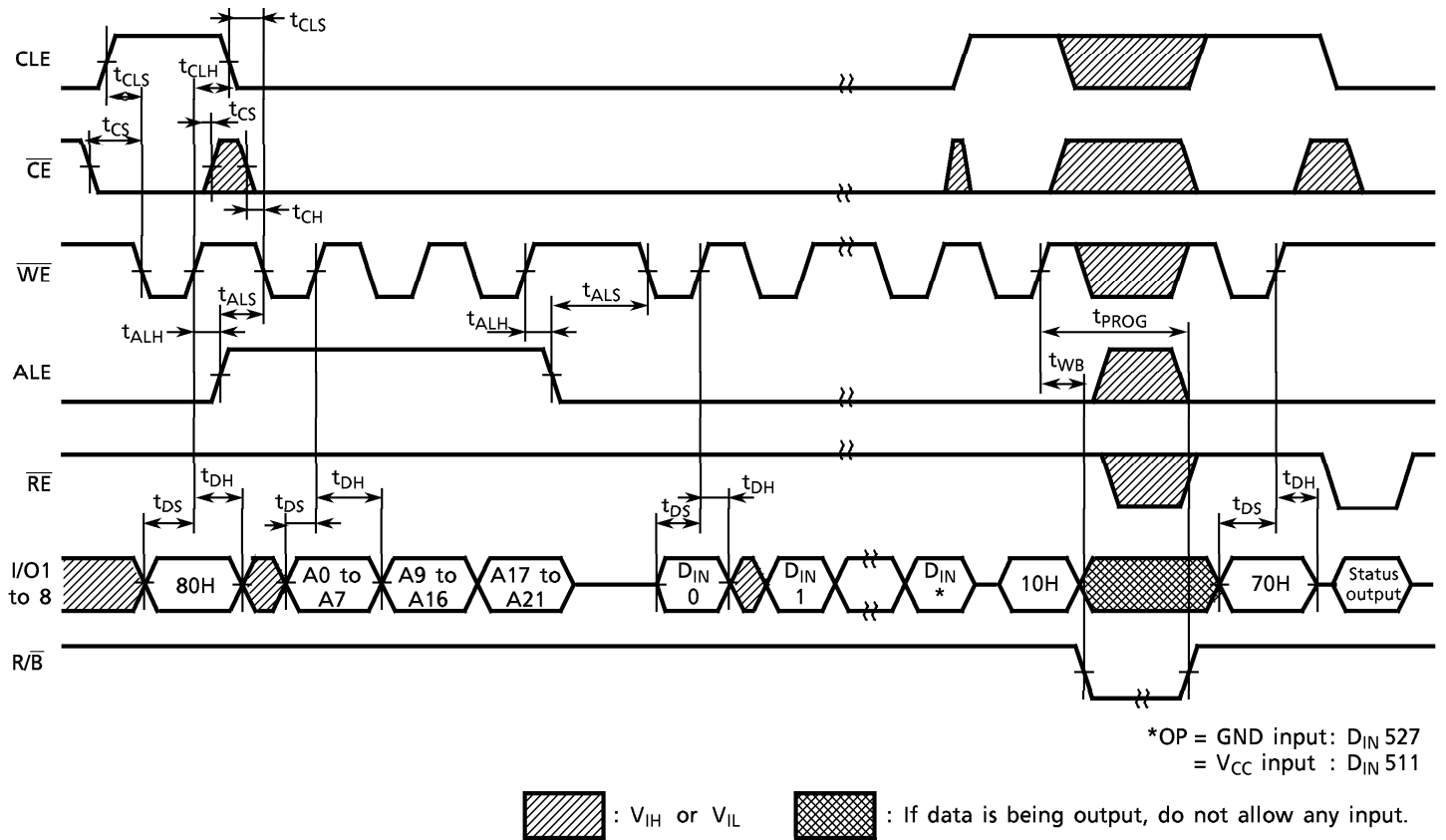
## Auto Block Erase Timing Diagram



Auto Block Erase
Set-Up
command

Erase Start
command

Status Read
command

▨ : $V_{IH}$ or $V_{IL}$    ▦ : If data is being output, do not allow any input.
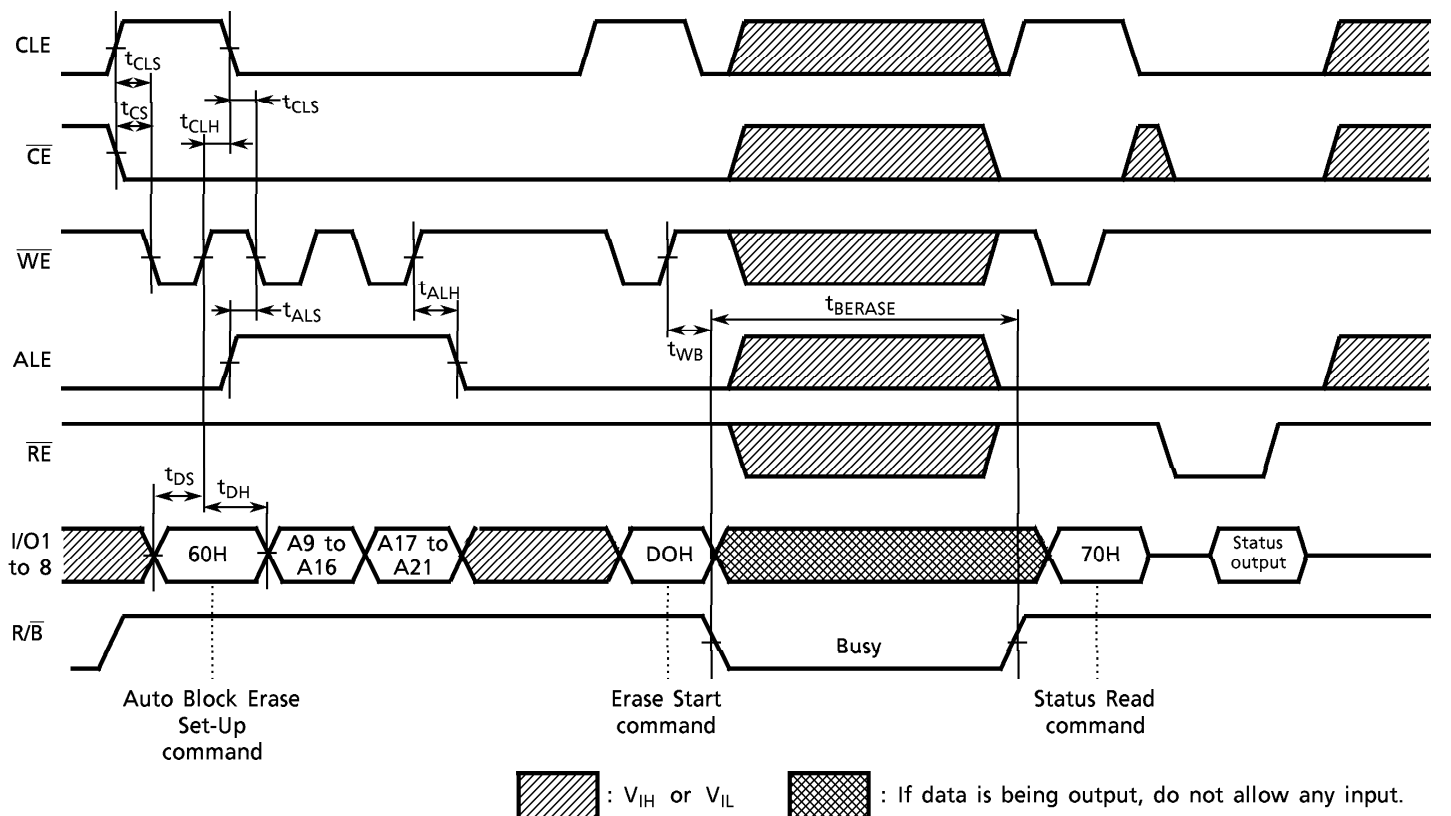
ID Read Operation Timing Diagram



Address input          Maker code     Device code

▨ : $V_{IH}$ or $V_{IL}$
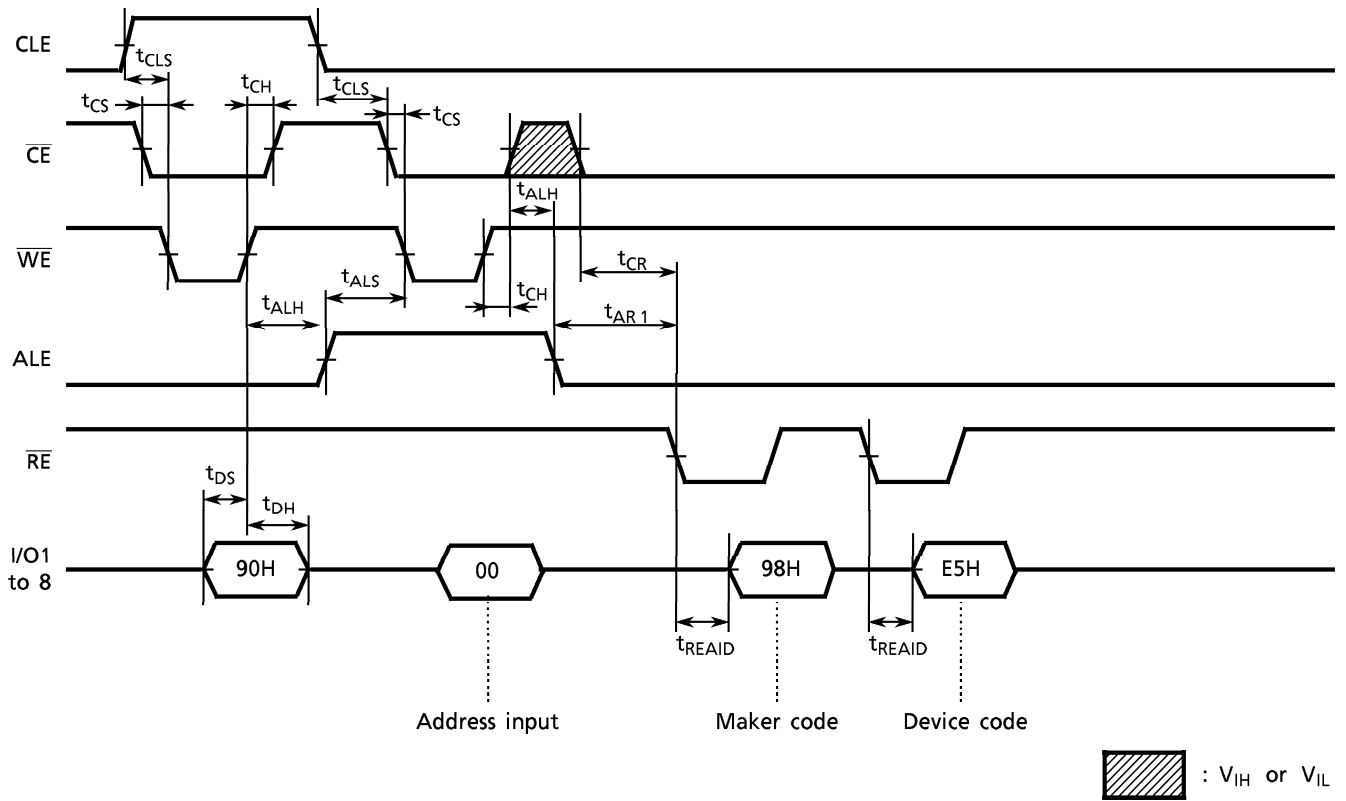
## PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

Command Latch Enable: CLE

The CLE input signal is used to control the acquisition of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is high.

Address Latch Enable: ALE

The ALE signal is used to control the acquisition of either address information or input data into the internal address/data resistor. Address information is latched on the rising edge of $\overline{WE}$ if ALE is high. Input data is latched if ALE is low.

Chip Enable: $\overline{CE}$

The device goes into a low power standby mode during a Read operation when $\overline{CE}$ goes high. The $\overline{CE}$ signal is ignored when the device is in the Busy state ($R/\overline{B}$ = L), such as during a Program or Erase operation, and will not go into Standby mode even if a $\overline{CE}$ goes high input. The $\overline{CE}$ pin must stay low during the Read mode Busy state to ensure that memory signal array data is correctly transferred to the data register.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available $t_{REA}$ after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address + 1) on this falling edge.

I/O Port: I/O 1 to 8

The I/O 1 to 8 pins are used as the port for transferring address, command and input/output data to or from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is low. This signal is usually used for protecting the data during the power on/off sequence when input signals are invalid.

Ready/Busy: $R/\overline{B}$

The $R/\overline{B}$ output signal is used to indicate the operating condition of the device. The $R/\overline{B}$ signal is in the Busy state ($R/\overline{B}$ = L) during the Program, Erase or Read operations and will return to Ready state ($R/\overline{B}$ = H) after completion of the operation. The output buffer for this signal is an open drain.

Option Pin: OP

The OP signal is used to change the page size. The device is in 528 byte/page mode when OP = GND, and 512 byte/page mode when OP = $V_{CC}$.

Low Voltage Detect: LVD

The LVD is used to detect the proper supply voltage. By connecting this pin to $V_{SS}$ through a pull-down resistor, it is possible to distinguish 3.3V product (TC58V32DC) from 5V product (TC5832DC). When 3.3V is applied as $V_{CC}$ to pins 12 and 22, a "H" level can be detected on the system side if the device is a 3.3V product, and "L" level for a 5V product.
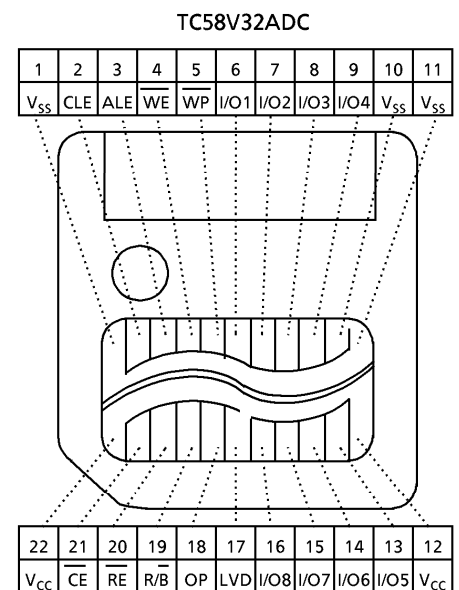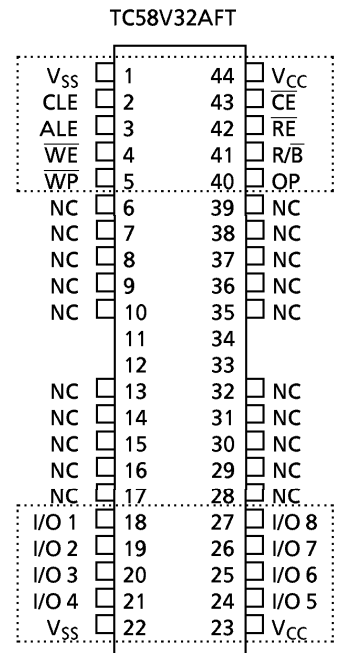
TC58V32AFT

| | | | |
|---|---|---|---|
| $V_{SS}$ | 1 | 44 | $V_{CC}$ |
| CLE | 2 | 43 | $\overline{CE}$ |
| ALE | 3 | 42 | $\overline{RE}$ |
| $\overline{WE}$ | 4 | 41 | $R/\overline{B}$ |
| $\overline{WP}$ | 5 | 40 | OP |
| NC | 6 | 39 | NC |
| NC | 7 | 38 | NC |
| NC | 8 | 37 | NC |
| NC | 9 | 36 | NC |
| NC | 10 | 35 | NC |
| | 11 | 34 | |
| | 12 | 33 | |
| NC | 13 | 32 | NC |
| NC | 14 | 31 | NC |
| NC | 15 | 30 | NC |
| NC | 16 | 29 | NC |
| NC | 17 | 28 | NC |
| I/O 1 | 18 | 27 | I/O 8 |
| I/O 2 | 19 | 26 | I/O 7 |
| I/O 3 | 20 | 25 | I/O 6 |
| I/O 4 | 21 | 24 | I/O 5 |
| $V_{SS}$ | 22 | 23 | $V_{CC}$ |

TC58V32ADC

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{SS}$ | CLE | ALE | $\overline{WE}$ | $\overline{WP}$ | I/O1 | I/O2 | I/O3 | I/O4 | $V_{SS}$ | $V_{SS}$ |



| 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $\overline{CE}$ | $\overline{RE}$ | $R/\overline{B}$ | OP | LVD | I/O8 | I/O7 | I/O6 | I/O5 | $V_{CC}$ |

Figure 1. Pinout

## Schematic Cell Layout and Address Assignment

The Program operation is implemented in a page units while the Erase operation is carried out in block units.
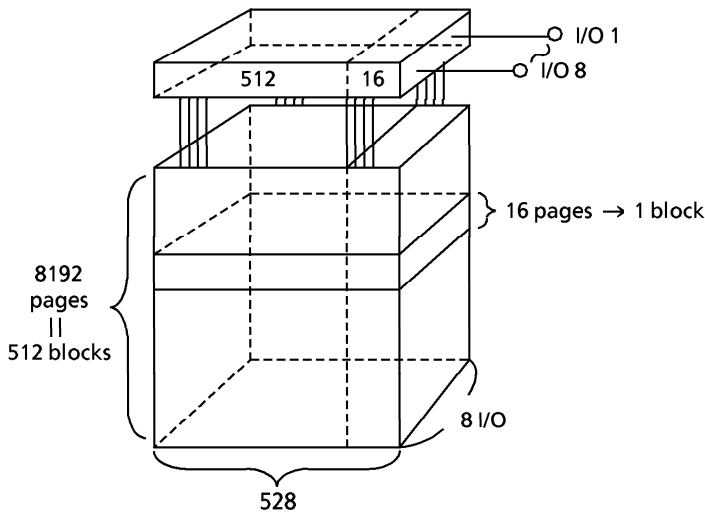


Figure 2. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are for main memory and 16 bytes are for redundancy or other uses.

1 Page = 528 bytes
1 Block = 528 bytes × 16 pages = (8 K + 256) bytes
Total Device Density = 528 bytes × 16 pages × 512 blocks

The address is acquired through the I/O port over three consecutive clock cycles, as shown in Table 1.

Table 1.  Addressing

|  | I/O 1 | I/O 2 | I/O 3 | I/O 4 | I/O 5 | I/O 6 | I/O 7 | I/O 8 |
|---|---|---|---|---|---|---|---|---|
| First cycle | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 |
| Second cycle | A9 | A10 | A11 | A12 | A13 | A14 | A15 | A16 |
| Third cycle | A17 | A18 | A19 | A20 | A21 | * L | * L | * L |

A0 to A7   : column address
A9 to A21 : page address
( A13 to A21: block address )
( A9 to A12 : NAND address in block )

*: A8 is automatically set to "Low" or "High" by the "00H" command or a "01H" command in device inside.
*: I/O 6 to 8 must be set low in the third cycle.

## Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the eleven different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2.  Logic Table

|  | CLE | ALE | $\overline{CE}$ | $\overline{WE}$ | $\overline{RE}$ | $\overline{WP}$ |
|---|---|---|---|---|---|---|
| Command Input | H | L | L | ⌐_⌐ | H | * |
| Data Input | L | L | L | ⌐_⌐ | H | * |
| Address Input | L | H | L | ⌐_⌐ | H | * |
| Serial Data Output | L | L | L | H | ⌐_⌐ | * |
| During Programming (Busy) | * | * | * | * | * | H |
| During Erasing (Busy) | * | * | * | * | * | H |
| Program, Erase Inhibit | * | * | * | * | * | L |

H: $V_{IH}$,    L: $V_{IL}$,    *: $V_{IH}$ or $V_{IL}$

Table 3.  Command table (HEX data)

|  | FIRST CYCLE | SECOND CYCLE | ACCEPTABLE COMMAND WHILE BUSY |
|---|---|---|---|
| Serial Data Input | 80 | – | |
| Read Mode (1) | 00 | – | |
| Read Mode (2) | 01 | – | |
| Read Mode (3) | 50 | – | |
| Reset | FF | – | ○ |
| Auto Program | 10 | – | |
| Auto Block Erase | 60 | D0 | |
| Status Read | 70 | – | ○ |
| ID Read | 90 | – | |

Bit assignment of HEX data
(Example)

Serial data input: 80H

| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|

I/O 8  7  6  5  4  3  2  I/O 1
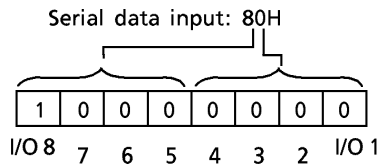
Once the device is set to Read mode by the "00H", "01H" or "50H" command, additional Read commands are not needed for sequential page Read operations. Table 4 shows the operation states for Read mode.

Table 4.  Read mode operation states

|  | CLE | ALE | $\overline{CE}$ | $\overline{WE}$ | $\overline{RE}$ | I/O 1 TO I/O 8 | POWER |
|---|---|---|---|---|---|---|---|
| Output Select | L | L | L | H | L | Data output | Active |
| Output Deselect | L | L | L | H | H | High impedance | Active |
| Standby | L | L | H | H | * | High impedance | Standby |

H : $V_{IH}$   L : $V_{IL}$     * : $V_{IH}$ or $V_{IL}$

## DEVICE OPERATION

### Read Mode (1)

Read mode (1) is set by issuing a '00H' command to the command register. Refer to Figure 3 below for timing details and block diagram.



Figure 3. Read mode (1) operation

A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the third cycle (after the address information has been latched.) The device will be in the Busy state during this transfer period. The $\overline{CE}$ signal must stay low after the third address input and during the Busy state.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the starting pointer designated in the address input cycle.

### Read Mode (2)



Figure 4. Read mode (2) operation

The operation of the device after input of the "01H" command is the same as Read Mode (1). To set the starting pointer is to be set after column address 256, use Read Mode (2).

For a Sequential Read, output of the next page starts from column address 0.

### Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The starting pointer is therefore assigned between bytes 512 and 527.
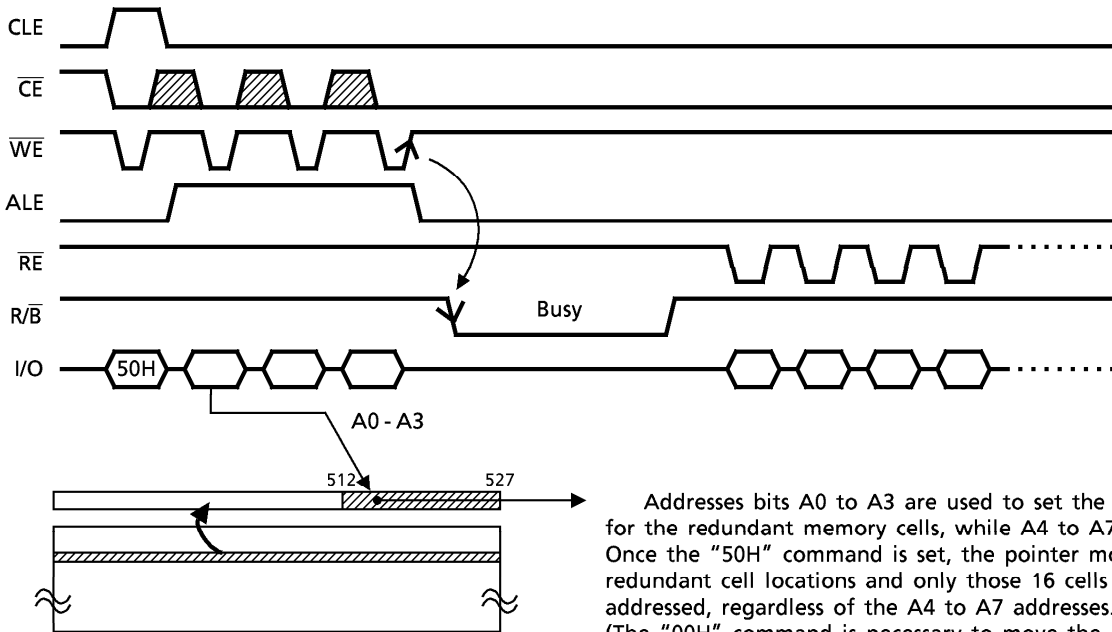
Figure 5. Read mode (3) operation

Addresses bits A0 to A3 are used to set the starting pointer for the redundant memory cells, while A4 to A7 are ignored. Once the "50H" command is set, the pointer moves to the redundant cell locations and only those 16 cells can be addressed, regardless of the A4 to A7 addresses.
(The "00H" command is necessary to move the pointer back to the 0 to 511 main memory cell locations.)
Read mode (3) operation is invalid when OP is at the $V_{CC}$ level.

Sequential Read (1)(2)(3)

This mode allows the sequential reading of pages without additional address input.



Sequential Read (1)          Sequential Read (2)          Sequential Read (3)
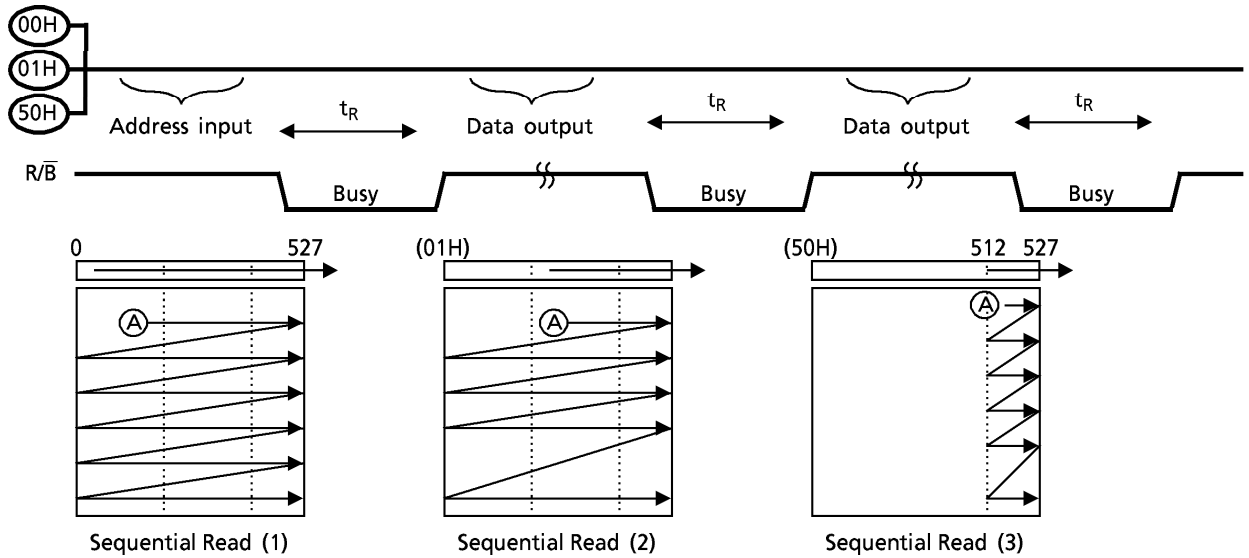
Sequential Read modes (1) and (2) output addresses 0 to 527 as shown above while Sequential Read mode (3) outputs the redundant address locations only. When the pointer reaches the last address, the device continues to output the data from this address ** on each $\overline{RE}$ clock signal.

** OP = GND : column address 527.
$\quad\quad\quad$ $V_{CC}$ : column address 511.

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the pass/fail result of a Program or Erase operation, and determine if the device is in Suspend or Protect mode. The device status is output through the I/O port using the $\overline{RE}$ clock after a "70H" command input. The resulting information is outlined in Table 5.

Table 5.  Status output table

|  | STATUS | OUTPUT | |
|---|---|---|---|
| I/O 1 | Pass / Fail | Pass : '0' | Fail : '1' |
| I/O 2 | Not used | '0' | |
| I/O 3 | Not used | '0' | |
| I/O 4 | Not used | '0' | |
| I/O 5 | Not used | '0' | |
| I/O 6 | Not used | '0' | |
| I/O 7 | Ready / Busy | Ready : '1' | Busy : '0' |
| I/O 8 | Write protect | Protect :'0' | Not Protect : '1' |

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.
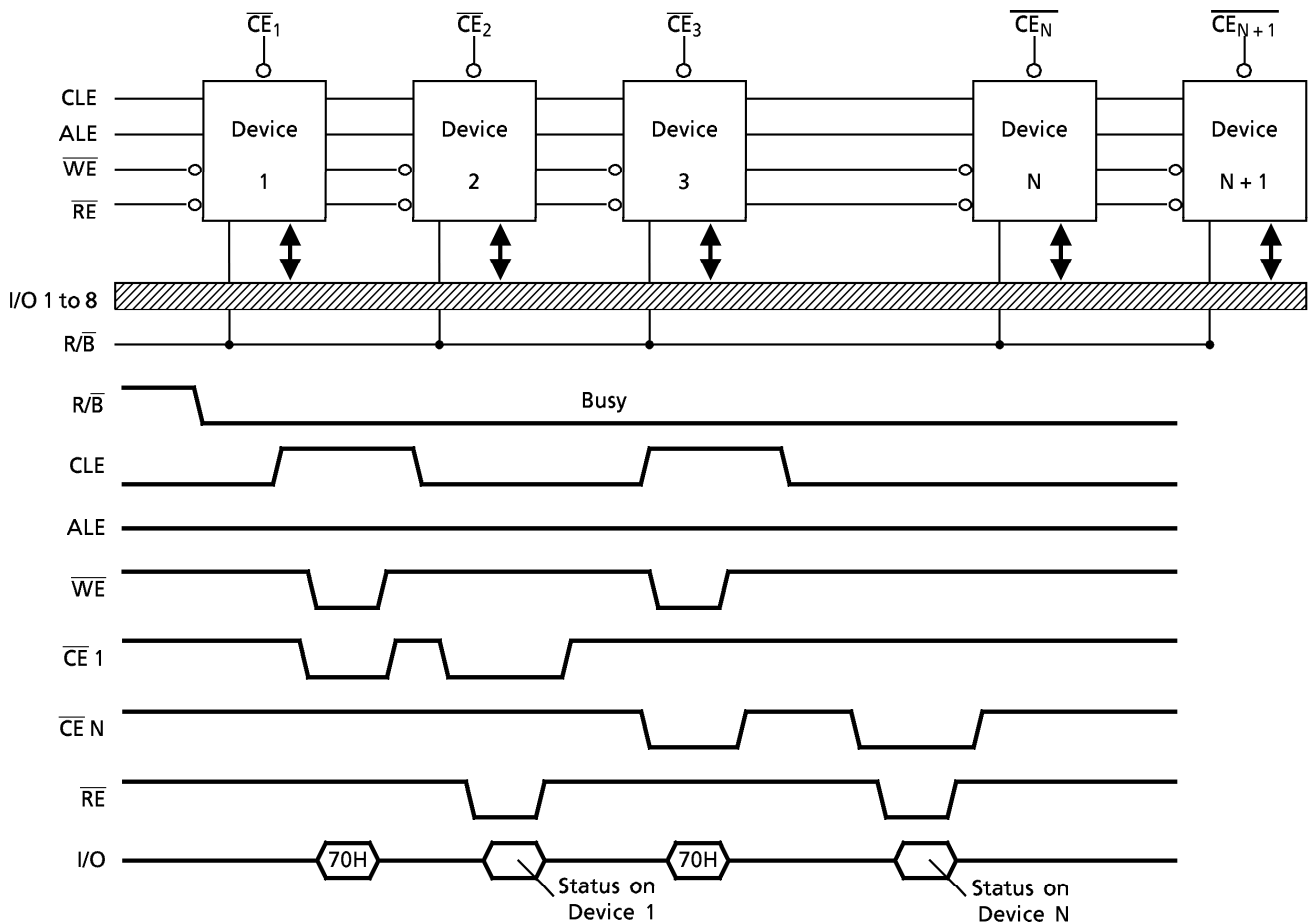


Figure 6.  Status read timing application example

SYSTEM DESIGN NOTE : If the $R/\overline{B}$ pin signals of multiple devices are common-wired as shown in the diagram, the Status Read Function can be used to determine the status of each individually selected

## Auto Page Program

The device implements the Automatic Page Program operation after receiving a "10H" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



Data Input command — Address input — Data input 0 to 527 When OP = GND, 0 to 511 When OP = V$_{CC}$ — Program command (10) — Status Read command (70) — I/O — Pass / Fail

R/B̄    R/B̄ automatically returns to Ready after completion.

Data input — Program — Read & Verification
Selected page
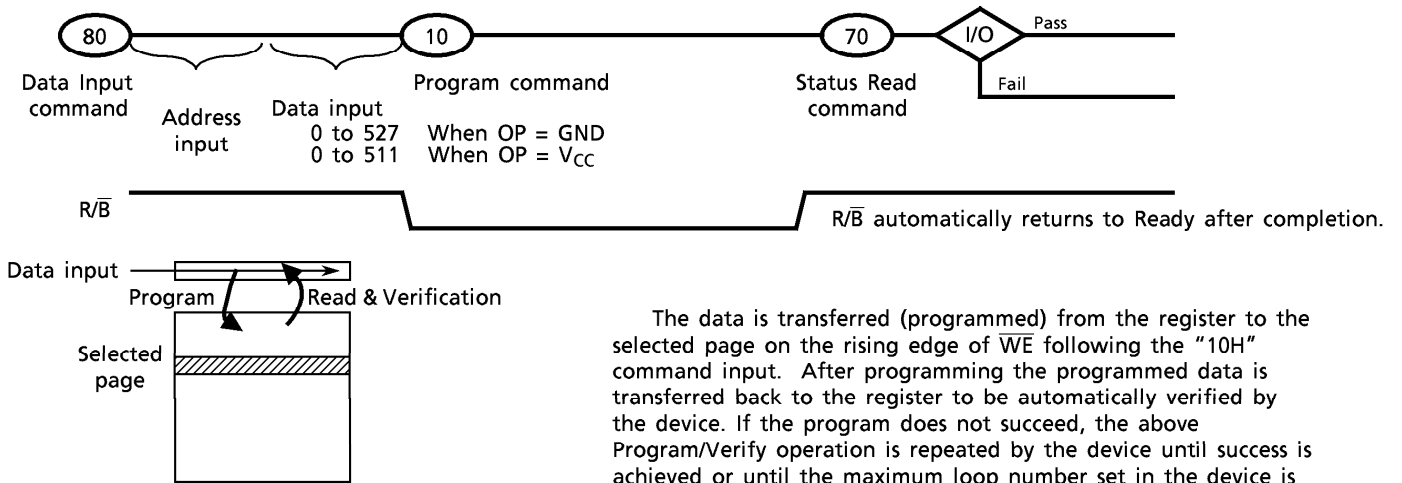
Figure 7. Auto Page Program operation

The data is transferred (programmed) from the register to the selected page on the rising edge of $\overline{WE}$ following the "10H" command input. After programming the programmed data is transferred back to the register to be automatically verified by the device. If the program does not succeed, the above Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

## Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Execution command "D0H" which follows the Erase Set-Up command "60H". This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



60 — Block address input : 2 cycles — D0 Erase Start command — 70 Status Read command — I/O — Pass / Fail

R/B̄    Busy
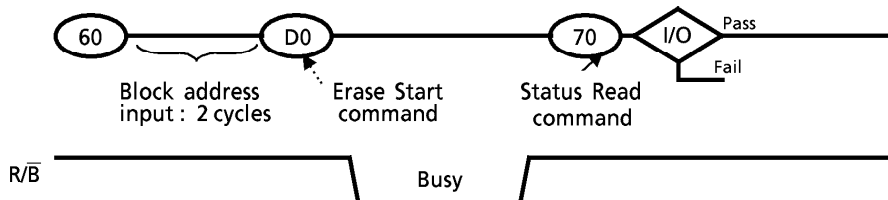
Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the regulated voltage is discharged to 0 volts and the device will go into Wait state. The address and data registers are set as follows after a Reset:

· Address Register    :   All "0"
· Data Register       :   All "1"
· Operation Mode      :   Wait State

The response after an "FFH" Reset command is input during each operation is as follows:

① If the Reset (FFH) command is input during programming :                    Figure 8.
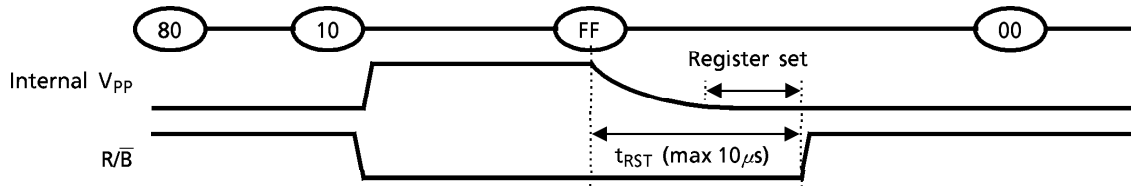


② If the Reset (FFH) command is input during erasing :                        Figure 9.
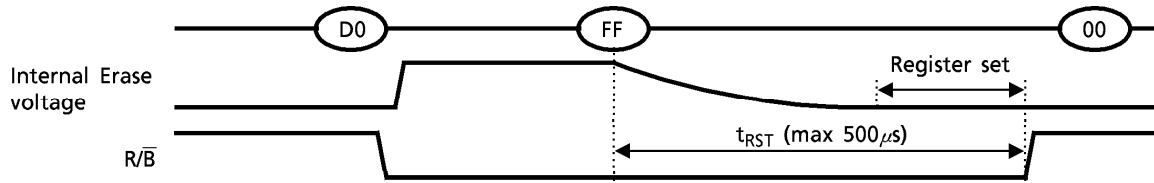


③ If the reset (FFH) command is input during a Read operation :               Figure 10.
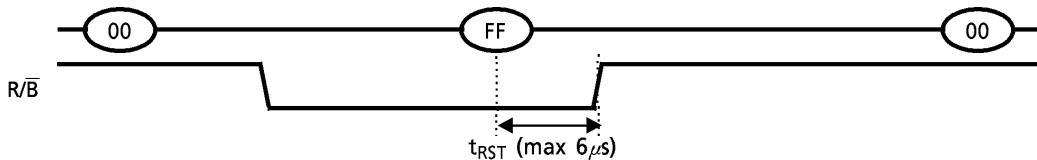


⑤ If the Status Read command (70H) is input after a Reset :                   Figure 11.



However, the following operation is prohibited. If the following operation is executed, set up for address and data register can not be guaranteed. (the Register may not be reset correctly)
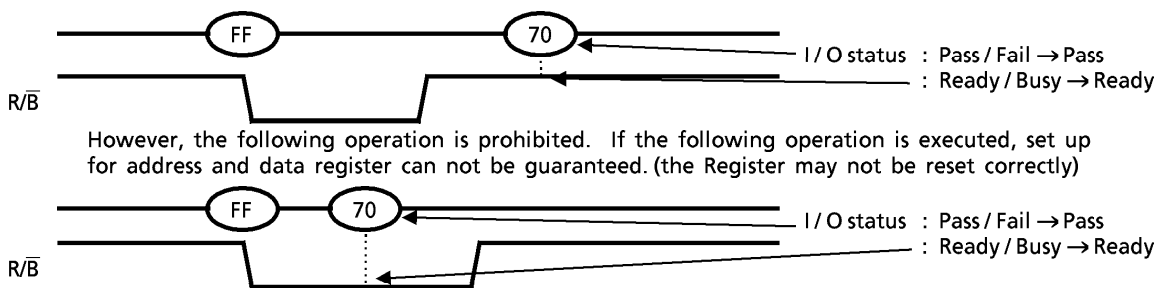


⑥ If the Reset command is input in succession :                              Figure 12.



The second $\overline{FF}$ command is invalid, but the third $\overline{FF}$ command is valid.
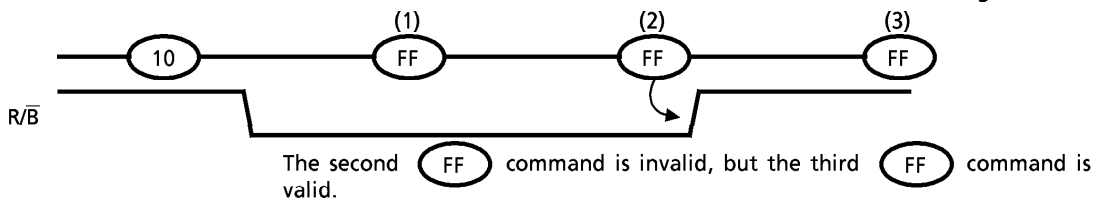
ID Read

The TC58V32AFT/ADC contains ID codes to identify the device type and the manufacturer. The ID codes are read out using the following timing conditions:
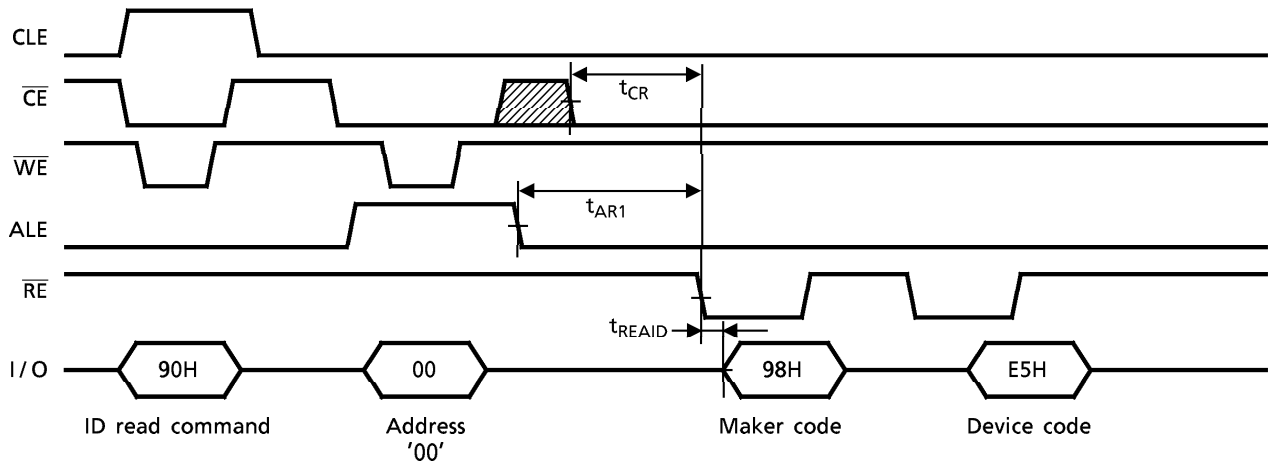


Figure 13. ID read timing

Table 6. Code table

|  | I/O 8 | I/O 7 | I/O 6 | I/O 5 | I/O 4 | I/O 3 | I/O 2 | I/O 1 | HEX DATA |
|---|---|---|---|---|---|---|---|---|---|
| Maker code | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 98H |
| Device code | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | E5H |

For the access time of $t_{REAID}$, $t_{CR}$ and $t_{AR1}$ (refer to the AC Characteristics.)

## APPLICATION NOTES AND COMMENTS

**(1) Prohibition of unspecified commands**

The operation commands are listed in Table 3.   Data input as a command other than the specified commands in Table 3 is prohibited.   Stored data may be corrupted if an unspecified command is entered during the command cycle.

**(2) Pointer control for '00H', '01H', '50H'**

The device has three read modes which set the destination of the pointer.   Table 7 shows the destination of the pointer, and figure 20 shows the block diagram of their operations.

Table 7.  Pointer Destination

| READ MODE | COMMAND | POINTER |
|-----------|---------|---------|
| (1) | 00H | 0 to 255 |
| (2) | 01H | 256 to 511 |
| (3) | 50H | 512 to 527 |
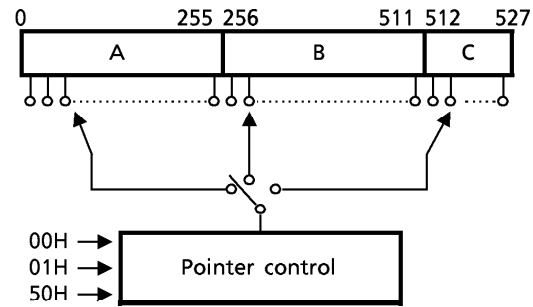


Figure 14.  Pointer control

The pointer is set to region 'A' by the '00H' command, to region 'B' by the '01' command, and to region 'C' by the '50H' command.

(Example)

The '00H' command needs to be input to set the pointer back to region 'A' when the pointer points to region 'C'.
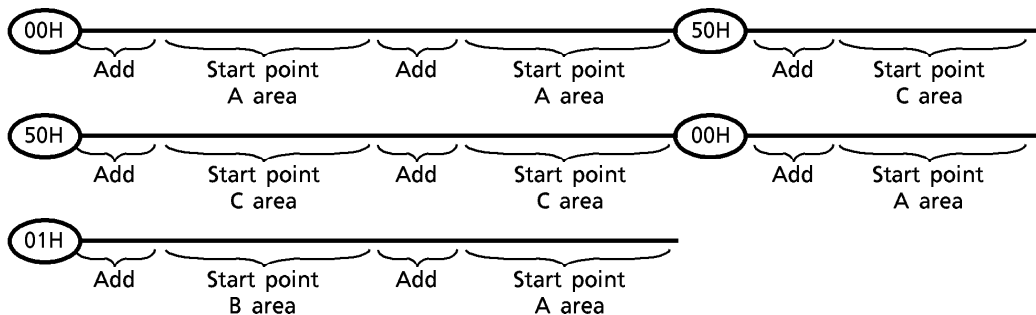


For programming into region 'C' only, set the start point to region 'C' with the '50H' command.
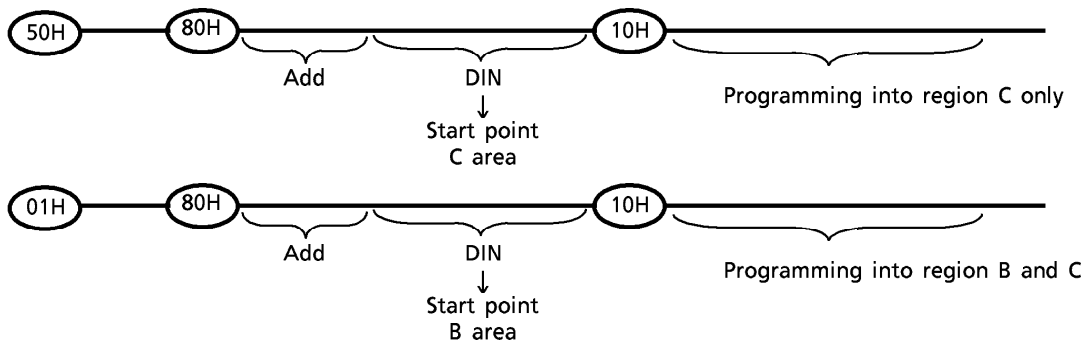


Figure 15.  Example of Pointer Setting

## (3) Acceptable commands after serial input command '80H'

Once the serial input command ('80H') is input, do not input any command other than the program execution command ('10H') or the reset command ('FFH').
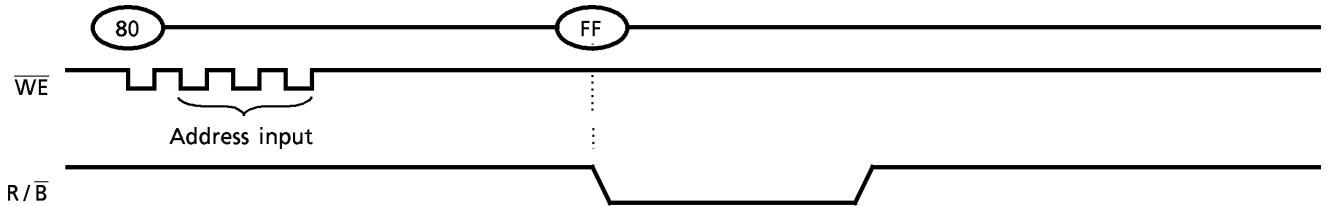


Figure 16.

If a command other than '10H' or 'FFH' is input, the program operation is not performed.



In case of this operation, the FFH command is needed.
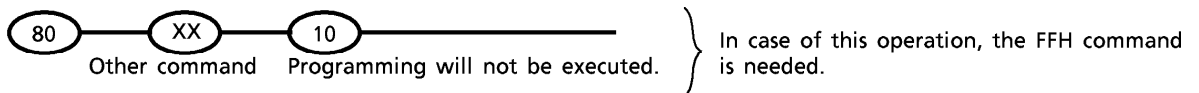
## (4) Status read during the read operation
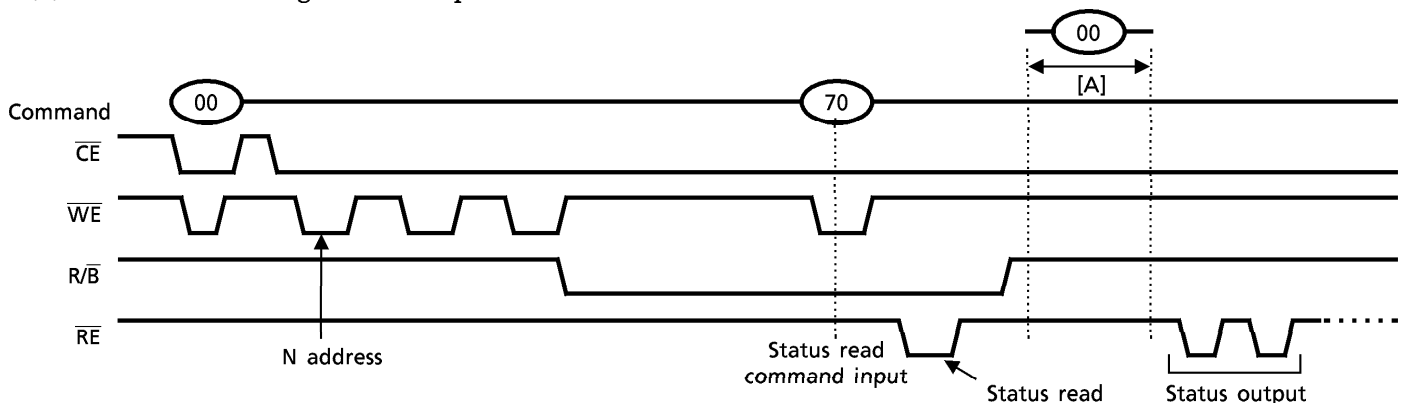


Figure 17.

The device status can be read out by inputting the status read command '70H' during the read mode. Once the device is set to the status read mode after '70H' command input, the device does not return to the read mode.

Therefore, a status read during the read operation is prohibited.

However, when the read command '00H' is input during [A], the status mode is reset, and the device returns to the read mode. In this case, the data output starts from address N without address input.

## (5) Auto program failure



When the programming result for page address M is 'Fail', try to program the page to address N in another block. Because the previous input data is lost, the same sequence of '80H' command, address and data input is necessary.
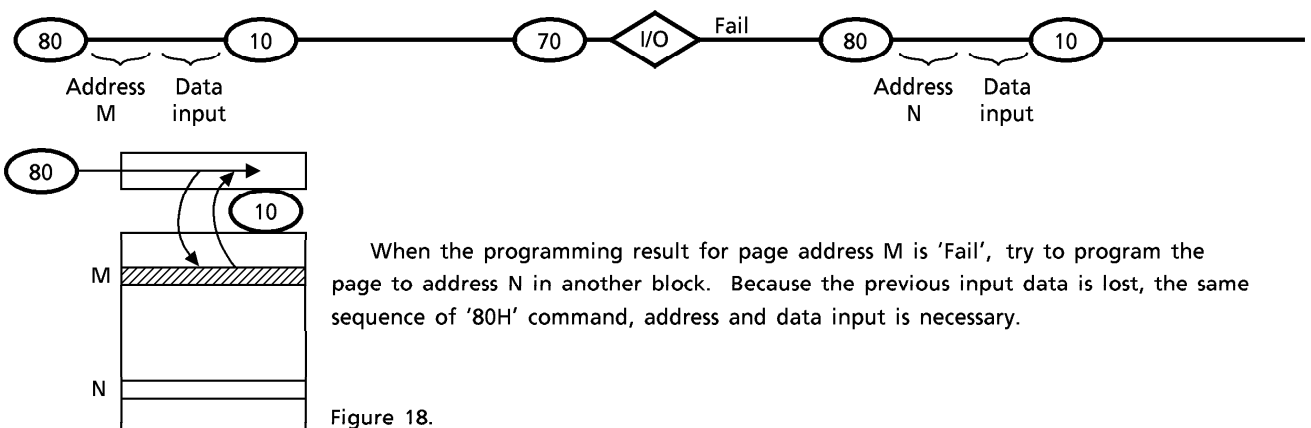
Figure 18.

(6) R/B̄ : Termination for the Ready / Busy pin (R / B̄)

A pull-up resistor needs to be used for termination because the R/B̄ buffer consists of an open drain circuit.



Figure 19.
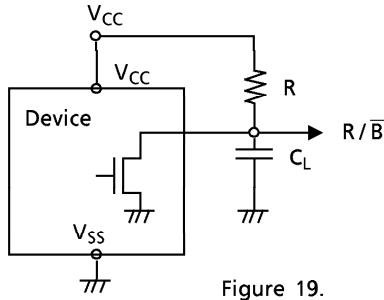
This data may vary by device.
We recommend that you use this data as a reference when selecting a resistor value.
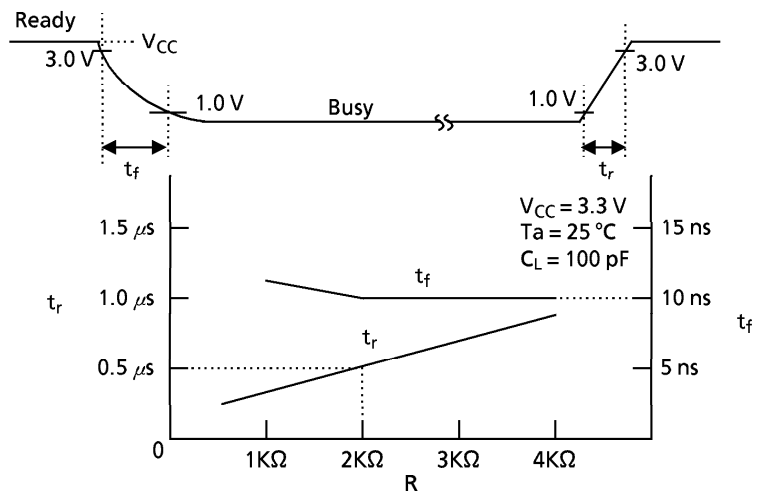
(7) Status after Power On

Although the device is set to the read mode after power‑up, the following sequence is needed because each input signal may not be stable at power on.
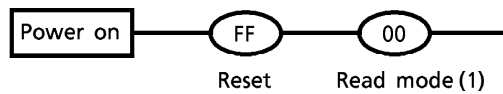


Figure 20.

(8) Power On / Off Sequence :

The W̄P̄ signal is useful for protecting against data corruption at power on / off.  The following timing is necessary :
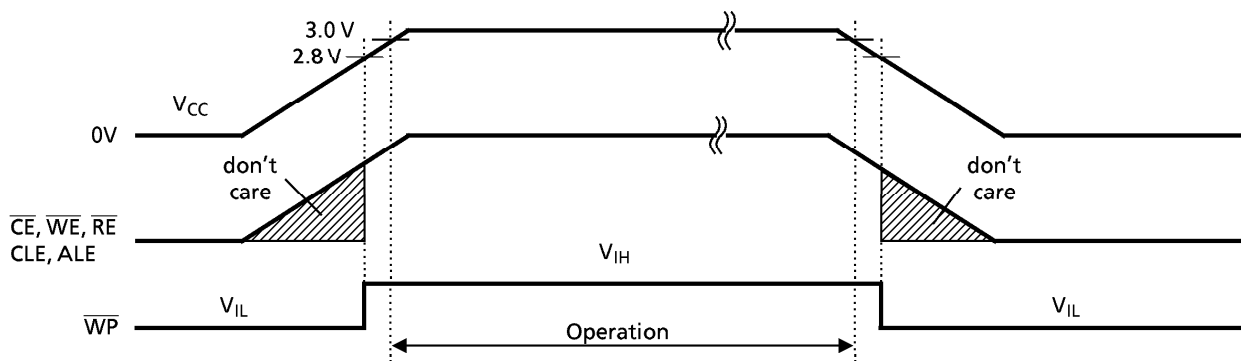


Figure 21.  Power On / Off Sequence

(9) Setup for $\overline{WP}$ Signal

The erase and program operations are compulsively reset when $\overline{WP}$ goes low. The following conditions must be met:

Program
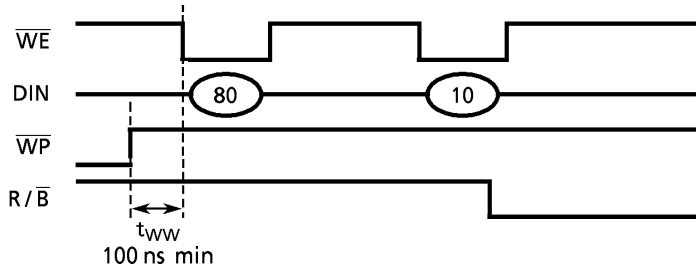


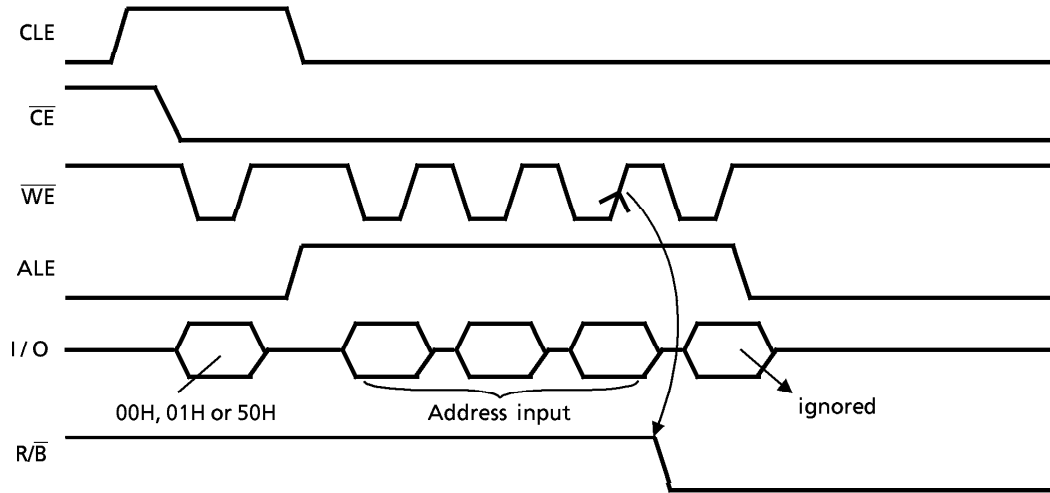Program Prohibition
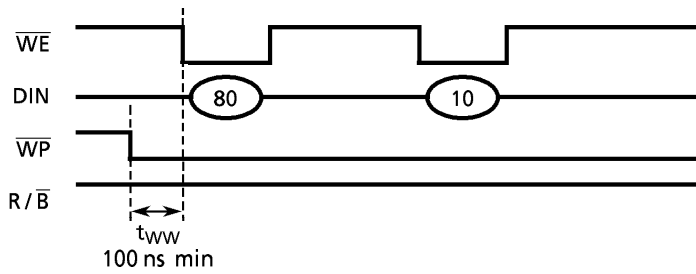


Erase
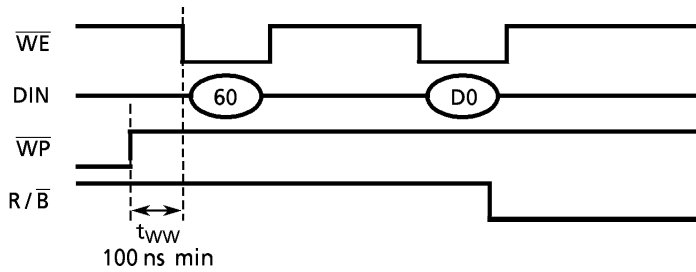


Erase Prohibition
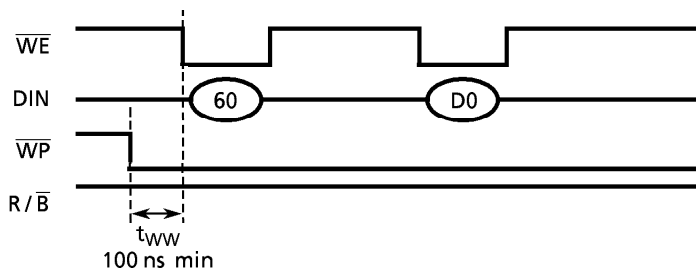
(10) In the case that 4 address cycles are input
    Although the device may acquire the fourth address, it is ignored inside the chip.

<u>Read operation</u>



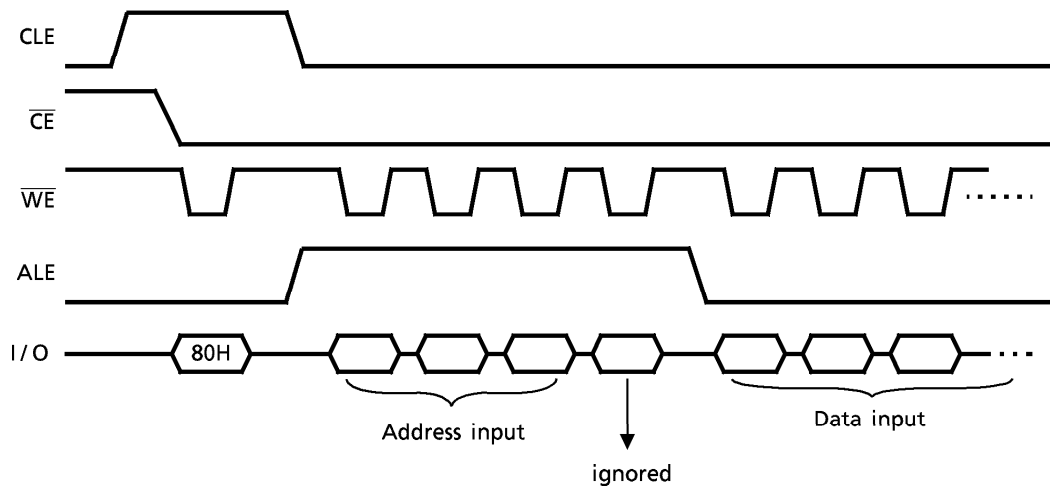Internal read operation starts when $\overline{\text{WE}}$ in the third cycle goes high.

Figure 22.

<u>Program operation</u>



Figure 23.

(11) Divided program in the same page (Partial page program)

The device allows a page to be divided into 10 segments (maximum) with each page segment programmed individually as follows:

The first programming

Column A          Column B

Page N    | Data Pattern 1 |                    '1'                    |

The second programming

Column C          Column D

Page N    |        '1'        | Data Pattern 2 |              '1'              |

The third programming

Column E          Column F

Page N    |                    '1'                | Data Pattern 3 | '1' |

Result

Column A          Column B    Column C          Column D    Column E          Column F

Page N    | Data Pattern 1 | '1' | Data Pattern 2 | '1' | Data Pattern 3 | '1' |
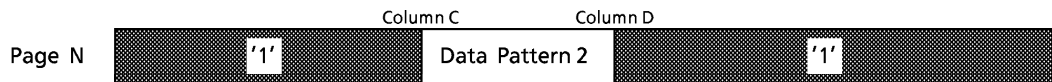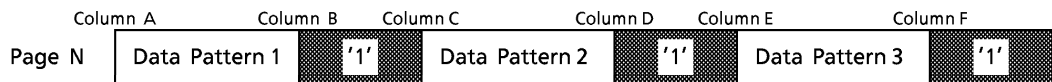
Figure 24.

Note : The input data for unprogrammed or previously programmed page segments must be '1'.
(i.e. Mask all page bytes outside the segment to be programmed with '1' data.)

(12) Notification for $\overline{RE}$ Signal

The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in the read mode. Therefore, once the device is set into the read mode by the '00H', '01H' or '50H' command, the internal column address counter is incremented by the $\overline{RE}$ clock independent of (before or after) the address input. Assuming that the $\overline{RE}$ clocks are inputted before address input and the pointer reaches the last column address, internal read operation (array → register) will occur and the device will be in the busy state. (Refer to Figure 25)
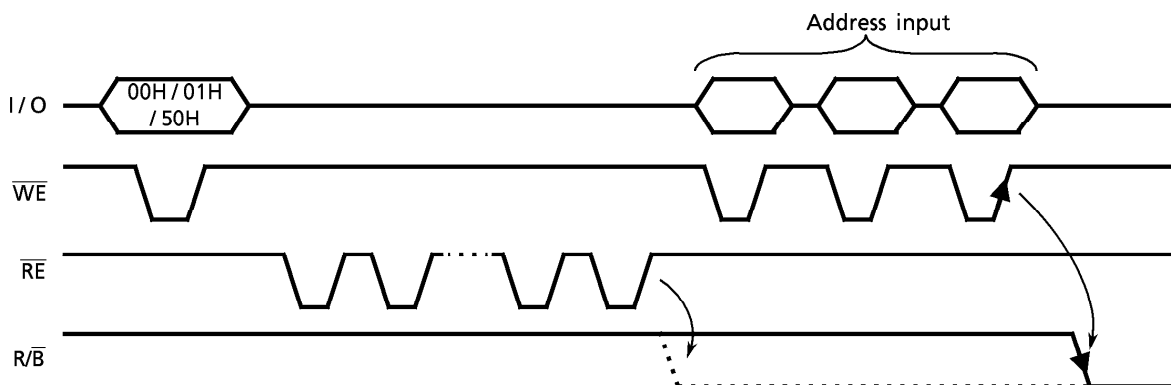
Figure 25.

Therefore, $\overline{RE}$ clocks must occur after the address input.

(13) Invalid block (bad block)

The device contains unusable blocks.  Therefore, the following issues must be recongnized:
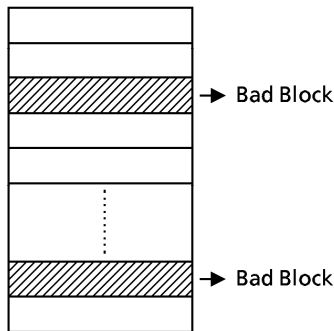


Figure. 26

Check if the device has any bad blocks after device installation into the system.  Do not try to access bad blocks.  A bad block does not affect the performance of good blocks becasue it is isolated from the bit line by the select gate.

The number of valid blocks is as follows:

|                            | MIN | TYP | MAX | UNIT  |
|----------------------------|-----|-----|-----|-------|
| Valid (Good) Block Number  | 502 | 508 | 512 | Block |

Figure 28 shows the bad block test flow.

(14) Failure Phenomena for Program and Erase Operations.

The device may fail during program or erase operation.

The following possible failure modes should be considered when inplementing a highly reliable system.

| FAILURE MODE | | DETECTION AND COUNTERMEASURE SEQUENCE |
|----------|----------------------|------------------------------------------|
| Block | Erase Failure | Status Read after Erase  → Block Replacement |
| Page | Program Failure | Status Read after Prog.  → Block Replacement |
| Single Bit* | Program Failure '1' → '0' | (1) Block Verify after Prog.  → Retry |
|  |  | (2) ECC |

* : (1) or (2)

● ECC   :   Error Correcting code → Hamming Code etc.
Example : 1 bit correction & 2 bit detection.
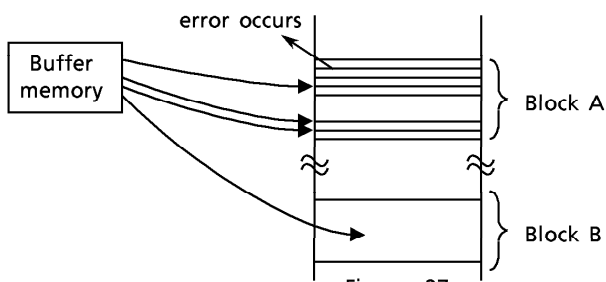
● Block Replacement

Program



Figure. 27

When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer.  Then, prevent further system accesses to Block A ( by creating a 'bad block' table or an another appropriate scheme.)

Erase

When an error occurs for an erase operation, prevent future accesses to this bad block (again by creating a table within the system or other appropriate scheme).

## BAD BLOCK TEST FLOW

C : Checker board pattern
C̄ : Invert checker board pattern
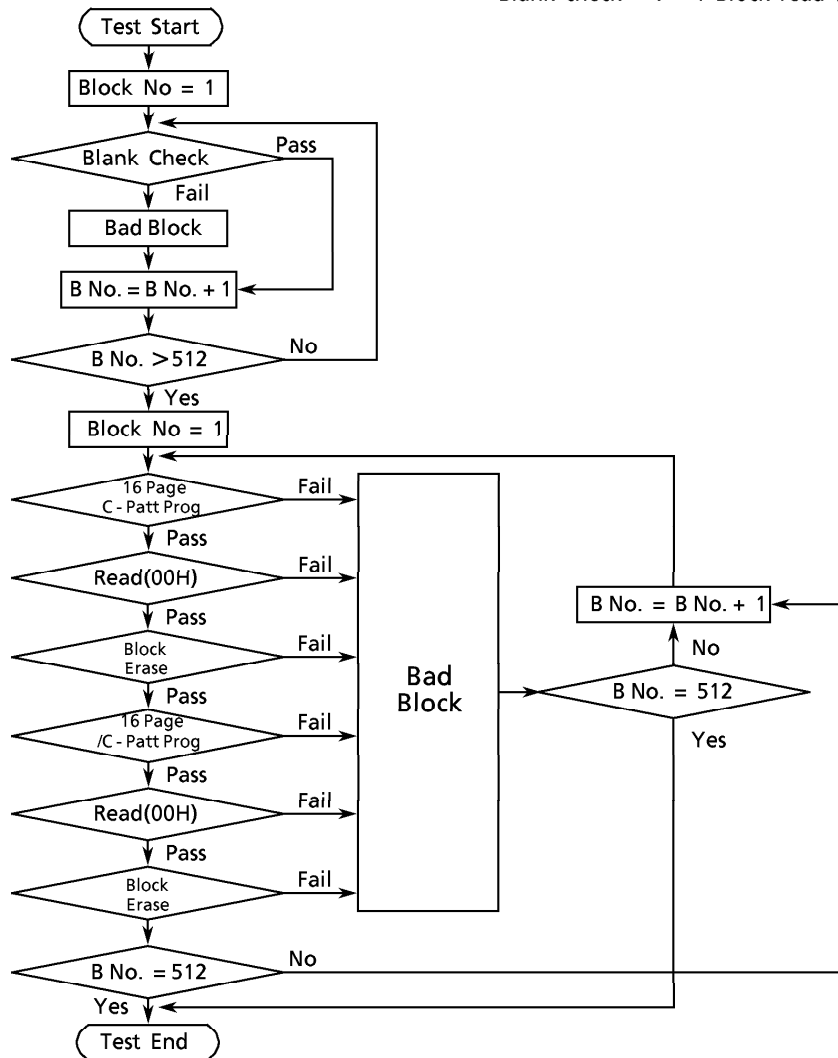Blank check : 1 Block read (FFH)



Figure 28.

## ATTENTION

(1) Avoid bending or subjecting the card to sudden impact.

(2) Avoid touching the connectors so as to avoid damage from static electricity.
This card should be kept in the antistatic film case when not in use.

(3) Toshiba cannot accept, and hereby disclaims liability for, any damage to the card including data
corruption that may occur because of mishandling.

## PACKAGE DIMENSIONs
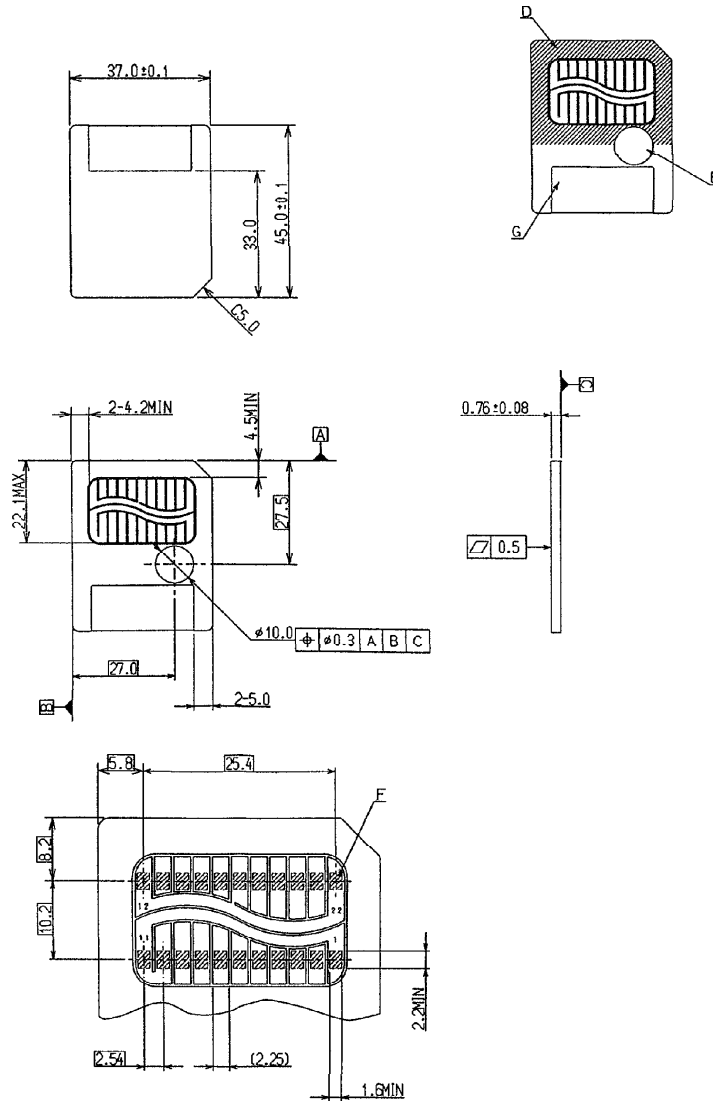
Plastic TSOP

TSOP Ⅱ 44/40 - P - 400 - 0.80B

UNITS : mm
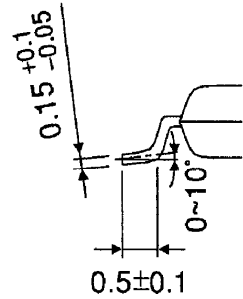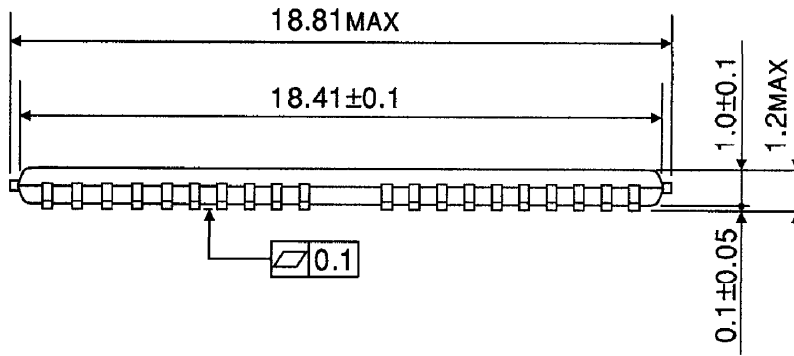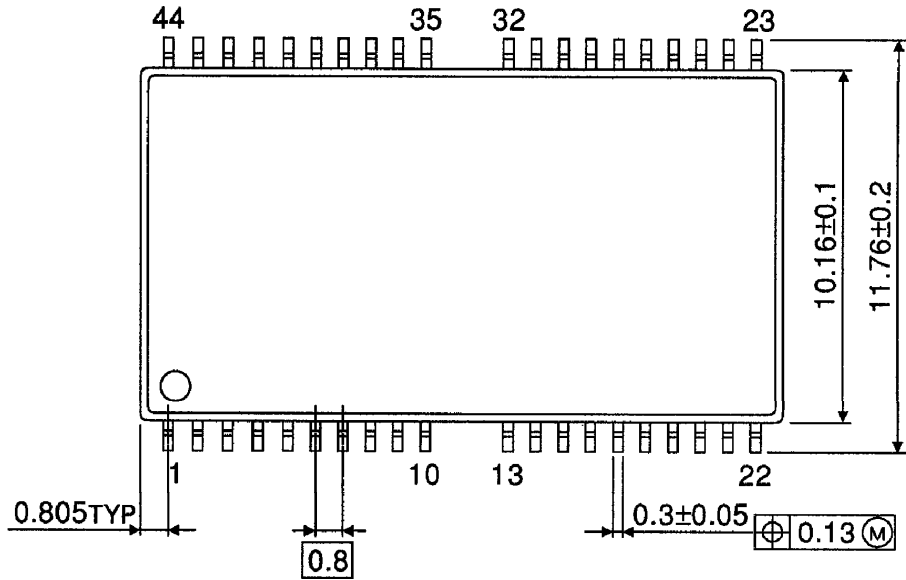
## PACKAGE DIMENSIONS

FDC−22A

UNITS: mm



Contact area (2 : 1)

E : Write protect area
F : The distance between the surface of D and all contact areas is less than 0.1 mm.
G: Index area