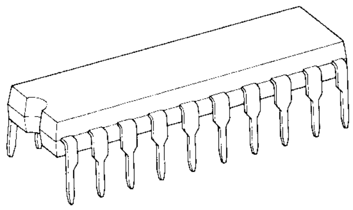
TOAHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

# TB62710P, TB62710F, TB62710FN

8-Bit Constant-Current LED Driver for Cathode Common LED

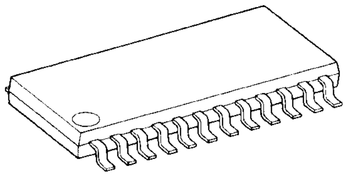
The TB62710P, TB62710F and TB62710FN are specifically designed for use as LED and LED display (cathode-common) Constant-current drivers.
The constant-current output circuits can be set up using an external resistor (IOUT = −90 mA max).
These ICs are monolithic integrated circuits have been designed using the Bi-CMOS process.
The devices consist of an 8-bit shift register, a latch, an ANDgate and constant-current drivers.

TB62710P



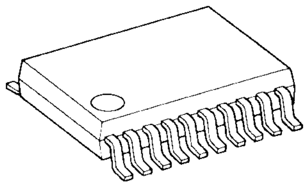
DIP20-P-300-2.54A

TB62710F



SSOP24-P-300-1.00

TB62710FN



SSOP20-P-225-0.65A

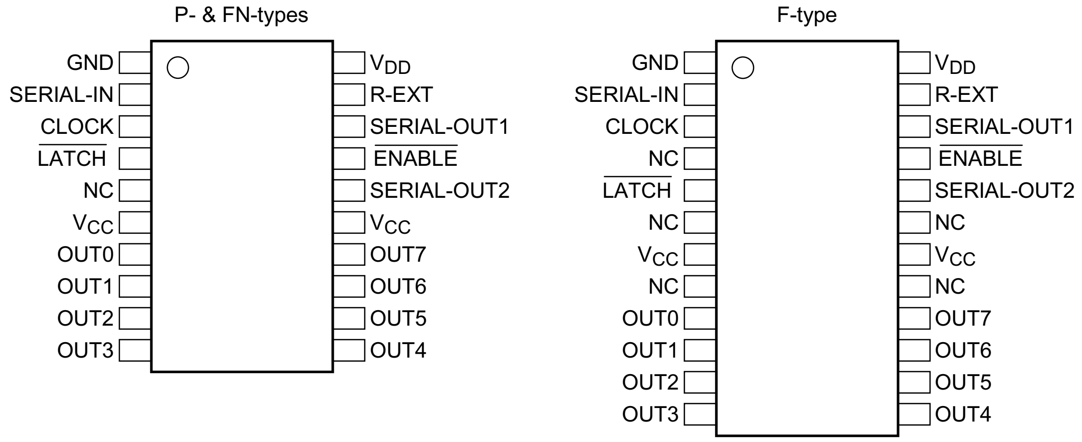
Weight:
DIP20-P-300-2.54A: 2.25 g (Typ.)
SSOP24-P-300-1.00: 0.33 g (Typ.)
SSOP20-P-225-0.65A: 0.10 g (Typ.)

## FEATURES

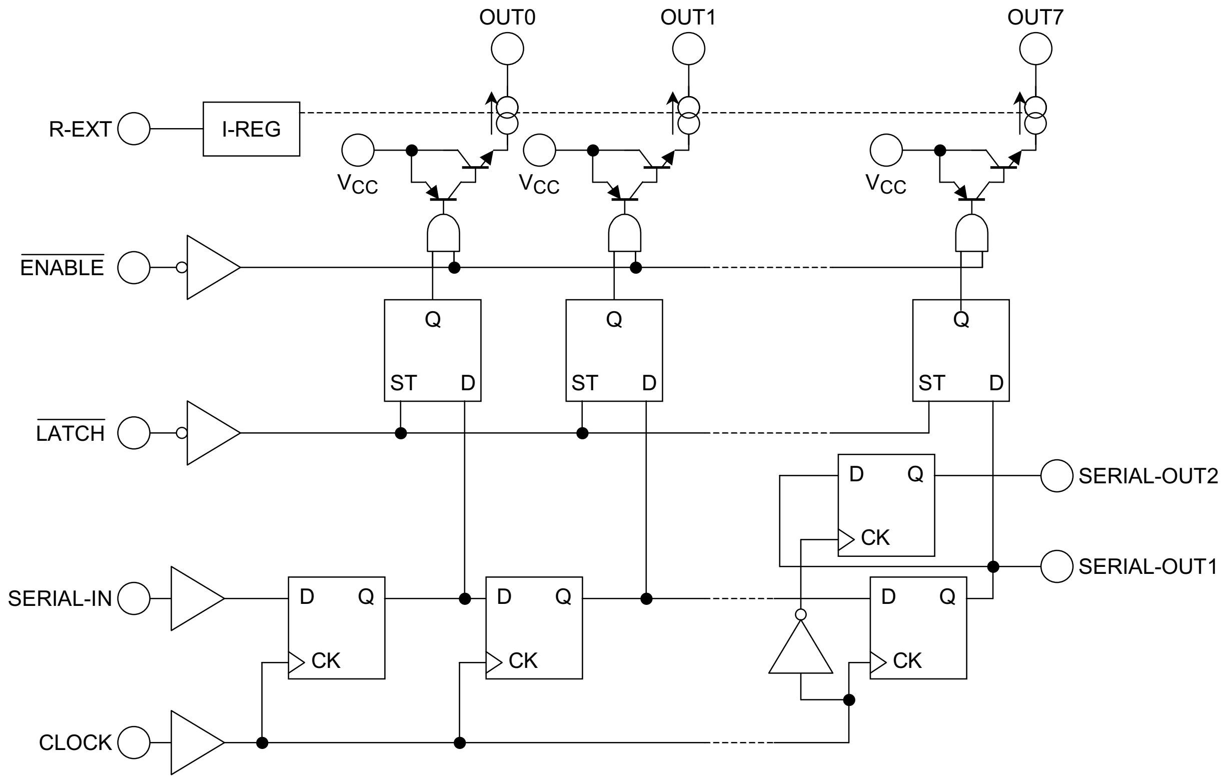
- Constant-current output:
  A single resistor can be used to set any output current in the range −5~−90 mA.
- Maximum clock frequency: $f_{CLK}$ = 15 MHz
  (operating while connected in cascade, $T_{opr}$ = 25°C)
- 5-V CMOS compatible input
- Packages:
  P-type: DIP20-P-300-2.54A
  F-type: SSOP24-P-300-1.00
  FN-type: SSOP20-P-225-0.65A
- Constant-output-current accuracy:

| Output – GND Voltage | Current accuracy | | Output Current (max) |
|---|---|---|---|
| | between bits | between ICs | |
| ≧ 2.0 V (min) | ±6% | ±15% | −5~−90 mA |
| ≧ 1.5 V (min) | | | −5~−40 mA |

## Pin Assignment (top view)




## Block Diagram

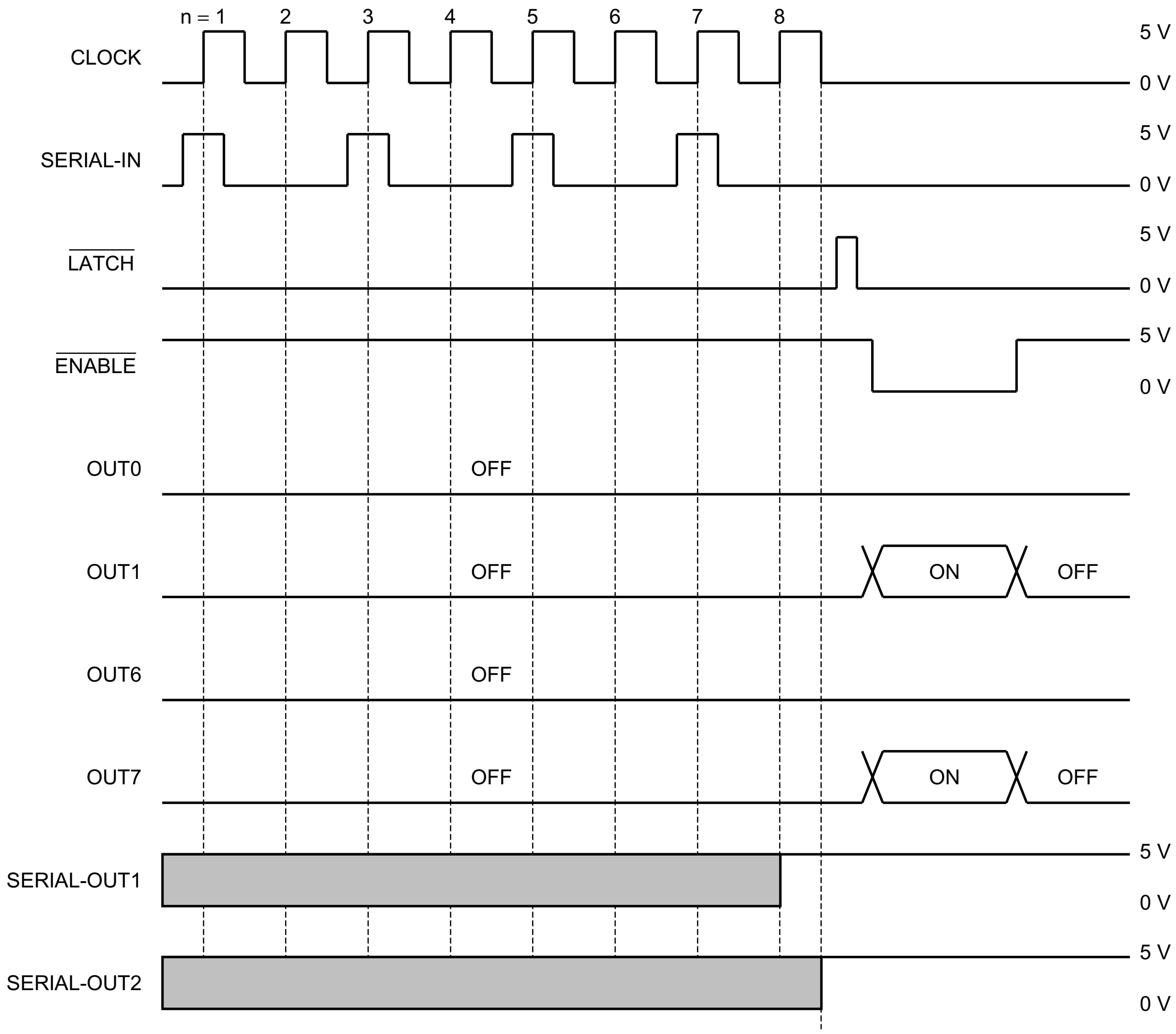



## Truth Table

| CLOCK | LATCH | ENABLE | SERIAL-IN | OUT0··· OUT5 ··· OUT7 | SERIAL-OUT |
|---|---|---|---|---|---|
| ↑ | H | L | Dn | Dn ··· Dn – 5 ··· Dn – 7 | Dn – 7 |
| ↑ | L | L | Dn + 1 | No Change | Dn – 6 |
| ↑ | H | L | Dn + 2 | Dn + 2 ··· Dn – 3 ··· Dn – 5 | Dn – 5 |
| ↓ | X | L | Dn + 3 | Dn + 2 ··· Dn – 3 ··· Dn – 5 | Dn – 5 |
| ↓ | X | H | Dn + 3 | OFF | Dn – 5 |

Note 1: OUT0~OUT7 = ON when Dn = "H"; OUT0~OUT7 = OFF when Dn = "L".
In order to ensure that the level of the power supply voltate is correct, an external resistor must be connected between R-EXT and GND.

## Timing Diagram



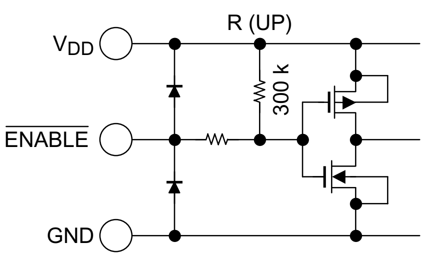

Note 2: The latches circuit holds data by pulling the LATCH terminal Low.
And, when LATCH terminal is a "H" level, latch circuit doesn't hold data, and it passes from the input to the output.
When ENABLE terminal is a "L" level, output terminal OUT0~ OUT7 respond to the data, and on & off does.
And, when ENABLE terminal is a "H" level, it offs with the output terminal regardless of the data.

## Terminal Description

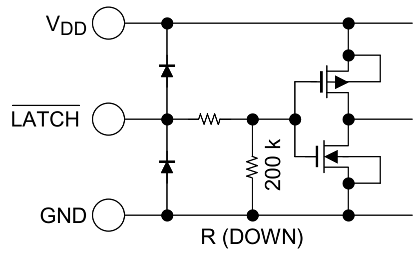
| Pin No. | | Pin Name | Function |
|---|---|---|---|
| P/FN-Type | F-Type | | |
| 1 | 1 | GND | GND terminal for control logic |
| 2 | 2 | SERIAL-IN | Input terminal for serial data for data shift register |
| 3 | 3 | CLOCK | Input terminal for clock for data shift on rising edge |
| 4 | 5 | $\overline{\text{LATCH}}$ | Input terminal for data strobe<br>When the $\overline{\text{LATCH}}$ input is driven High, data is latched. When it is pulled Low, data is hold. |
| 6, 15 | 7, 18 | $V_{CC}$ | 0 V~17 V supply voltage terminal for LED |
| 7~14 | 9~16 | OUT0~OUT7 | Output terminals |
| 17 | 21 | $\overline{\text{ENABLE}}$ | Input terminal for output enable.<br>All outputs (OUT0~OUT7) are turned off, when the $\overline{\text{ENABLE}}$ terminal is driven High.<br>And are turned on, when the terminal is driven Low. |
| 16 | 20 | SERIAL-OUT2 | Output terminal for serial data input on SERIAL-IN terminal |
| 18 | 22 | SERIAL-OUT1 | Output terminal for serial data input on SERIAL-IN terminal |
| 19 | 23 | R-EXT | Input terminal used to connect an external resistor. This regulated the output current. |
| 20 | 24 | $V_{DD}$ | 5-V supply voltage terminal |
| 5 | 4, 6, 8, 17, 19 | NC | Not connected |

## Equivalent Circuits For Inputs and Outputs

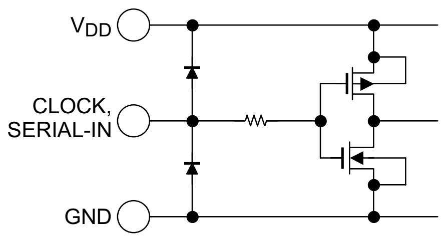
### $\overline{\text{ENABLE}}$ terminal



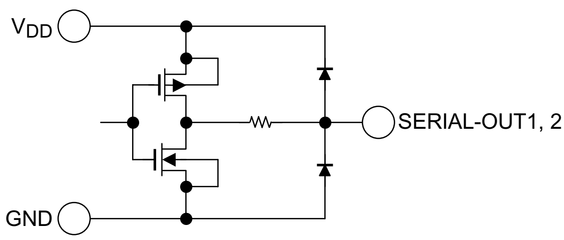

### $\overline{\text{LATCH}}$ terminal




### CLOCK, SERIAL-IN terminal




### SERIAL-OUT1 and SERIAL-OUT2 terminals



## Maximum Ratings ($T_{opr}$ = 25°C)

| Characteristic | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | | $V_{DD}$ | 0~7.0 | V |
| Supply voltage for LED | | $V_{LED}$ | 0~17.0 | V |
| Input voltage | | $V_{IN}$ | –0.4~$V_{DD}$ + 0.4 | V |
| Output current | | $I_{OUT}$ | –90 | mA |
| Output voltage | | $V_{OUT}$ | –0.4~17 | V |
| Clock frequency | | $f_{CLK}$ | 15 | MHz |
| $V_{CC}$ terminal current | | $IV_{CC}$ | 1440 | mA |
| Power Dissipation (Note 3) | P-type (when not mounted) | $P_{d1}$ | 1.47 | W |
| | F-type (when not mounted) | $P_{d2}$ | 0.59 | |
| | F-type (on PCB) | | 0.83 | |
| | FN-type (when not mounted) | $P_{d3}$ | 0.71 | |
| | FN-type (on PCB) | | 0.96 | |
| Thermal Resistance (Note 3) | P-type (when not mounted) | $R_{th\ (j\text{-}a)\ 1}$ | 85 | °C/W |
| | F-type (when not mounted) | $R_{th\ (j\text{-}a)\ 2}$ | 210 | |
| | F-type (on PCB) | | 150 | |
| | FN-type (when not mounted) | $R_{th\ (j\text{-}a)\ 3}$ | 175 | |
| | FN-type (on PCB) | | 130 | |
| Operating Temperature | | $T_{opr}$ | –40~85 | °C |
| Storage Temperature | | $T_{stg}$ | –55~150 | °C |

Note 3: P-Type: Powes dissipation is derated by 12.5 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.

F-Type: Powes dissipation is derated by 6.7 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.
With device mounted on PCB of 60% Cu and of dimensions 50 mm × 50 mm × 1.6 mm

FN-Type: Powes dissipation is derated by 7.7 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.
With device mounted on PCB of 40% Cu and of dimensions 50 mm × 50 mm × 1.6 mm

## Recommended Operating Conditions ($T_{opr}$ = –40°C ~85°C unless otherwise specified)

| Characteristic | | Symbol | Conditions | | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Supply voltage | | $V_{DD}$ | — | | 4.5 | 5.0 | 5.5 | V |
| Supply voltage for LED | | $V_{CC1}$ | $V_{CC} - V_{OUT} \geqq 2.0$ V, $I_{OUT} \leqq -90$ mA | | 4 | — | 17 | V |
| | | $V_{CC2}$ | $V_{CC} - V_{OUT} \geqq 1.5$ V, $I_{OUT} \leqq -40$ mA | | 3.5 | — | 17 | |
| Output voltage | | $V_{OUT}$ | $V_{CC}$ common | | 0 | — | –17 | V |
| Output current | | $I_{OUT}$ | DC1 circuit | | –5 | — | –78 | mA |
| | | $I_{OH}$ | SERIAL-OUT1, 2 | | — | — | –1.0 | |
| | | $I_{OL}$ | SERIAL-OUT1, 2 | | — | — | 1.0 | |
| Input voltage | | $V_{IH}$ | $V_{DD}$ = 4.5~5.5 V | | 0.7 $V_{DD}$ | — | $V_{DD}$ + 0.3 | V |
| | | $V_{IL}$ | | | –0.3 | — | 0.3 $V_{DD}$ | |
| $\overline{\text{LATCH}}$ pulse width | | $t_{wLAT}$ | $V_{DD}$ = 4.5~5.5 V | | 100 | — | — | ns |
| CLOCK pulse width | | $t_{wCLK}$ | $V_{DD}$ = 4.5~5.5 V | | 50 | — | — | ns |
| $\overline{\text{ENABLE}}$ pulse width | | $t_{wENA}$ | $V_{DD}$ = 4.5~5.5 V | | 1000 | — | — | ns |
| Set-up time for DATA | | $t_{setup}$ | $V_{DD}$ = 4.5~5.5 V | | 100 | — | — | ns |
| Hold time for DATA | | $t_{hold}$ | $V_{DD}$ = 4.5~5.5 V | | 100 | — | — | ns |
| Clock frequency | | $t_{CLK}$ | $V_{DD}$ = 4.5~5.5 V, Cascade operation | | — | — | 10.0 | ns |
| Power Dissipation | P-type | $P_{d1}$ | $T_{opr}$ = 85°C | When not mounted | — | — | 0.76 | W |
| | F-type | $P_{d2}$ | | On PCB | — | — | 0.43 | |
| | FN-type | $P_{d3}$ | | | — | — | 0.50 | |

## Electrical Characteristics ($T_{opr}$ = 25°C, $V_{DD}$ = 5 V, $V_{CC}$ = 17 V unless otherwise specified)

| Characteristic | | Symbol | Test circuit | Conditions | | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Output leakage current | | $I_{LEAK}$ | — | $V_{CC}$ = 17.0 V | | — | — | –10 | μA |
| Output voltage | SERIAL-OUT 1, 2 | $V_{OH}$ | — | $I_{OH}$ = –1.0 mA | | — | — | 0.4 | V |
| | | $V_{OL}$ | — | $I_{OL}$ = 1.0 mA | | 4.6 | — | — | |
| Output current (including current skewing) | | $I_{OUT1}$ | — | $V_{CC}$ = 4 V, $V_{OUT}$ = $V_{CC}$ – 2.0 V | $R_{EXT}$ = 360 Ω | –62.1 | –73.0 | –83.9 | mA |
| | | $I_{OUT2}$ | — | $V_{CC}$ = 4 V, $V_{OUT}$ = $V_{CC}$ – 2.0 V | $R_{EXT}$ = 620 Ω | –34.0 | –40.0 | –46.0 | |
| | | $I_{OUT3}$ | — | $V_{CC}$ = 3.5 V, $V_{OUT}$ = $V_{CC}$ – 1.5 V | $R_{EXT}$ = 620 Ω | –32.3 | –38.0 | –43.7 | |
| | Current skew | $\Delta I_{OUT}$ | — | Same as $I_{OUT1}$, $I_{OUT2}$ and $I_{OUT3}$ | | — | ±1.5 | ±6.0 | % |
| Supply voltage regulation | | %/$V_{DD}$ | — | Ta = –40~85°C | $R_{EXT}$ = 360 Ω | — | 1.5 | 5.0 | %/V |
| Pull-up resistor | | $R_{in\ (Up)}$ | — | — | | 150 | 300 | 600 | kΩ |
| Pull-down resistor | | $R_{in\ (Down)}$ | — | — | | 100 | 200 | 400 | kΩ |
| Supply current | $V_{DD}$ | $I_{DD\ (OFF)}$ | — | All outputs = OFF | $R_{EXT}$ = OPEN | — | 0.6 | 1.2 | mA |
| | | $I_{DD\ (ON)\ 1}$ | — | DATA = ALL “H”, All outputs = ON (no load) | $R_{EXT}$ = 360 Ω | — | 7.5 | 10.0 | |
| | | $I_{DD\ (ON)\ 2}$ | — | DATA = ALL “H”, All outputs = ON (no load) | $R_{EXT}$ = 620 Ω | — | 4.0 | 7.0 | |
| | $V_{CC}$ | $I_{CC\ (OFF)}$ | — | DATA = ALL “L”, All outputs = OFF (no load) | $R_{EXT}$ = 620 Ω | — | 0.5 | 1.0 | |
| | | $I_{CC\ (ON)}$ | — | DATA = ALL “H”, All outputs = ON (no load) | $R_{EXT}$ = 360 Ω | — | 42.0 | 52.0 | |

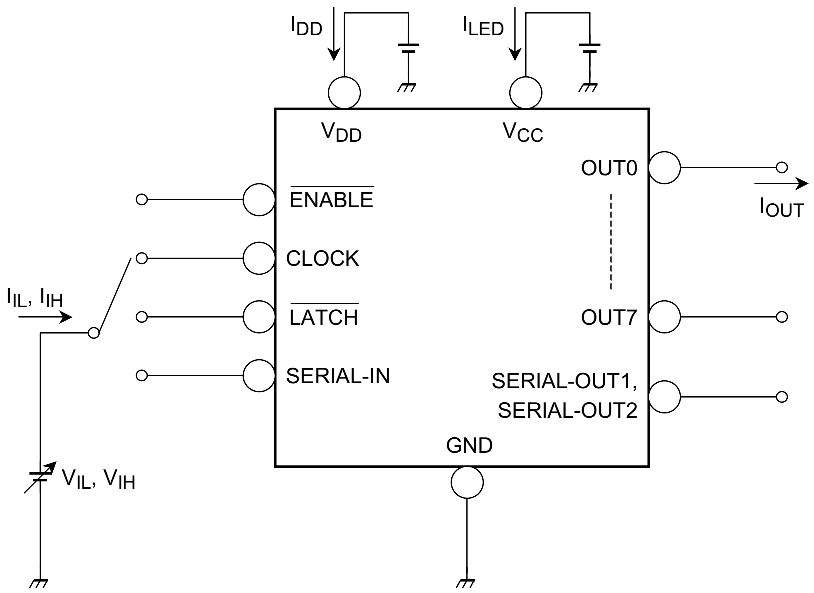
### Switching Characteristics ($T_{opr}$ = 25°C unless otherwise specifed)

| Characteristic | | Symbol | Test circuit | Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time ("L" to "H") | CLK-OUTn | $t_{pLH}$ | — | $V_{DD}$ = 5.0 V, $V_{CC}$ = 17.0 V<br>$V_{OUT}$ = $V_{CC}$ − 2.0 V<br>$V_{IH}$ = $V_{DD}$, $V_{IL}$ = GND<br>$R_{EXT}$ = 620 Ω<br>$C_L$ = 10.5 pF<br>$t_{or}$: 10~90%<br>$t_{of}$: 90~10%<br>$t_{pLH}$: 50~10%<br>$t_{pHL}$: 50~90%<br>Set the switching characteristics according to the result of measuring the voltage waveform. | — | 200 | 450 | ns |
| | $\overline{LATCH}$ -OUTn | | — | | | | | |
| | $\overline{ENABLE}$ -OUTn | | — | | | | | |
| | CLK-SOUTn | | — | | — | 20 | 70 | |
| Propagation delay time ("H" to "L") | CLK-OUTn | $t_{pHL}$ | — | | — | 60 | 180 | ns |
| | $\overline{LATCH}$ -OUTn | | — | | | | | |
| | $\overline{ENABLE}$ -OUTn | | — | | | | | |
| | CLK-SOUTn | | — | | — | 20 | 70 | |
| Pulse width | CLK | $t_{wCLK}$ | — | | — | 20 | 30 | ns |
| | $\overline{LATCH}$ | $t_{wLAT}$ | — | | — | 10 | 25 | |
| Set-up time $\overline{LATCH}$ /SIN/ CLOCK | DATA = "L" → "H" | $t_{setup}$ | —<br>— | | — | 25 | 50 | ns |
| Hold time $\overline{LATCH}$ /SIN/ CLOCK | DATA = "H" → "L" | $t_{hold}$ | —<br>— | | — | 0 | 30 | ns |
| Slow clock | Rise time (Note 4) | $t_r$ | — | | — | — | 10 | μs |
| | Fall time (Note 4) | $t_f$ | — | | — | — | 10 | μs |
| Output rise time | | $t_{or}$ | — | | 25 | 55 | 110 | ns |
| Output fall time | | $t_{of}$ | — | | 250 | 450 | 600 | ns |

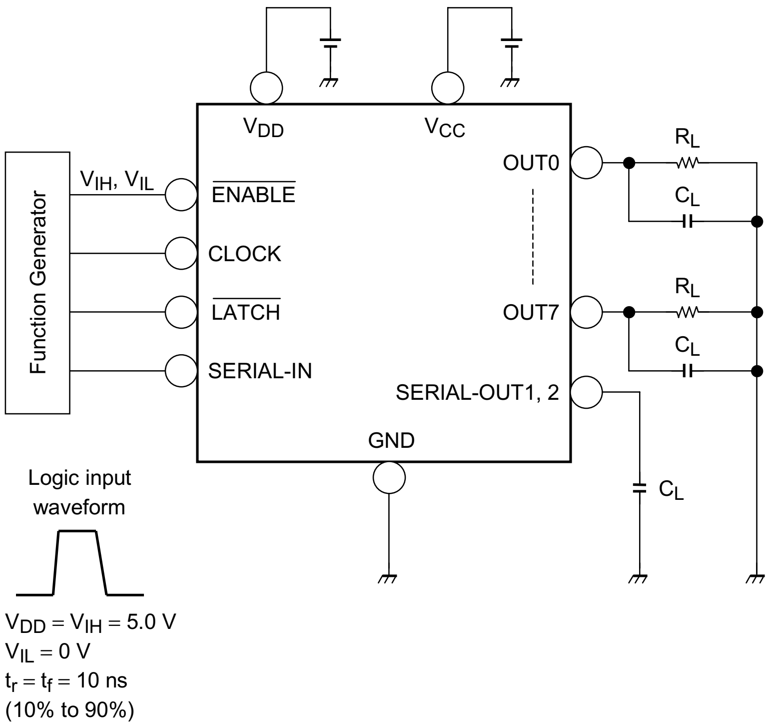
Note 4: If the device is connected in a cascade and $t_r$/$t_f$ for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.

# Test Circuit

## DC Characteristic

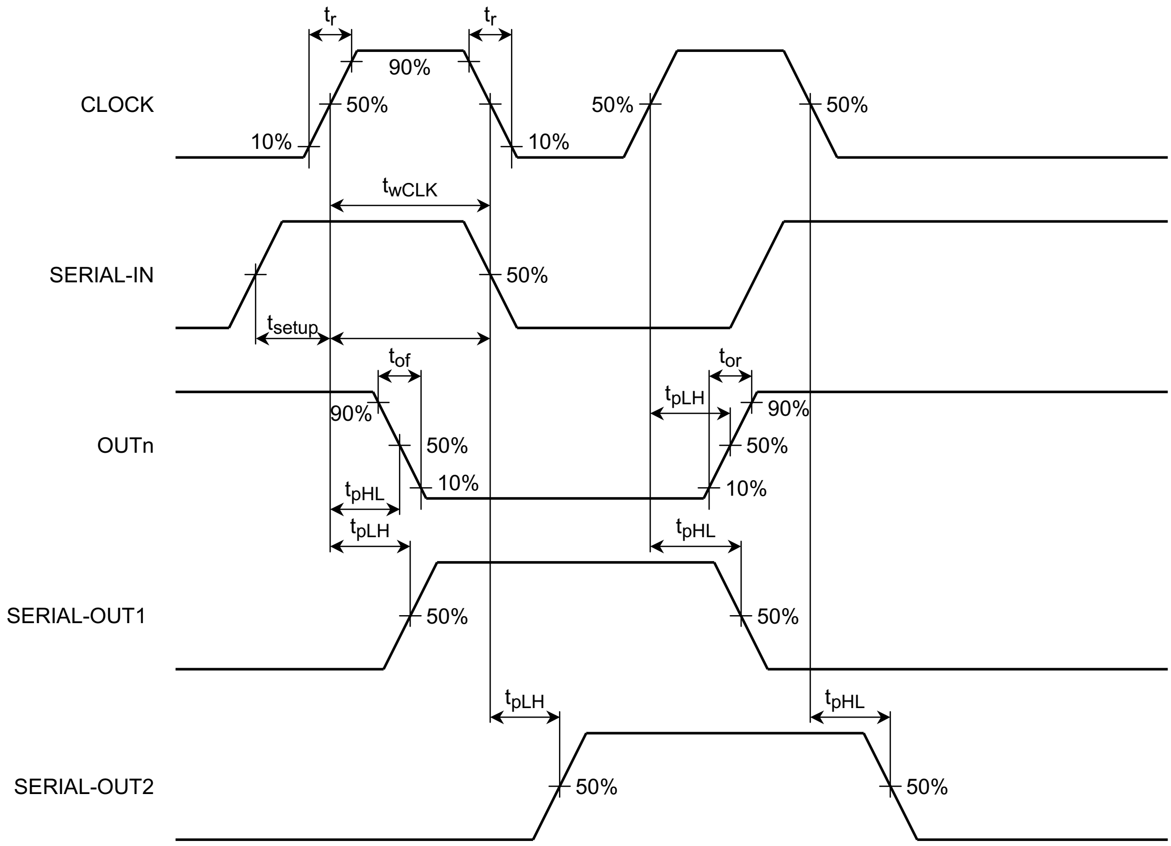



## AC Characteristic

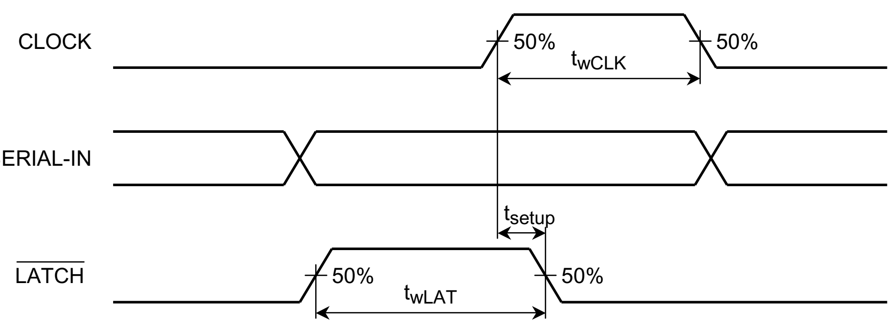


## Timing Waveforms

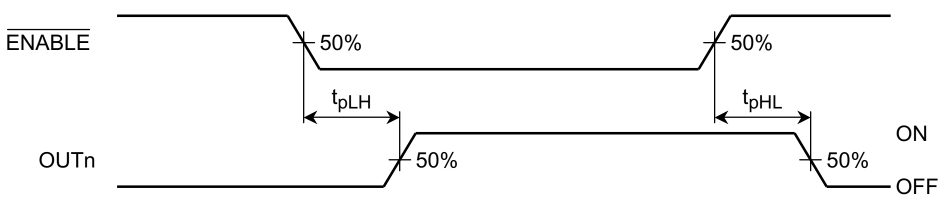
### 1. CLOCK, SERIAL OUTn



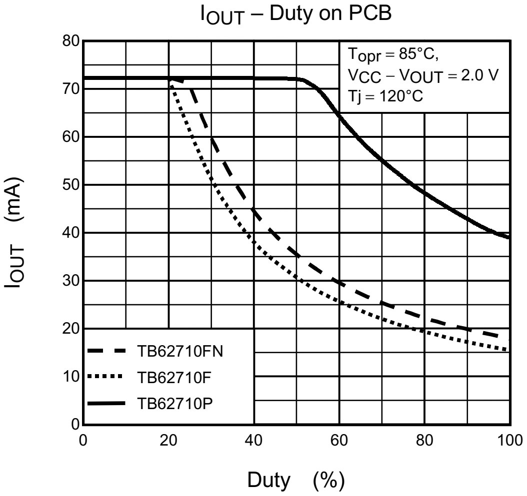

### 2. CLOCK, $\overline{\text{LATCH}}$

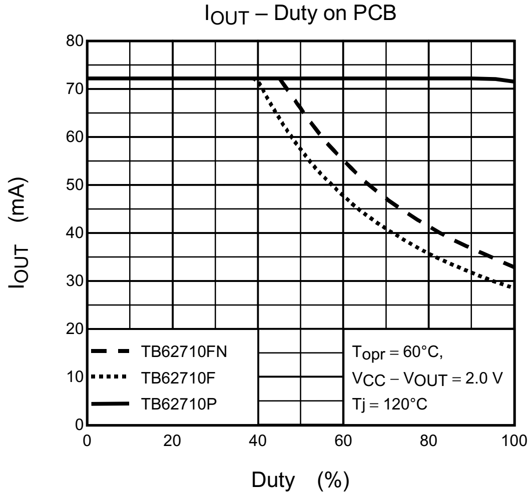


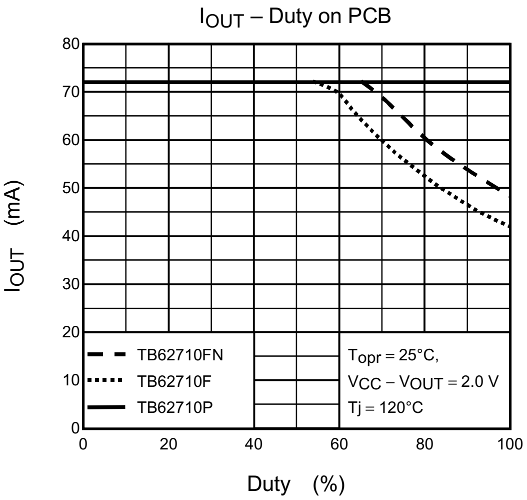

### 3. $\overline{\text{ENABLE}}$ – OUTn

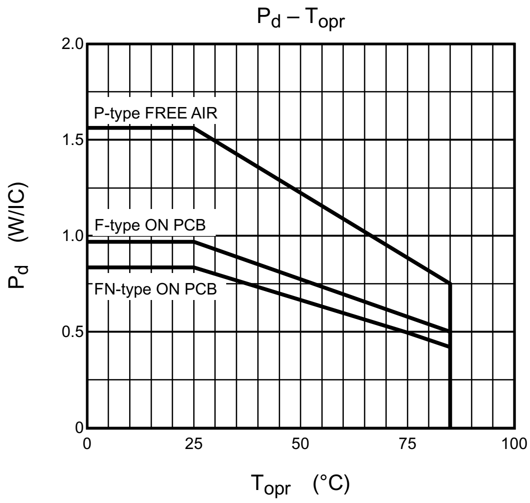


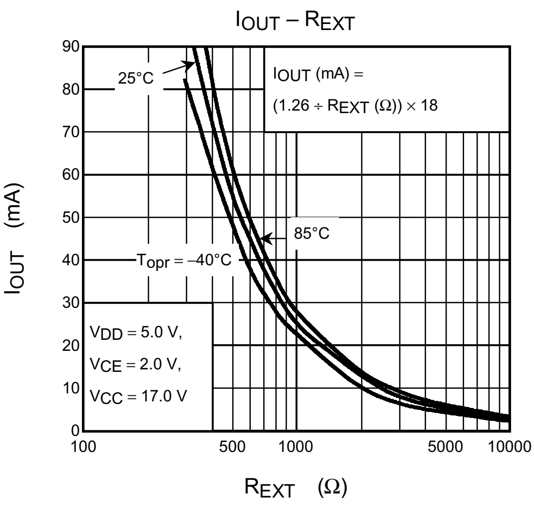
## Reference Data (duty curves + package power dissipation)



The bottom figure shows an application circuit.
For best results, this IC should be operated with $V_O = 2.0$ V.

$V_O\ (V) = V_{CC} - V_{OUT}$
$= V_{CC} - V_f\ (LED) - V_{CE1}$

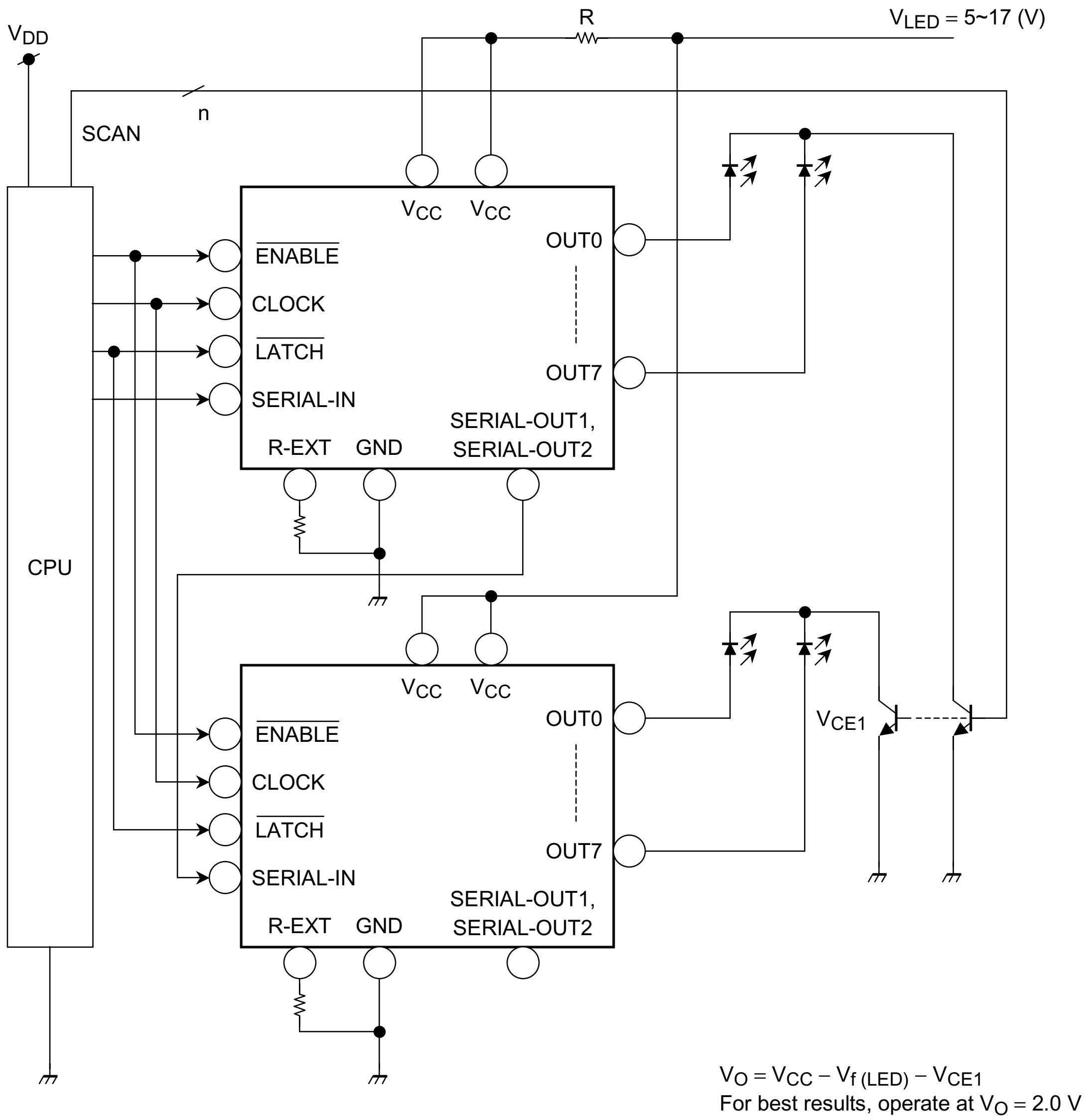
When $V_{CC}$ is high and the $V_f$ of the LED is low.
$V_O$ is also high , the increase in power dissipation may in turn adversely affect the IC's output current.
In this case, reduce the voltage by connecting an external resistor.
In this way the IC's output current can be stabilized.

$$R = \frac{V_{CC} - V_f - V_O\ (min)}{I_{OUT}\ (max) \times BIT\ number\ (max)}$$

It is looked for.

it is also possible that the IC will operate in an unstable manner due to the inductance of the wiring.
To counter this, it is recommended that the IC be situated as close as possible on the PCB to the LED module, and as far as possible from other ICs. Otherwise, there is the risk that the IC will malfunction.

## Application



## Notes

- Operation may become unstable due to the electromagnetic interference caused by the wiring and other phenomena.
  To counter this, it is recommended that the IC be situated as close as possible to the LED module.
  If overvoltage is caused by inductance between the LED and the output terminals, both the LED and the terminals may suffer damage as a result.

- There is only one GND terminal on this device when the inductance in the GND line and the resistor are large, the device may malfunction due to the GND noise when output switchings by the circuit board pattern and wiring.
  To achieve stable operation, it is necessary to connect a resistor between the REXT terminal and the GND line.
  Fluctuation in the output waveform is likely to occur when the GND line is unstable or when a capacitor (of more than 50 pF) is used.
  Therefore, take care when designing the circuit board pattern layout and the wiring from the controller.

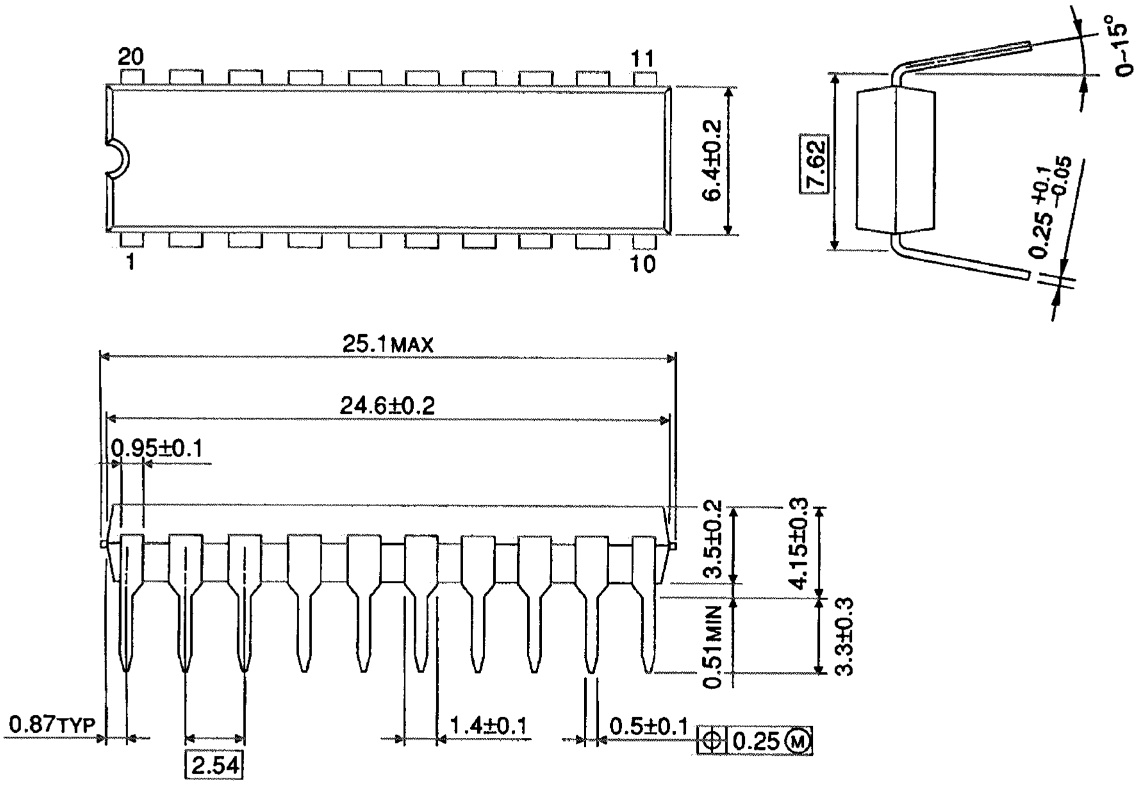
- This application circuit is a reference example and is not guaranteed to work in all conditions.
  Be sure to check the operation of your circuits.

- This device does not include protection circuits for overvoltage, overcurrent or overtemperature.
  If protection is necessary, it must be incorporated into the control circuitry.

- The device is likely to be destroyed if a short-circuit occurs between either of the power supply pins and any of the output terminals when designing circuits, pay special attention to the positions of the output terminals and the power supply terminals ($V_{DD}$ and $V_{LED}$), and to the design of the GND line.

## Package Dimensions

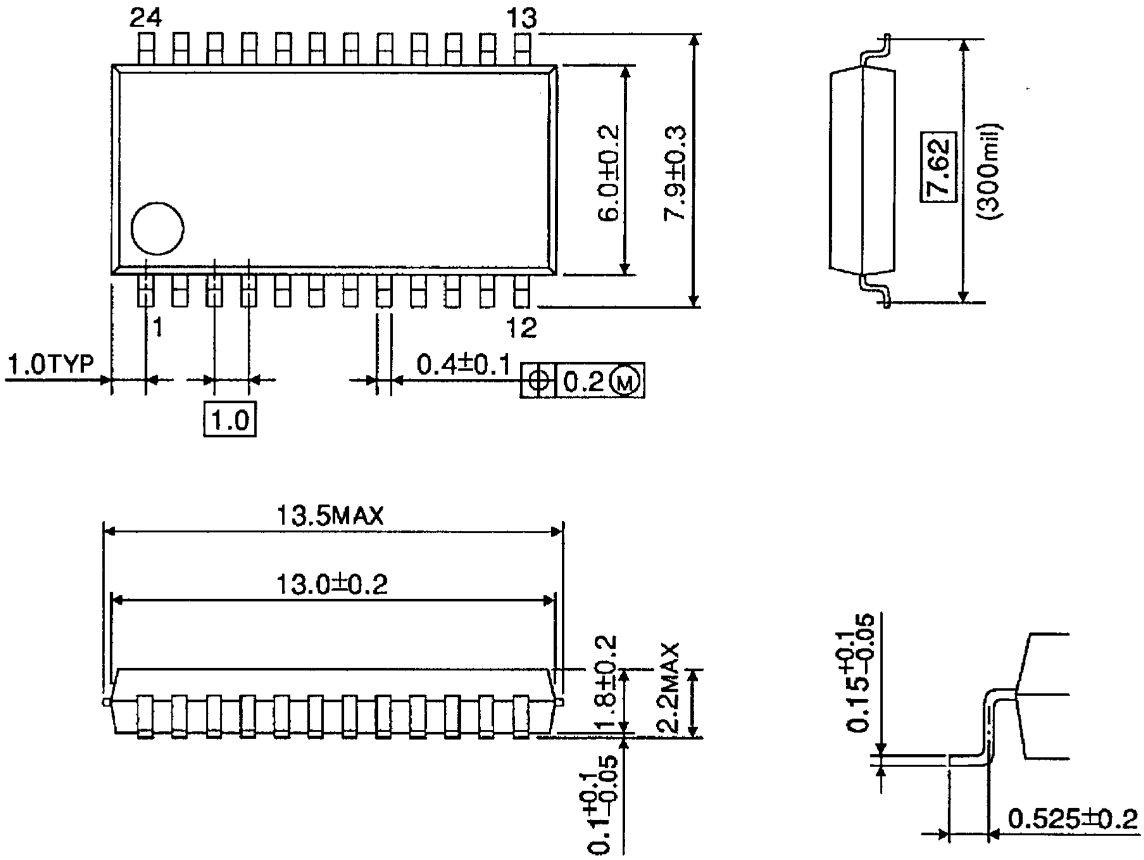
DIP20-P-300-2.54A Unit : mm




質量: 2.25 g (標準)

## Package Dimensions

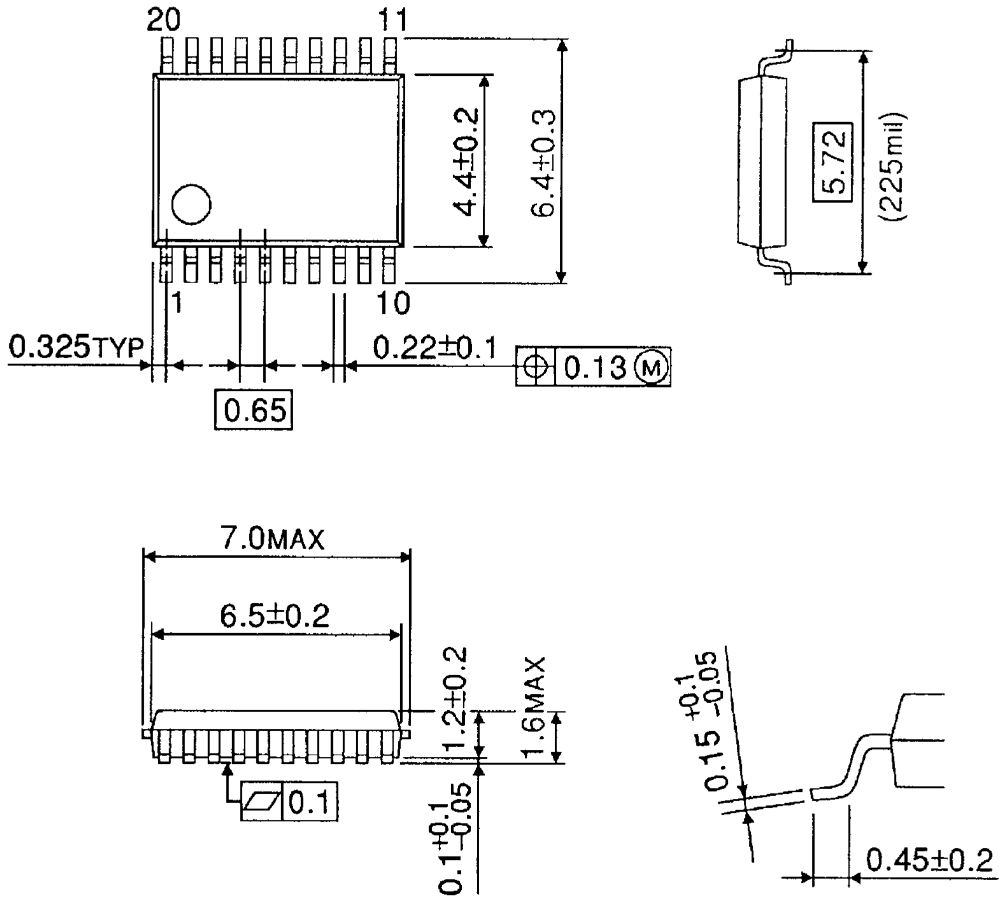
SSOP24-P-300-1.00 Unit : mm




質量: 0.33 g (標準)

## Package Dimensions

SSOP20-P-225-0.65A Unit : mm




質量: .0.10 g (標準)

## RESTRICTIONS ON PRODUCT USE