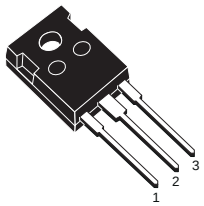
# STW47NM50

## N-CHANNEL 500V - 0.065Ω - 45A TO-247
## MDmesh™ Power MOSFET

**ADVANCED DATA**

| TYPE | $V_{DSS}$ | $R_{DS(on)}$ | $R_{ds(on)}*Q_g$ | $I_D$ |
|---|---|---|---|---|
| STW47NM50 | 500V | < 0.085Ω | 5.6 Ω*nC | 45 A |

- TYPICAL $R_{DS}(on)$ = 0.065Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS




**TO-247**

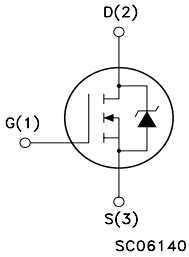
### DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

### APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

### INTERNAL SCHEMATIC DIAGRAM




### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source Voltage ($V_{GS}$ = 0) | 500 | V |
| $V_{DGR}$ | Drain-gate Voltage ($R_{GS}$ = 20 kΩ) | 500 | V |
| $V_{GS}$ | Gate- source Voltage | ±30 | V |
| $I_D$ | Drain Current (continuous) at $T_C$ = 25°C | 45 | A |
| $I_D$ | Drain Current (continuous) at $T_C$ = 100°C | 28.4 | A |
| $I_{DM}$ (•) | Drain Current (pulsed) | 180 | A |
| $P_{TOT}$ | Total Dissipation at $T_C$ = 25°C | 417 | W |
| | Derating Factor | 2.08 | W/°C |
| dv/dt (1) | Peak Diode Recovery voltage slope | 15 | V/ns |
| $T_{stg}$ | Storage Temperature | –65 to 150 | °C |
| $T_j$ | Max. Operating Junction Temperature | 150 | °C |

(•)Pulse width limited by safe operating area

(1) $I_{SD}$ ≤45A, di/dt ≤400A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX.}$

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| Rthj-case | Thermal Resistance Junction-case | Max | 0.3 | °C/W |
| Rthj-amb | Thermal Resistance Junction-ambient | Max | 30 | °C/W |
| $T_l$ | Maximum Lead Temperature For Soldering Purpose | | 300 | °C |

## AVALANCHE CHARACTERISTICS

| Symbol | Parameter | Max Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max) | 20 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (starting $T_j$ = 25 °C, $I_D = I_{AR}$, $V_{DD}$ = 35 V) | 810 | mJ |

## ELECTRICAL CHARACTERISTICS ($T_{CASE}$ = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D$ = 250 µA, $V_{GS}$ = 0 | 500 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating | | | 10 | µA |
| | | $V_{DS}$ = Max Rating, $T_C$ = 125 °C | | | 100 | µA |
| $I_{GSS}$ | Gate-body Leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ±30 V | | | ±100 | nA |

ON (1)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 22.5 A | | 0.065 | 0.085 | Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward Transconductance | $V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D$ = 22.5A | | 20 | | S |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25V, f = 1 MHz, $V_{GS}$ = 0 | | 3700 | | pF |
| $C_{oss}$ | Output Capacitance | | | 610 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 50 | | pF |
| $C_{oss\ eq.}$ (2) | Equivalent Output Capacitance | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 400V | | 325 | | pF |
| $R_G$ | Gate Input Resistance | f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain | | 1.7 | | Ω |

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.

**ELECTRICAL CHARACTERISTICS** (CONTINUED)

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}$ = 250V, $I_D$ = 22.5 A<br>$R_G$ = 4.7Ω $V_{GS}$ = 10 V<br>(see test circuit, Figure 3) | | 40 | | ns |
| $t_r$ | Rise Time | | | 35 | | ns |
| $Q_g$ | Total Gate Charge | $V_{DD}$ = 400 V, $I_D$ = 45 A,<br>$V_{GS}$ = 10 V | | 87 | 117 | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 23 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 42 | | nC |

SWITCHING OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{r(Voff)}$ | Off-voltage Rise Time | $V_{DD}$ = 400 V, $I_D$ = 45 A,<br>$R_G$ = 4.7Ω, $V_{GS}$ = 10 V<br>(see test circuit, Figure 5) | | 18 | | ns |
| $t_f$ | Fall Time | | | 23 | | ns |
| $t_c$ | Cross-over Time | | | 44 | | ns |

SOURCE DRAIN DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain Current | | | | 45 | A |
| $I_{SDM}$ (2) | Source-drain Current (pulsed) | | | | 180 | A |
| $V_{SD}$ (1) | Forward On Voltage | $I_{SD}$ = 45 A, $V_{GS}$ = 0 | | | 1.5 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 40 A, di/dt = 100A/µs,<br>$V_{DD}$ = 100 V, $T_j$ = 25°C<br>(see test circuit, Figure 5) | | 520<br>7.8<br>30 | | ns<br>µC<br>A |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 40 A, di/dt = 100A/µs,<br>$V_{DD}$ = 100 V, $T_j$ = 150°C<br>(see test circuit, Figure 5) | | 680<br>11.2<br>33 | | ns<br>µC<br>A |

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

**Fig. 1:** Unclamped Inductive Load Test Circuit

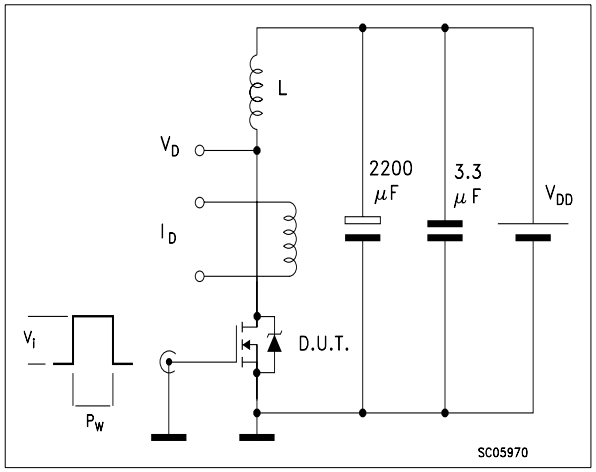



**Fig. 2:** Unclamped Inductive Waveform

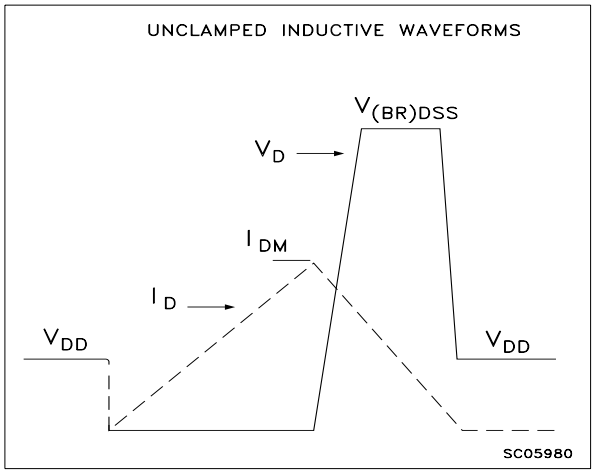



**Fig. 3:** Switching Times Test Circuit For Resistive Load

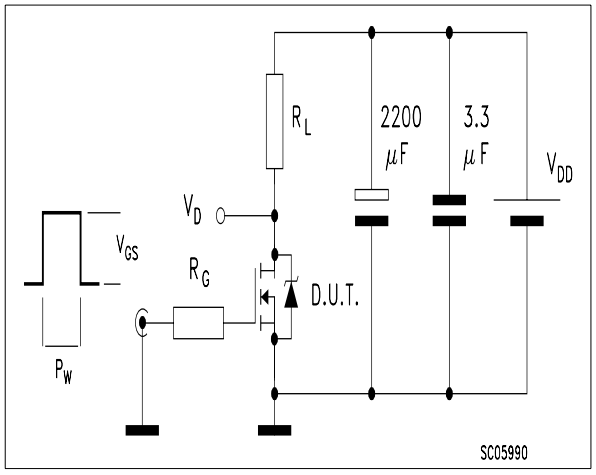



**Fig. 4:** Gate Charge test Circuit

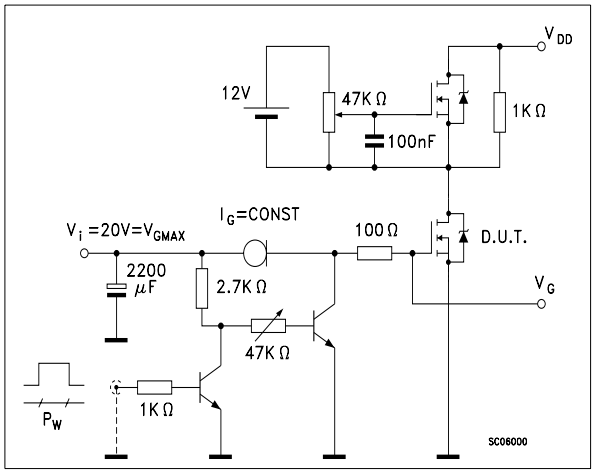
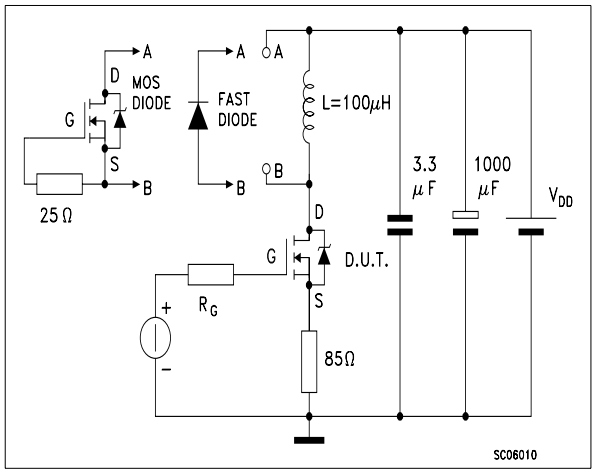



**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times



# TO-247 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 4.85 | | 5.15 | 0.19 | | 0.20 |
| D | 2.20 | | 2.60 | 0.08 | | 0.10 |
| E | 0.40 | | 0.80 | 0.015 | | 0.03 |
| F | 1 | | 1.40 | 0.04 | | 0.05 |
| F1 | | 3 | | | 0.11 | |
| F2 | | 2 | | | 0.07 | |
| F3 | 2 | | 2.40 | 0.07 | | 0.09 |
| F4 | 3 | | 3.40 | 0.11 | | 0.13 |
| G | | 10.90 | | | 0.43 | |
| H | 15.45 | | 15.75 | 0.60 | | 0.62 |
| L | 19.85 | | 20.15 | 0.78 | | 0.79 |
| L1 | 3.70 | | 4.30 | 0.14 | | 0.17 |
| L2 | | 18.50 | | | 0.72 | |
| L3 | 14.20 | | 14.80 | 0.56 | | 0.58 |
| L4 | | 34.60 | | | 1.36 | |
| L5 | | 5.50 | | | 0.21 | |
| M | 2 | | 3 | 0.07 | | 0.11 |
| V | | 5º | | | 5º | |
| V2 | | 60º | | | 60º | |
| Dia | 3.55 | | 3.65 | 0.14 | | 0.143 |