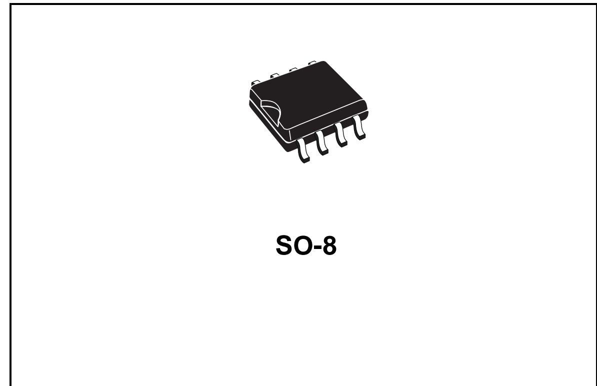
STS2DPF20V

DUAL P-CHANNEL 20V - 0.14Ω - 2A SO-8 2.7V-DRIVE STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS2DPF20V	20 V	$<0.20\Omega$ (@4.5V) $<0.25\Omega$ (@2.7V)	2 A

- TYPICAL R_{DS}(on) = 0.14Ω (@4.5V)
- TYPICAL R_{DS}(on) = 0.2Ω (@2.7V)
- ULTRA LOW THRESHOLD GATE DRIVE (2.7V)
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY



SO-8

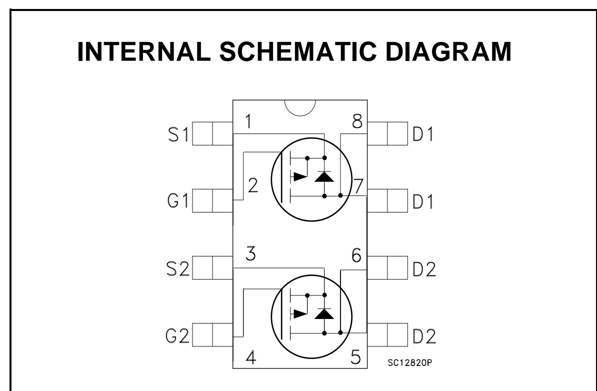
DESCRIPTION

This Power MOSFET is the second generation of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- BATTERY MANAGMENT IN NOMADIC EQUIPMENT
- POWER MANAGMENT IN CELLULAR PHONES

INTERNAL SCHEMATIC DIAGRAM



MOSFET ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	20	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	20	V
V_{GS}	Gate- source Voltage	± 12	V
I_D	Drain Current (continuos) at T_C = 25°C Single Operation Drain Current (continuos) at T_C = 100°C Single Operation	2 1.26	A A
I_{DM} (●)	Drain Current (pulsed)	8	A
P_{TOT}	Total Dissipation at T_C = 25°C Dual Operation Total Dissipation at T_C = 25°C Single Operation	1.6 2	W W

(●)Pulse width limited by safe operating area.

Note: For the P-CHANNEL MOSFET actual polarity of Voltages and current has to be reversed

THERMAL DATA

Rthj-amb	(*)Thermal Resistance Junction-ambient Single Operation Dual Operation	62.5 78	°C/W °C/W
T_{stg}	Storage Temperature	-55 to 150	°C
T_j	Junction-ambient Temperature	-55 to 150	°C
	(*) When Mounted on 0.5 in² of 2 oz. Copper		

MOSFET ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	20			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 12 V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.6			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 4.5 V, I_D = 1 A		0.14	0.20	Ω
		V_{GS} = 2.7 V, I_D = 1 A		0.20	0.25	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D = 1.5 A		4.5		S
C_{iss}	Input Capacitance	V_{DS} = 15V, f = 1 MHz, V_{GS} = 0		315		pF
C_{oss}	Output Capacitance			87		pF
C_{rss}	Reverse Transfer Capacitance			17		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 10 V, I_D = 1.5A R_G = 4.7Ω V_{GS} = 4.5V (see test circuit, Figure 1)		38 30		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 10V, I_D = 2 A, V_{GS} = 4.5 V (see test circuit, Figure 2)		3.8 0.34 0.8	4.8	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 10 V, I_D = 1 A, R_G = 4.7Ω, V_{GS} = 4.5 V (see test circuit, Figure 1)		45 11		ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				2 8	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 2 A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 2 A, di/dt = 100A/µs, V_{DD} = 10 V, T_j = 150°C (see test circuit, Figure 3)		15 7.5 1		ns nC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Switching Times Test Circuit For Resistive Load

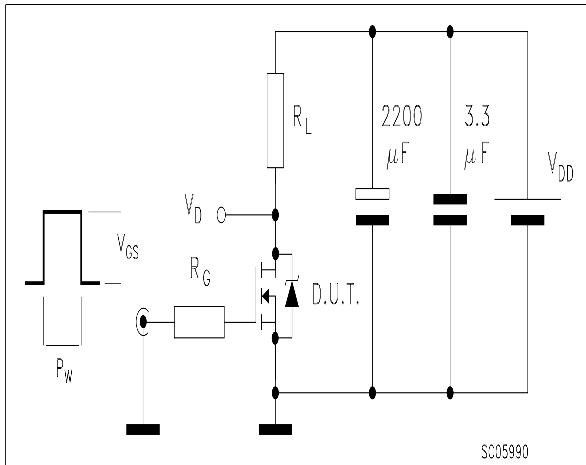


Fig. 2: Gate Charge test Circuit

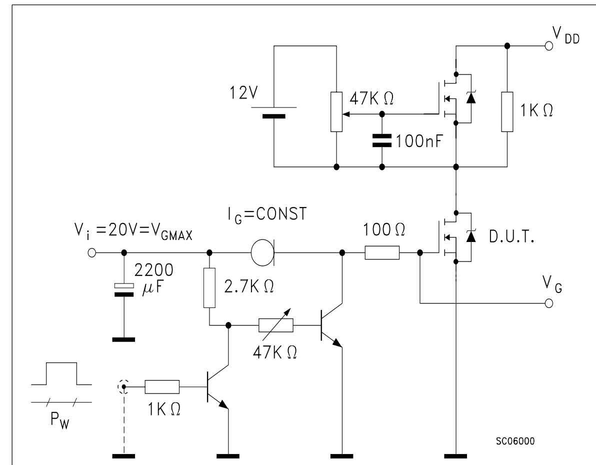
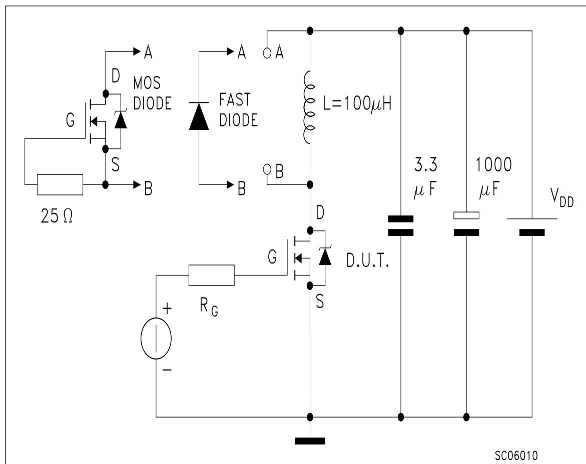
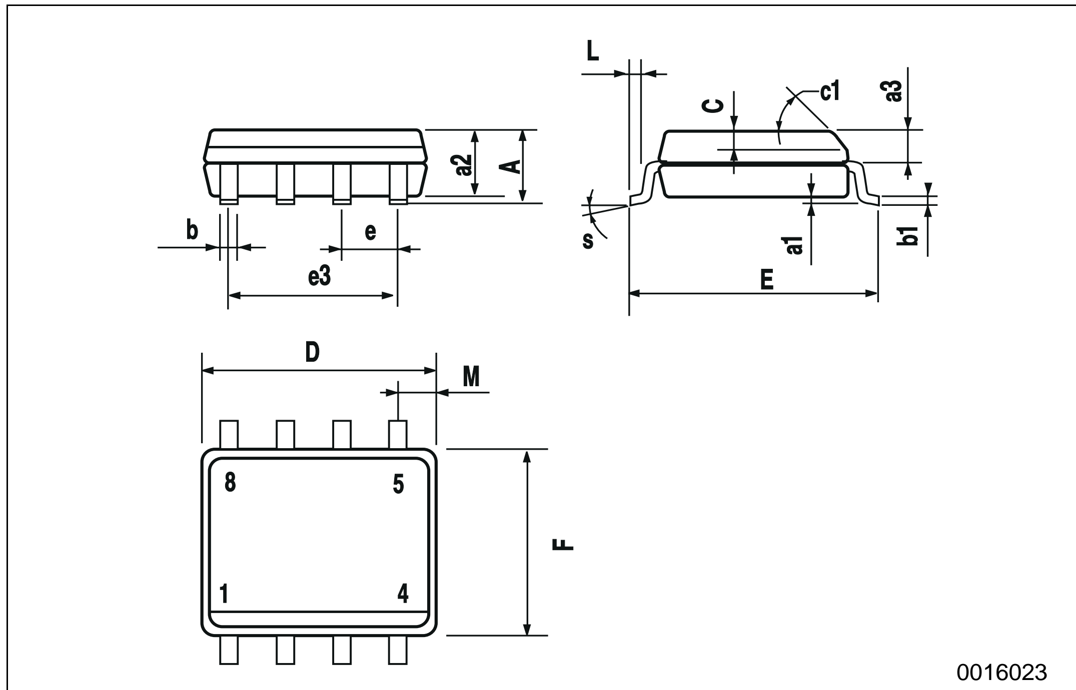


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

http://www.st.com