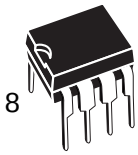
SGS-THOMSON MICROELECTRONICS

ST95P02

SERIAL ACCESS SPI BUS 2K (256 x 8) EEPROM

NOT FOR NEW DESIGN

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE 3V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- ***The ST95P02 will be replaced shortly by the updated version ST95020***



PSDIP8 (B)
0.25mm Frame

SO8 (M)

DESCRIPTION

The ST95P02 is a 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The 2K bit memory is organised as 16 pages of 16 bytes. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q). The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

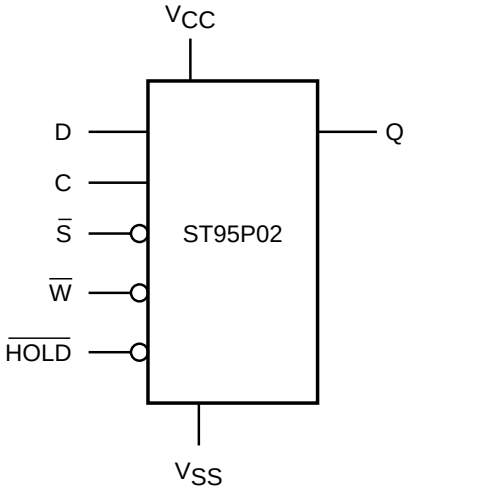


Figure 2A. DIP Pin Connections

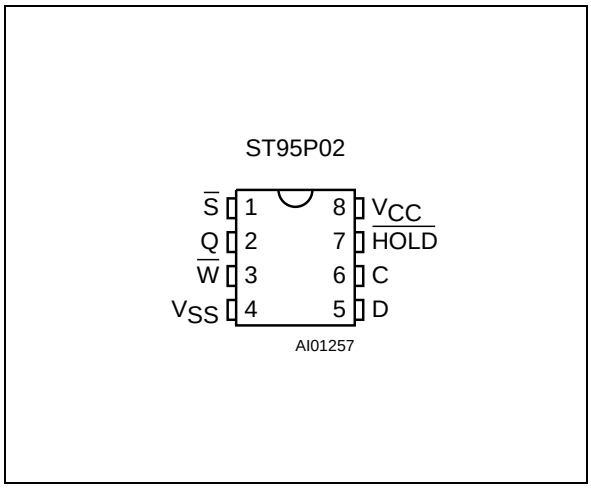


Figure 2B. SO Pin Connections

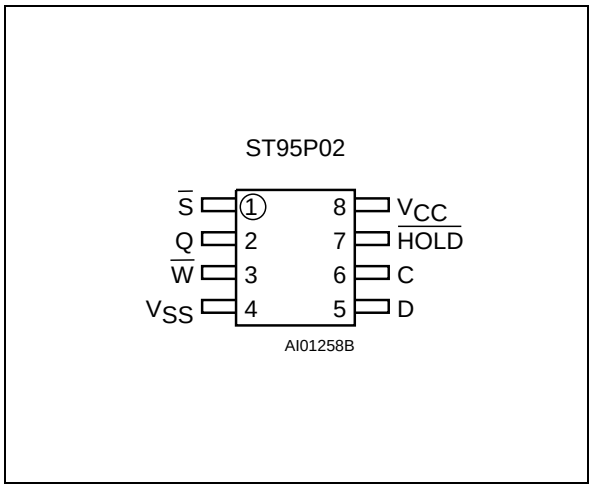


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

SIGNALS DESCRIPTION

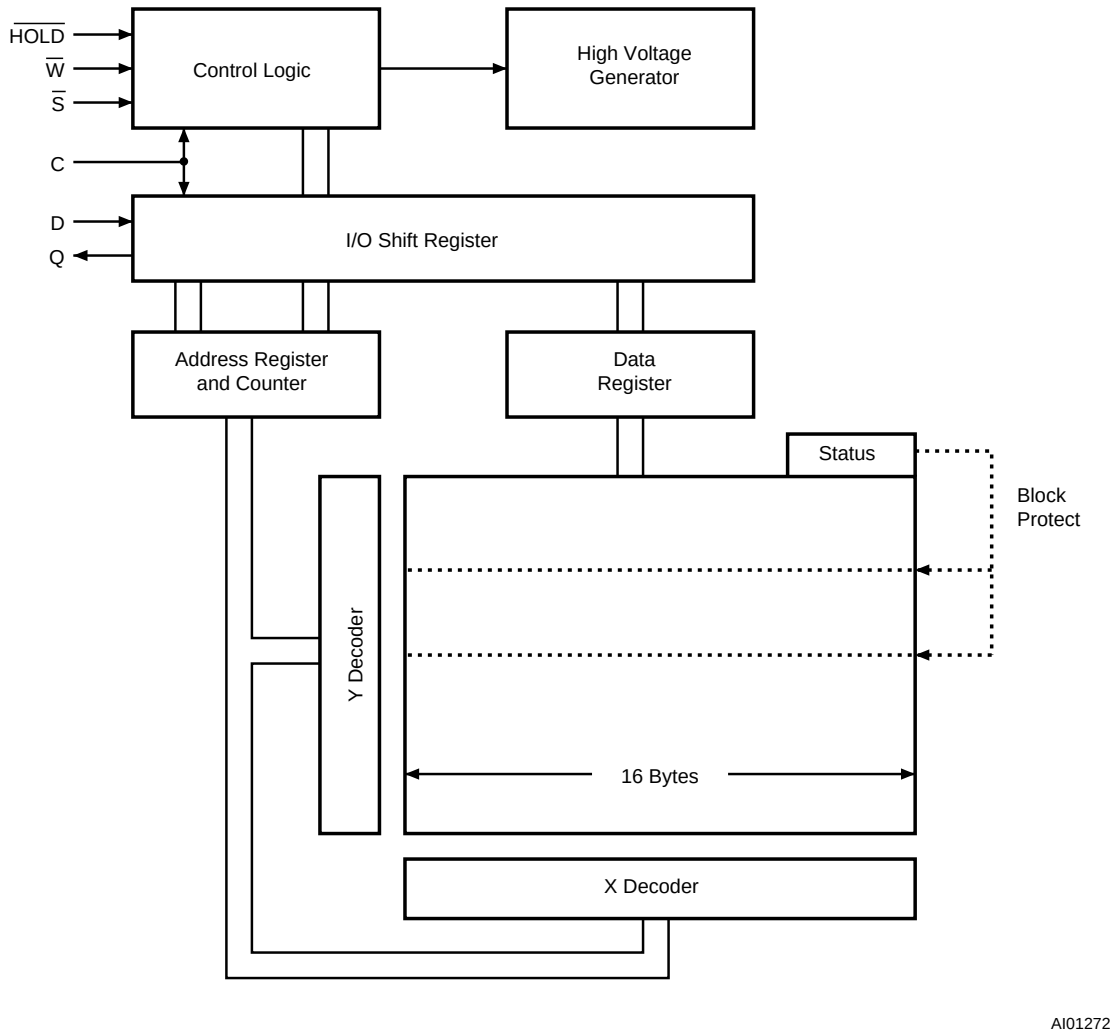
Serial Output (Q). The output pin is used to transfer data serially out of the ST95P02. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the rising edge of the serial clock.

Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). This input is used to select the ST95P02. The chip is selected by a high to low transition on the $\overline{S}$ pin when C is at '0' state. At any time, the chip is deselected by a low to high transition on the $\overline{S}$ pin when C is at '0' state. As soon as the chip is deselected, the Q pin is at high impedance state. This pin allows multiple ST95P02 to share the same SPI bus. After power up, the chip is at the deselect state. Transitions of $\overline{S}$ are ignored when C is at '1' state.

Figure 3. Block Diagram



AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Input Output Waveforms

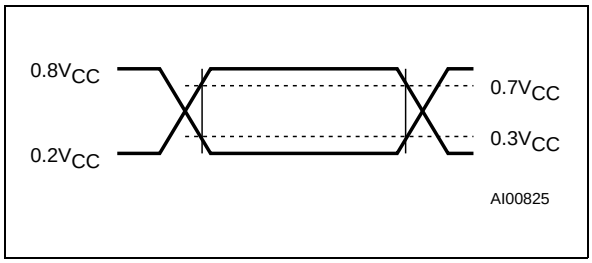


Table 3. Input Parameters (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width		10	ns

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , @ 2 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V		50	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3V		10	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –2mA	0.8 V_{CC}		V

Table 5. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	2	MHz
t_{SLCH}	t_{SU}	$\overline{S}$ Setup Time		50		ns
t_{CLSH}	t_{SH}	$\overline{S}$ Hold Time		50		ns
t_{CH}	t_{WH}	Clock High Time		200		ns
t_{CL}	t_{WL}	Clock Low Time		300		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		50		ns
t_{CHDX}	t_{DH}	Data In Hold Time		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HXCH}	t_{HSU}	$\overline{HOLD}$ Setup Time		50		ns
t_{CLHX}	t_{HH}	$\overline{HOLD}$ Hold Time		50		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	4.5V < V_{CC} < 5.5V	200		ns
			3V < V_{CC} < 4.5V	250		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			150	ns
t_{QVCL}	t_V	Clock Low to Output Valid			300	ns
t_{CLQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			100	ns
t_{QHQL}	t_{FO}	Output Fall Time			100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			150	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z			150	ns
t_W (1)	t_W	Write Cycle Time			10	ms

Note: 1. Not enough characterisation data were available on this parameter at the time of issue this Data Sheet. The typical value is well below 5ms, the maximum value will be reviewed and lowered when sufficient data is available.

Figure 5. Output Timing

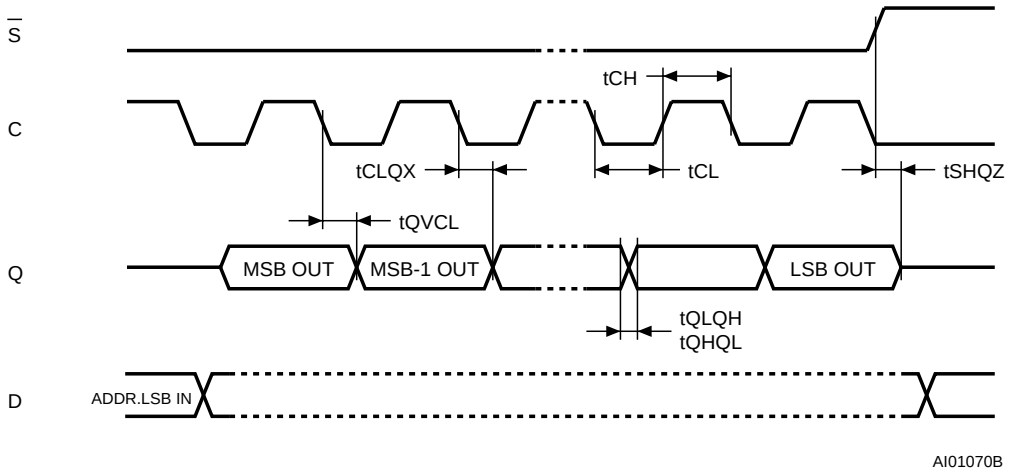


Figure 6. Serial Input Timing

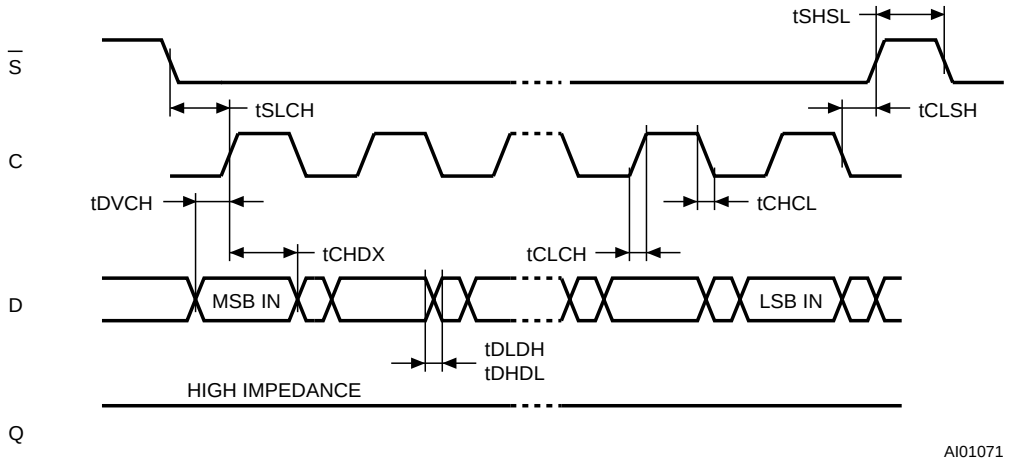
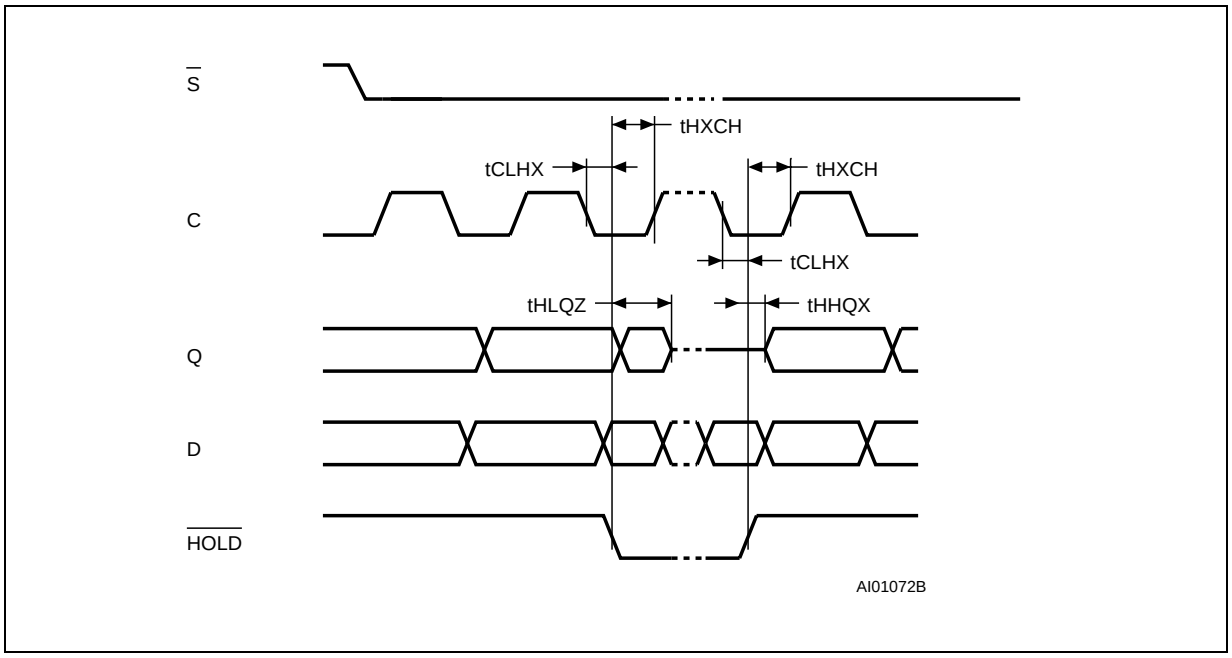


Figure 7. Hold Timing



Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes to the ST95P02 are disabled but any other operation stays enabled. When $\overline{W}$ is high, all operations including non-volatile writes are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with a ST95P02 without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95P02 is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 7 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 7), the chip is automatically deselected.

Write Enable (WREN) and Write Disable (WRDI)

The ST95P02 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95P02, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the ST95P02 enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and Write bits
WEL, WIP: Read only bits.

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a non volatile write to the status register, the only bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read only bit indicates whether the ST95P02 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset.

The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95P02 is divided into four 512 bit blocks. The user may read the blocks but will be unable to write within the selected blocks.

The blocks and respective WRSR control bits are shown in Table 6.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear after the 8th bit of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Then, the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out.

Table 6. Array Addresses Protect

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	none
0	1	C0h - FFh
1	0	80h - FFh
1	1	00h - FFh

Table 7. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
WRITE	Write Data to Memory Array	0000 0010

OPERATIONS (cont'd)

When the highest address is reached (FFh), the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95P02 will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing a one byte address (A7-A0), and one byte of data. $\overline{S}$ must remain low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur at the clock low pulse just after the eigth bit of data of a word is received.

Figure 8. Read Operation Sequence

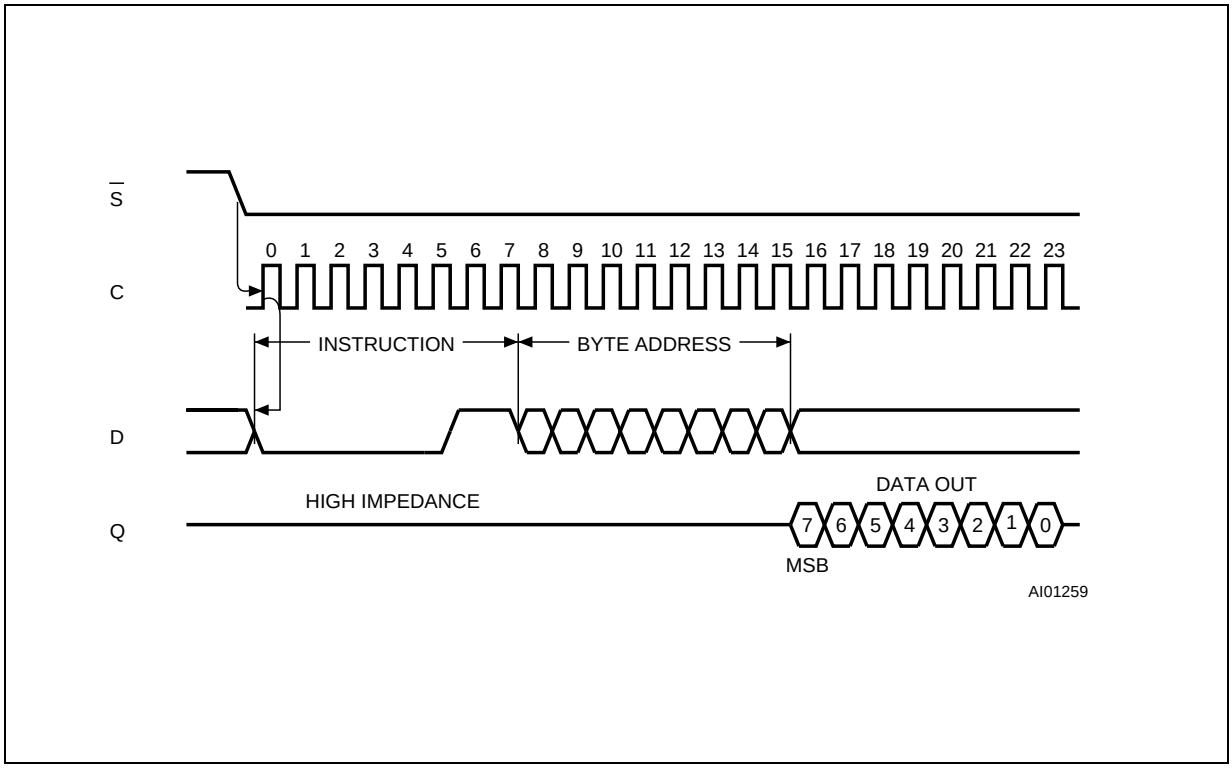


Figure 9. Write Enable Latch Sequence

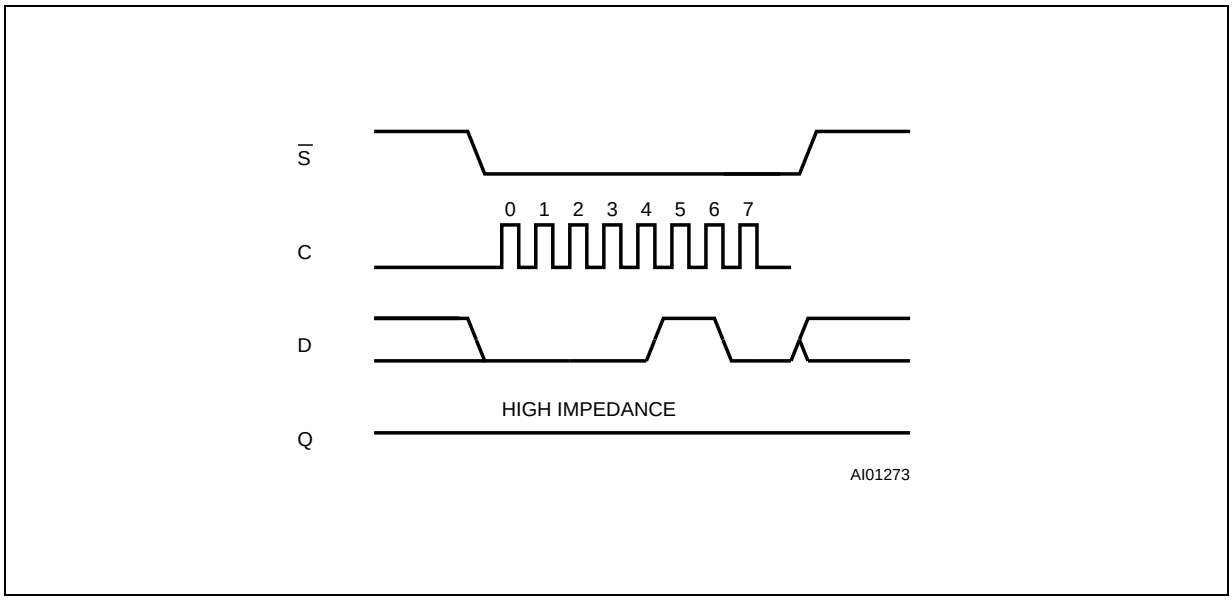


Figure 10. Write Operation Sequence

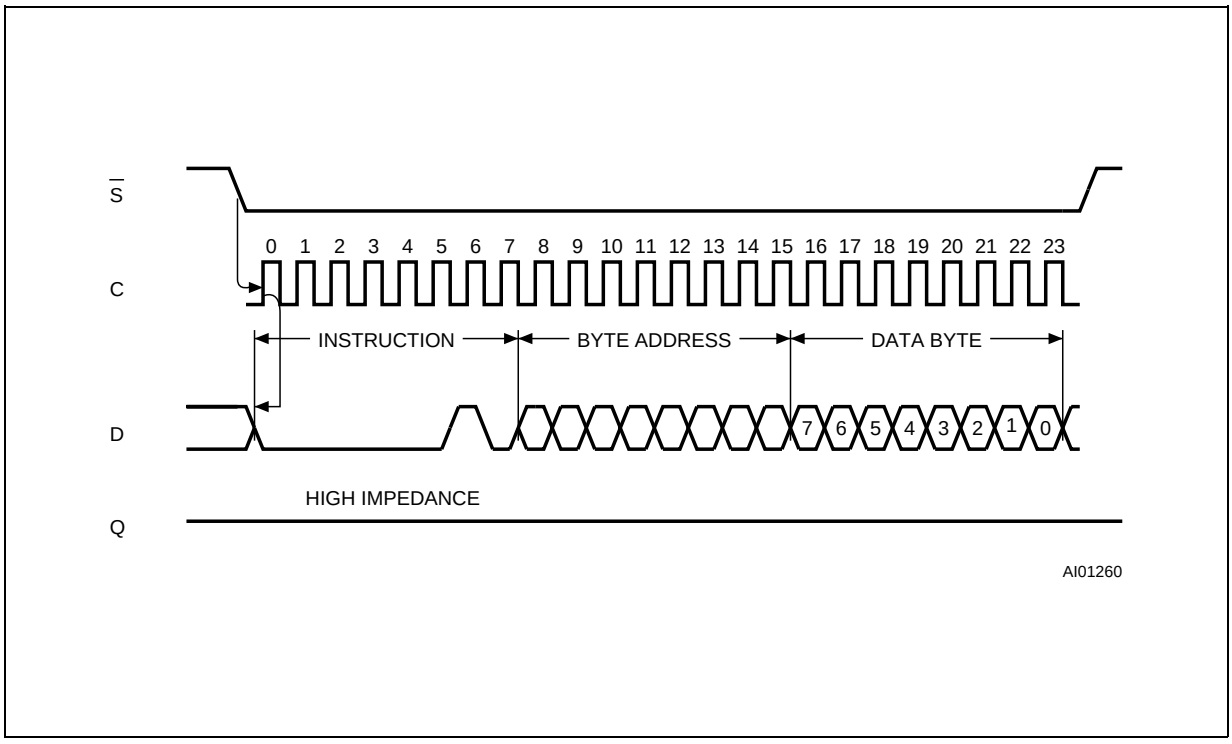


Figure 11. Page Write Operation Sequence

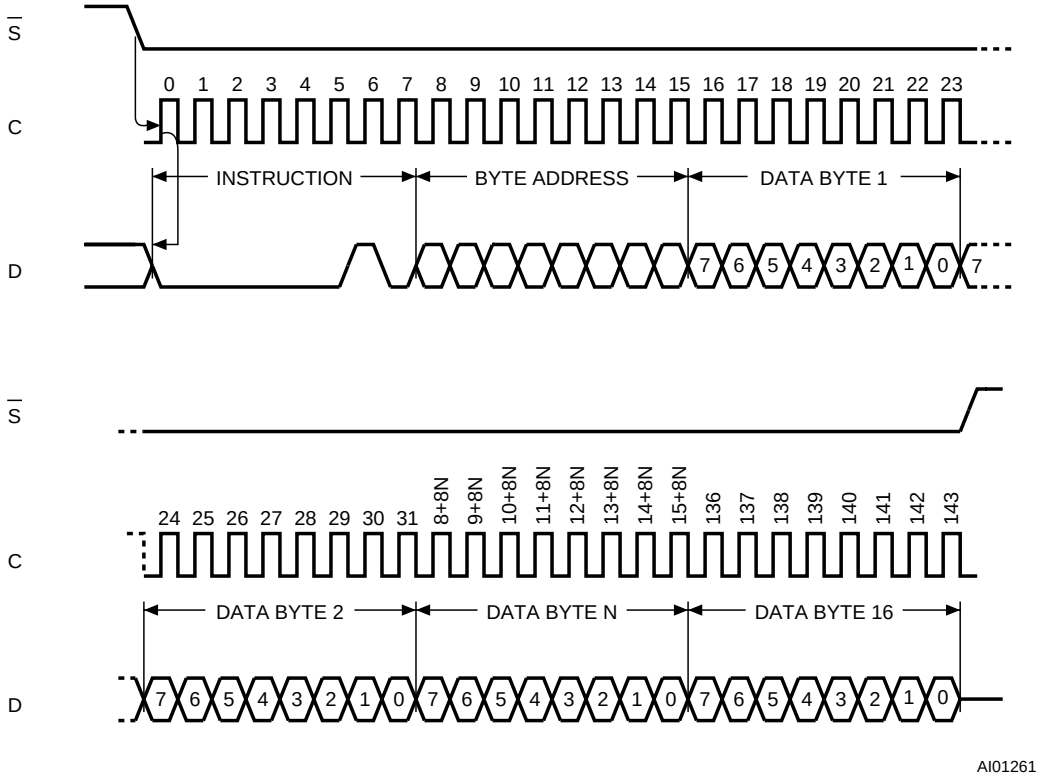


Figure 12. RDSR: Read Status Register Sequence

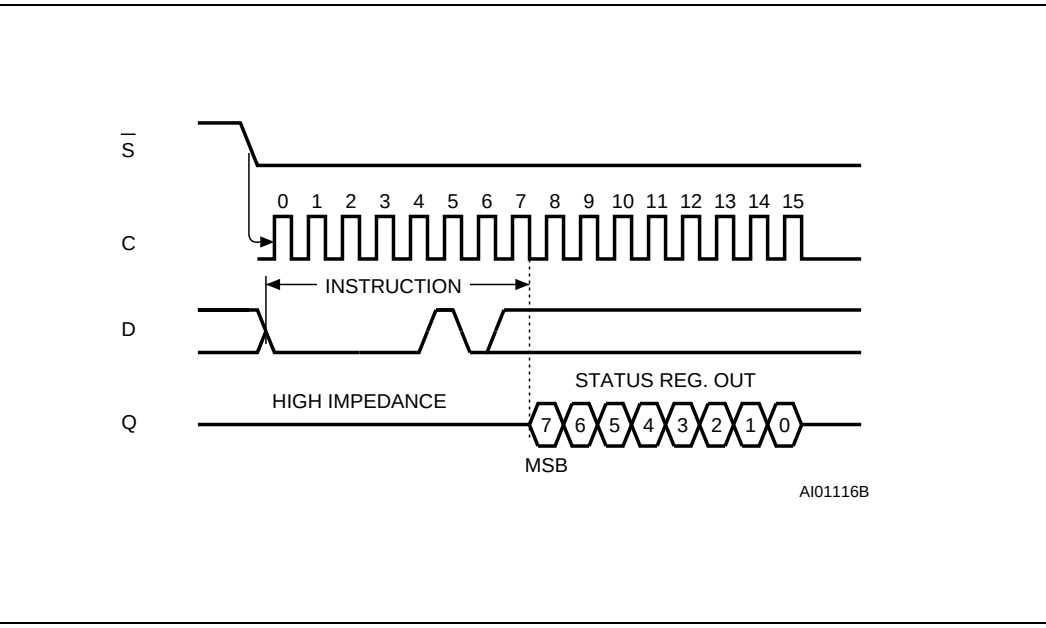
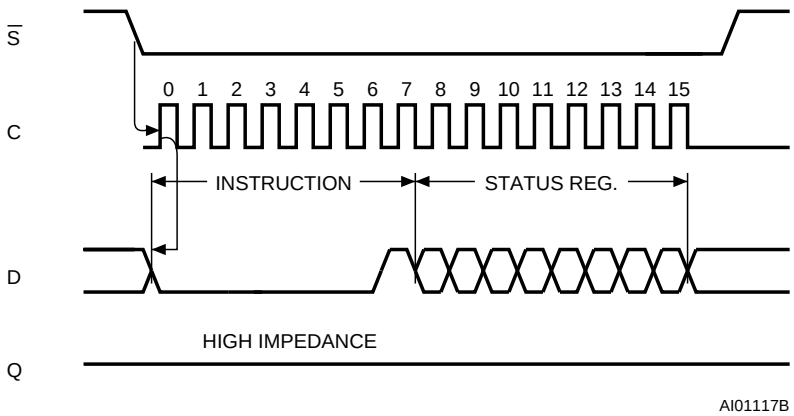


Figure 13. WRSR: Write Status Register Sequence



POWER ON STATE

After a Power up the ST95P02 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

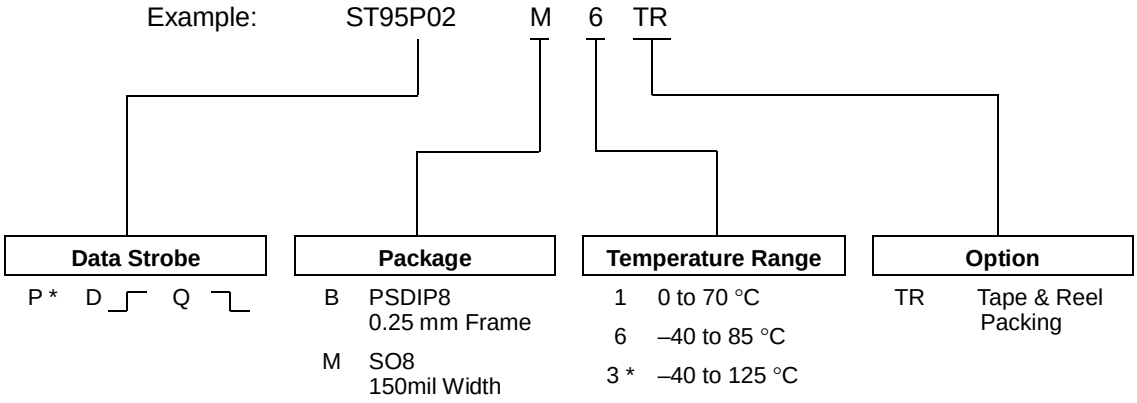
DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 3.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register). The Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

ORDERING INFORMATION SCHEME



Notes: P * Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock.
3 * Temperature range on special request only.

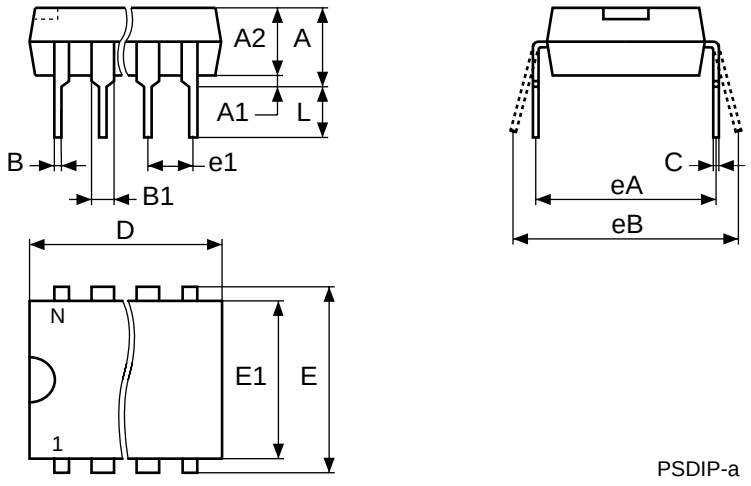
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8



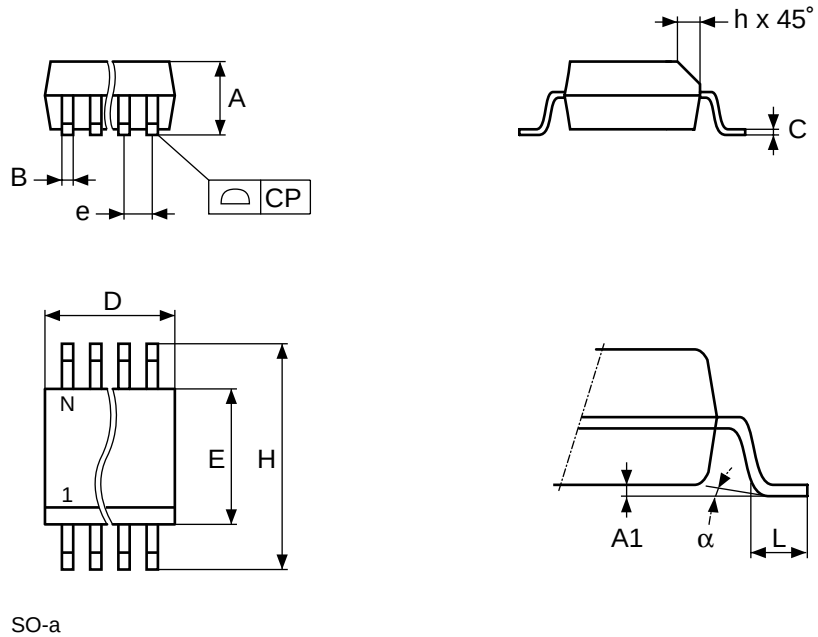
PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



SO-a

Drawing is not to scale