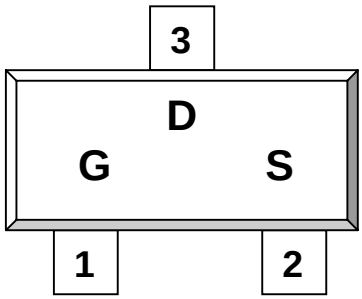
P Channel Enchancement Mode MOSFET ST3403

-3.5A

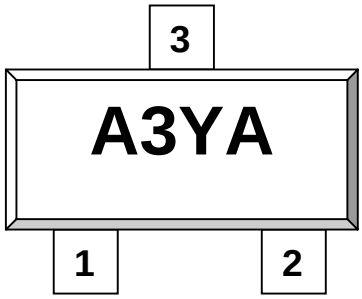
DESCRIPTION

The ST3403 is the P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits, and low in-line power loss are needed in a very small outine surface mount package.

PIN CONFIGURATION
SOT-23-3L



1.Gate 2.Source 3.Drain



Y: Year Code A: Process Code

FEATURE

- -30V/-2.8A, $R_{DS(ON)}$ = 105m-ohm @VGS = -10V
- -30V/-2.5A, $R_{DS(ON)}$ = 115m-ohm @VGS = -4.5V
- -30V/-1.5A, $R_{DS(ON)}$ = 155m-ohm @VGS = -2.5V
- -30V/-1.0A, $R_{DS(ON)}$ =255m-ohm
- @VGS = -1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

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ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	+/-12	V
Continuous Drain Current (T_J=150°C)	T_A=25°C T_A=70°C	I_D	-3.5 -2.8	A
Pulsed Drain Current		I_{DM}	-20	A
Continuous Source Current (Diode Conduction)		I_S	-1.4	A
Power Dissipation	T_A=25°C T_A=70°C	P_D	1.25 0.81	W
Operation Junction Temperature		T_J	150	°C
Storgae Temperature Range		T_{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	105	°C/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-0.4		-1.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V			-1	uA
		V_{DS}=-24V,V_{GS}=0V T_J=85℃			-5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≧-5V,V_{GS}=-4.5V	-4			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-2.8A		0.09	0.105	Ω
		V_{GS}=-4.5V,I_D=-2.5A		0.100	0.115	
		V_{GS}=-2.5V,I_D=-1.5A		0.140	0.155	
		V_{GS}=-1.8V,I_D=-1.0A		0.200	0.255	
Forward Transconductance	g_{fs}	V_{DS}=-10V,I_D=-2.8A		4		S
Diode Forward Voltage	V_{SD}	I_S=-1.2A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Qg	V_{DS}=-15V,V_{GS}=-4.5V I_D≡-2.0A		5.8		nC
Gate-Source Charge	Qgs			0.8		
Gate-Drain Charge	Qgd			1.5		
Input Capacitance	Ciss	V_{DS}=-15V,V_{GS}=0V F=1MHz		380		pF
Output Capacitance	Coss			55		
Reverse Transfer Capacitance	Crss			40		
Turn-On Time	$t_{d(on)}$	V_{DD}=-15V,R_L=15Ω V_{GEN}=-10V,R_G=3Ω I_D≡-1.0A		6		nS
	t_r			3.9		
Turn-Off Time	$t_{d(off)}$			40		
	t_f			15		

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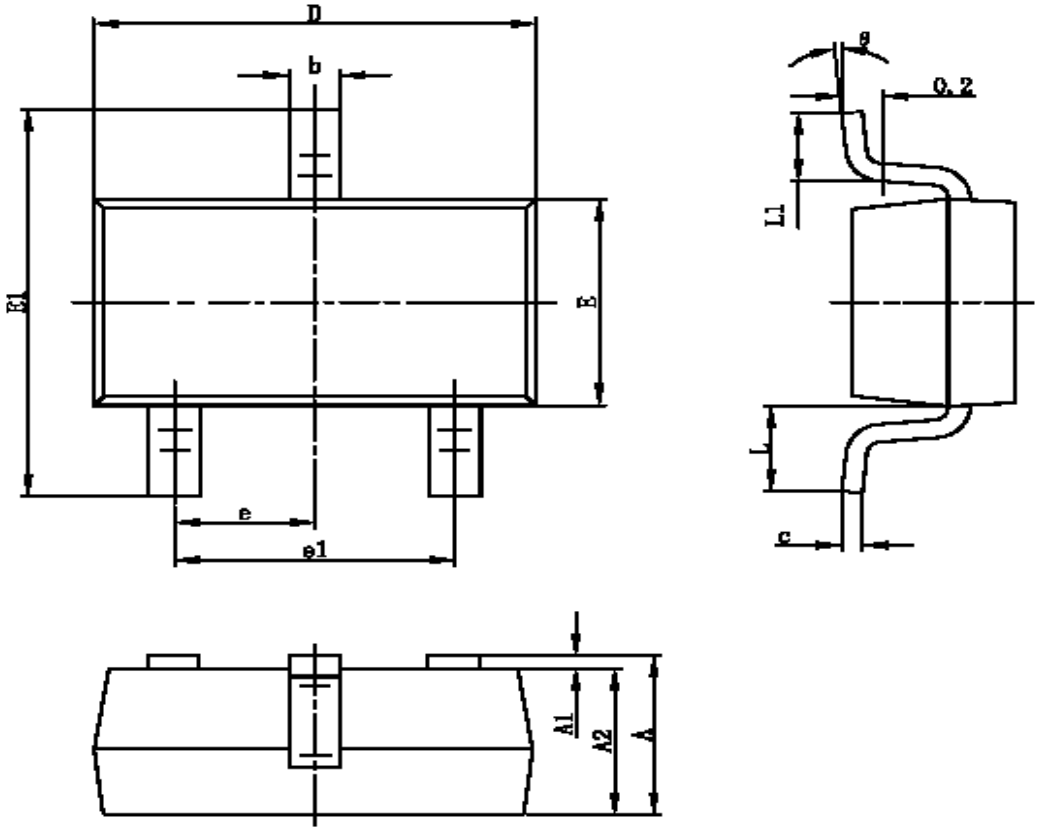
SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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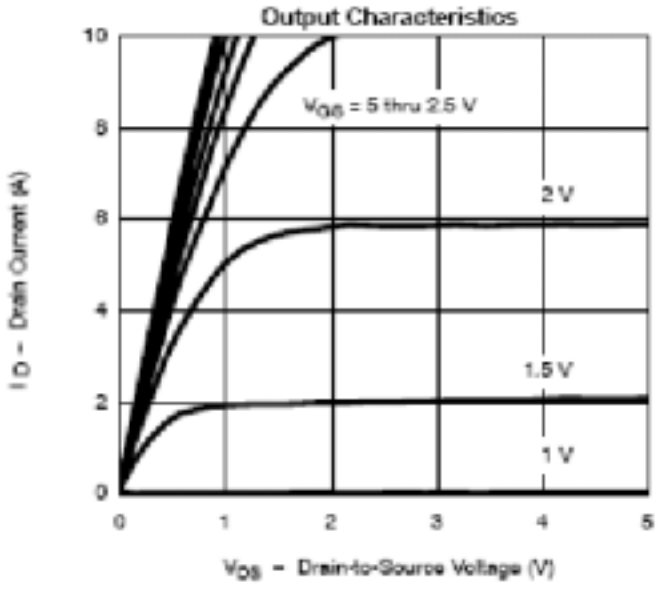
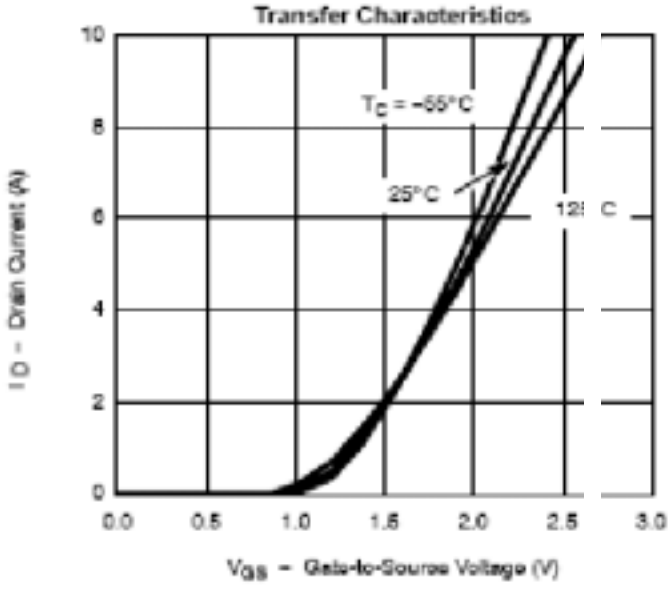
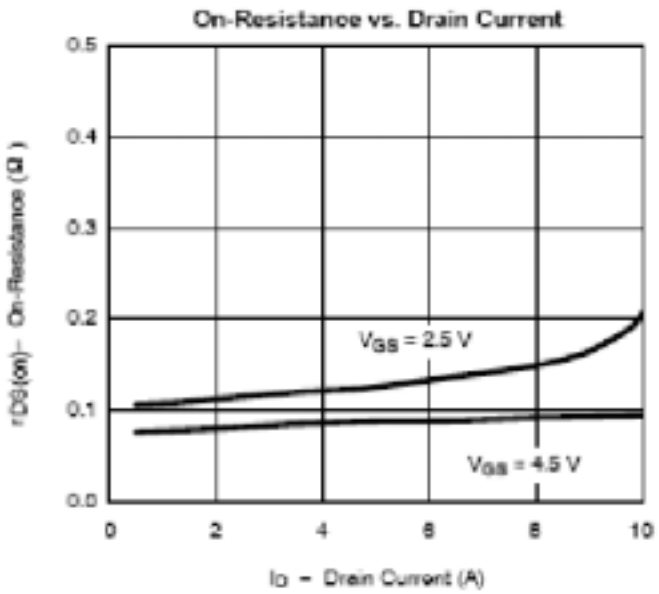
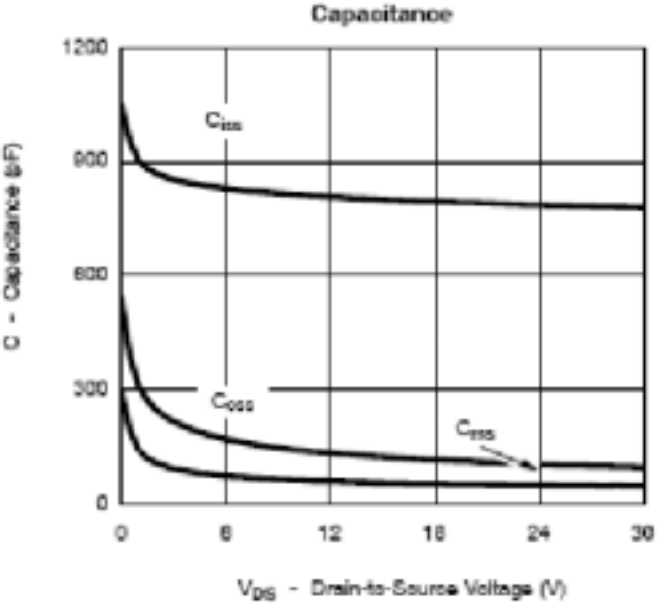
TYPICAL CHARACTERISTICS









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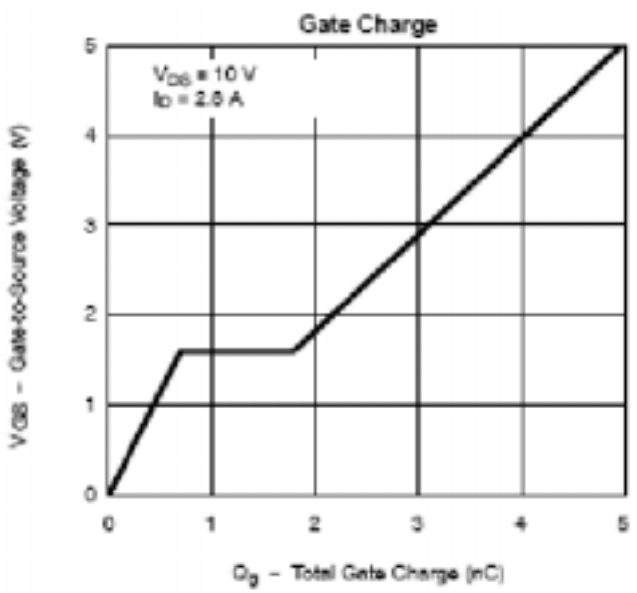

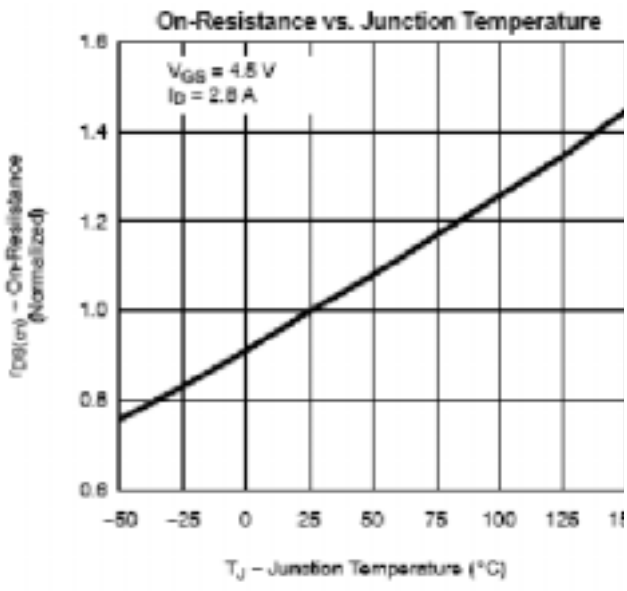

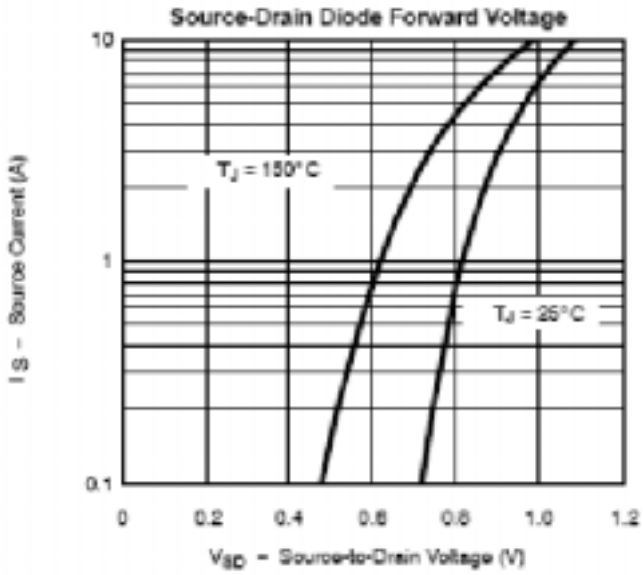

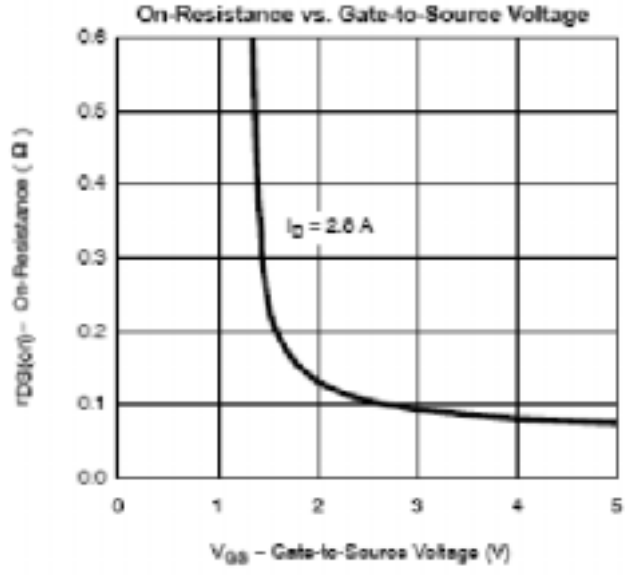

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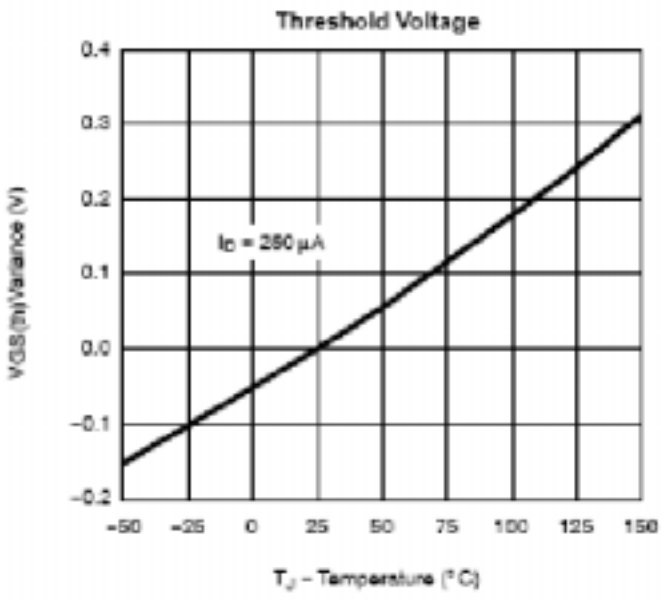

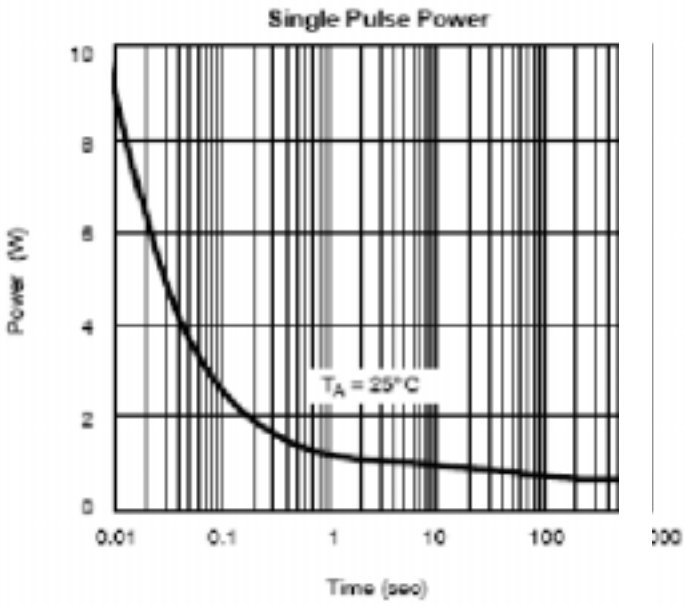

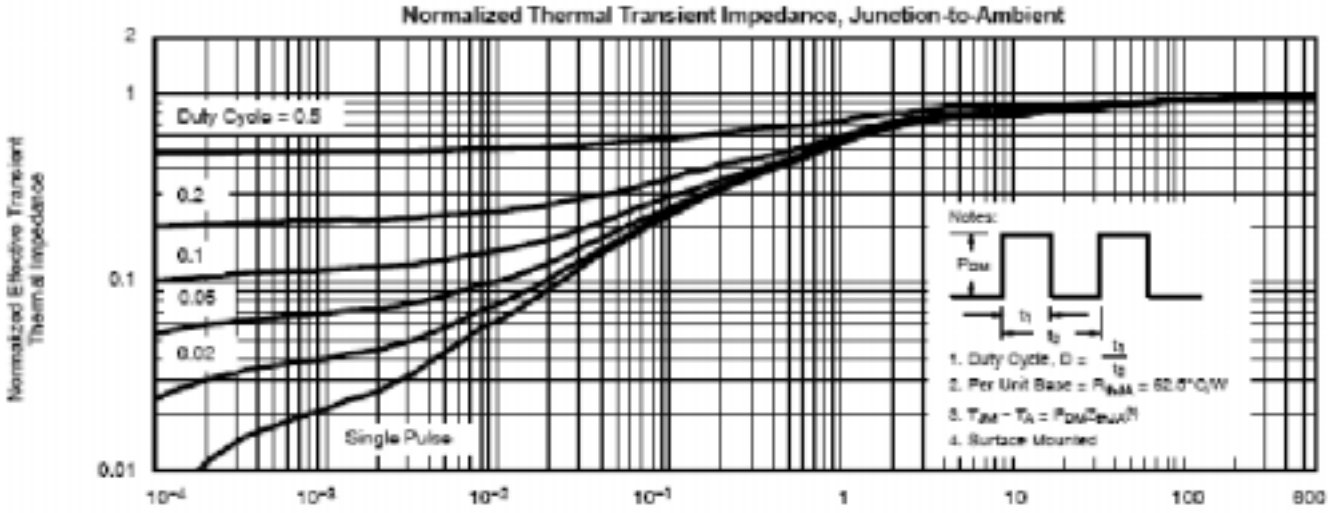

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