1 Mbit / 2 Mbit (x8) Many-Time Programmable Flash
SST27VF010 / SST27VF020

Preliminary Specifications

FEATURES:

- **Organized as 128K x8 / 256K x8**
- **2.7-3.6V Read Operation**
- **Superior Reliability**
  - Endurance: At least 1000 Cycles
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Current: 20 mA (typical)
  - Standby Current: 2 µA (typical)
- **Fast Read Access Time**
  - 70 ns (PLCC or TSOP)
  - 90 ns (PDIP)
- **Fast Byte-Program Operation**
  - Byte-Program Time: 15 µs (typical)
  - Chip Program Time:
    2 seconds (typical) for SST27VF010
    4 seconds (typical) for SST27VF020
- **Electrical Erase Using Programmer**
  - Does not require UV source
  - Chip-Erase Time: 100 ms (typical)
- **JEDEC Standard Byte-wide EPROM Pinouts**
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)
  - 32-pin PDIP

PRODUCT DESCRIPTION

The SST27VF010/020 are 128K x8 / 256K x8 CMOS, Many-Time Programmable (MTP) low cost flash, manufactured with SST's proprietary, high-performance SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. These MTP devices can be electrically erased and programmed at least 1000 times using an external programmer with a 12V power supply. They have to be erased prior to programming. These devices conform to JEDEC standard pinouts for byte-wide memories.

Featuring high performance Byte-Program, the SST27VF010/020 provide a Byte-Program time of 15 µs. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with an endurance of at least 1000 cycles. Data retention is rated at greater than 100 years.

The SST27VF010/020 are suited for applications that require infrequent writes and low power nonvolatile storage. These devices will improve flexibility, efficiency, and performance while matching the low cost in nonvolatile applications that currently use UV-EPROMs, OTPs, and mask ROMs.

To meet surface mount and conventional through hole requirements, the SST27VF010/020 are offered in 32-pin PDIP, 32-lead PLCC, and 32-lead TSOP packages. See Figures 1, 2, and 3 for pin assignments.

Device Operation

The SST27VF010/020 are a low cost flash solution that can be used to replace existing UV-EPROM, OTP, and mask ROM sockets. These devices are functionally (read and program) and pin compatible with industry standard EPROM products. In addition to EPROM functionality, these devices also support electrical Erase operation via an external programmer. They do not require a UV source to erase, and therefore the packages do not have a window.

Read

The Read operation of the SST27VF010/020 is controlled by CE# and OE#. Both CE# and OE# have to be low for the system to obtain data from the outputs. Once the address is stable, the address access time is equal to the delay from CE# to output (T_{CE}). Data is available at the output after a delay of T_{OE} from the falling edge of OE#, assuming that CE# pin has been low and the addresses have been stable for at least T_{CE}-T_{OE}. When the CE# pin is high, the chip is deselected and a typical standby current of 2 µA is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high.

Byte-Program Operation

The SST27VF010/020 are programmed by using an external programmer. The programming mode for SST27VF010/020 is activated by asserting 11.4-12.0V on V_{PP} pin, V_{DD} = 2.7-3.6V, V_{IL} on CE# pin, and V_{IH} on OE# pin. These devices are programmed byte-by-byte with the desired data at the desired address using a single pulse (PGM# pin low for SST27VF010/020) of 15 µs. Using the MTP programming algorithm, the Byte-Programming process continues byte-by-byte until the entire chip has been programmed.

Chip-Erase Operation

The only way to change a data from a "0" to "1" is by electrical erase that changes every bit in the device to "1". Unlike traditional EPROMs, which use UV light to do the Chip-Erase, the SST27VF010/020 uses an electrical Chip-Erase operation. This saves a significant amount of time (about 30 minutes for each Erase operation). The entire chip can be erased in a single pulse of 100 ms (PGM# pin for SST27VF010/020). In order to activate the Erase mode for SST27VF010/020, the 11.4-12.6V is applied to the A_9 pin, 11.4-12.0V is applied to the V_{PP} pin, V_{DD} = 2.7-3.6V, V_{IL} on CE# pin, and V_{IH} on OE# pin. All other address and data pins are "don't care". The falling edge of CE# (PGM# for SST27VF010/020) will start the Chip-Erase operation. Once the chip has been erased, all bytes must be verified for FFH. Refer to Figure 9 for the flowchart.

Product Identification Mode

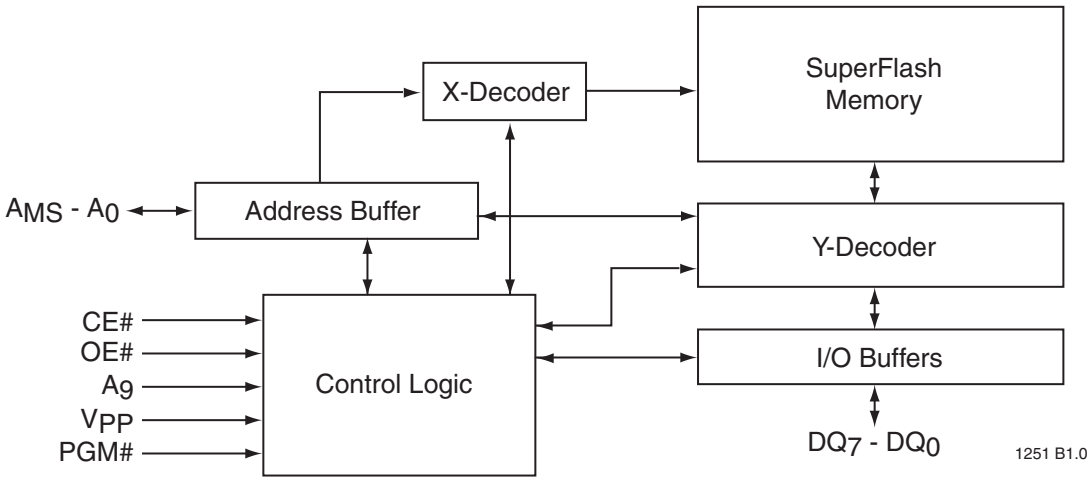
The Product Identification mode identifies the devices as the SST27VF010 or SST27VF020 and manufacturer as SST. This mode may be accessed by the hardware method. To activate this mode for SST27VF010/020, the programming equipment must force V_H (11.4-12.6V) on address A_9 with V_{PP} pin at V_{DD} (2.7-3.6V) or V_{SS}. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0. For details, see Table 3 for hardware operation.

TABLE 1: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST27VF010	0001H	A9H
SST27VF020	0001H	AAH

T1.0 1251

FUNCTIONAL BLOCK DIAGRAM OF THE SST27VF010/020



A_{MS} = A_{17} for SST27VF020, A_{16} for SST27VF010

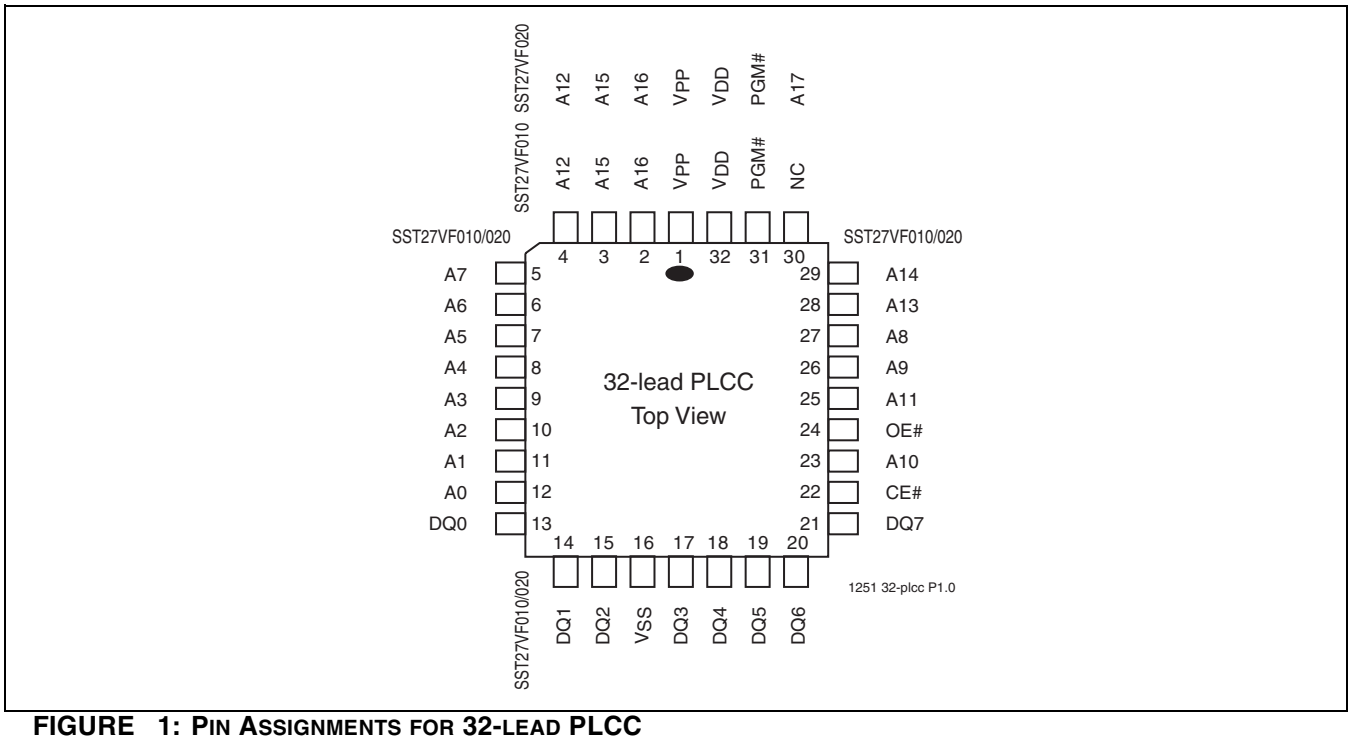


FIGURE 1: PIN ASSIGNMENTS FOR 32-LEAD PLCC

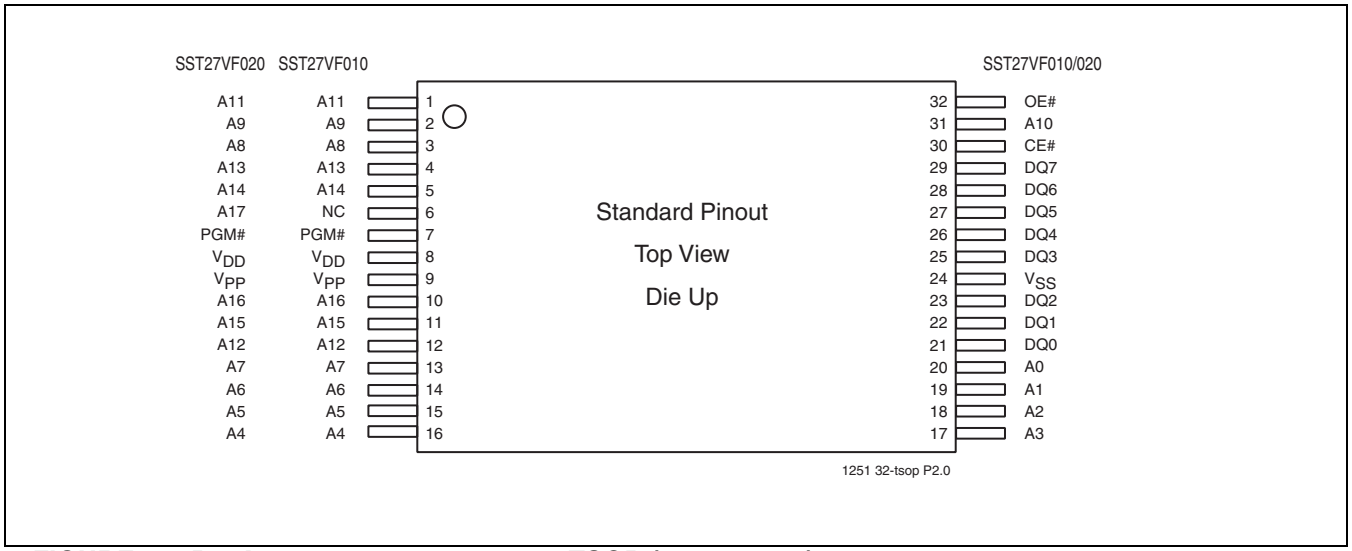


FIGURE 2: PIN ASSIGNMENTS FOR 32-LEAD TSOP (8MM X 14MM)

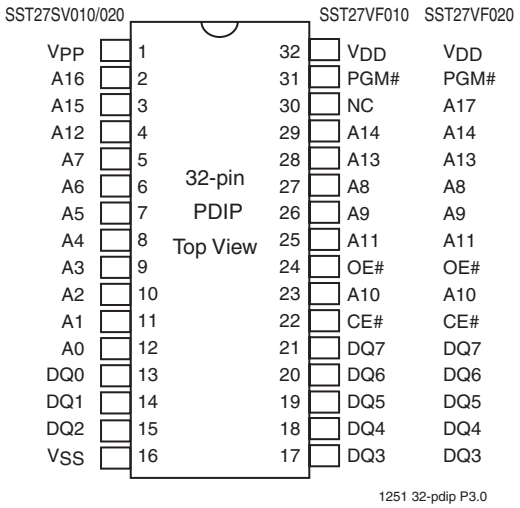


FIGURE 3: PIN ASSIGNMENTS FOR 32-PIN PDIP

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{MS}[1]-A_0	Address Inputs	To provide memory addresses
DQ_7-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Program cycles The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low
OE#	Output Enable	To gate the data output buffers during Read operation
V_{PP}	Power Supply for Program or Erase	High voltage pin during Chip-Erase and programming operation 11.4-12.0V
V_{DD}	Power Supply	To provide 3.0V supply (2.7-3.6V)
V_{SS}	Ground	
NC	No Connection	Unconnected pins.

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1. A_{MS} = Most significant address
   A_{MS} = A_{16} for SST27VF010 and A_{17} for SST27VF020

TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	PGM#	A_9	V_{PP}	DQ	Address
Read	V_{IL}	V_{IL}	X[1]	A_{IN}	V_{DD} or V_{SS}	D_{OUT}	A_{IN}
Output Disable	V_{IL}	V_{IH}	X	X	V_{DD} or V_{SS}	High Z	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	A_{IN}	V_{PPH}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	X	V_{DD} or V_{SS}	High Z	X
Chip-Erase	V_{IL}	V_{IH}	V_{IL}	V_H	V_{PPH}	High Z	X
Program/Erase Inhibit	V_{IH}	X	X	X	V_{PPH}	High Z	X
Product Identification	V_{IL}	V_{IL}	X	V_H	V_{DD} or V_{SS}	Manufacturer's ID (BFH) Device ID[2]	A_{MS}[3] - A_1=V_{IL}, A_0=V_{IL} A_{MS}[3] - A_1=V_{IL}, A_0=V_{IH}

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1. X can be V_{IL} or V_{IH}, but no other value.
2. Device ID = A9H for SST27VF010 and AAH for SST27VF020
3. A_{MS} = Most significant address
   A_{MS} = A_{16} for SST27VF010 and A_{17} for SST27VF020

Note: V_{PPH} = 11.4-12.0V, V_H = 11.4-12.6V

Preliminary Specifications

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Voltage on A_9 and V_{PP} Pin to Ground Potential . . . . . -0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hold Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}	V_{PP}
Commercial	0°C to +70°C	2.7-3.6V	11.4-12.0V

AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 5 ns
Output Load . . . . . C_L = 30 pF
See Figures 7 and 8

TABLE 4: READ MODE DC OPERATING CHARACTERISTICS V_{DD} = 2.7-3.6V, $V_{PP}=V_{DD}$ OR V_{SS} (Ta = 0°C to +70°C (Commercial))

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	V_{DD} Read Current				Address input=V_{ILT}/V_{IHT} at f=1/T_{RC} Min $V_{DD}=V_{DD}$ Max
			15	mA	CE#=OE#=V_{IL}, all I/Os open
I_{PPR}	V_{PP} Read Current				Address input=V_{ILT}/V_{IHT} at f=1/T_{RC} Min $V_{DD}=V_{DD}$ Max, $V_{PP}=V_{DD}$
			100	µA	CE#=OE#=V_{IL}, all I/Os open
I_{SB}	Standby V_{DD} Current		15	µA	CE#=V_{DD}-0.3, $V_{DD}=V_{DD}$ Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		10	µA	V_{OUT}=GND to V_{DD}, $V_{DD}=V_{DD}$ Max
V_{IL}	Input Low Voltage		0.8	V	$V_{DD}=V_{DD}$ Min
V_{IH}	Input High Voltage	0.7V_{DD}		V	$V_{DD}=V_{DD}$ Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	$V_{DD}=V_{DD}$ Max
V_{OL}	Output Low Voltage		0.2	V	I_{OL}=100 µA, $V_{DD}=V_{DD}$ Min
V_{OH}	Output High Voltage	V_{DD}-0.3		V	I_{OH}=-100 µA, $V_{DD}=V_{DD}$ Min
I_H	Supervoltage Current for A_9		200	µA	CE#=OE#=V_{IL}, $A_9=V_H$ Max

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TABLE 5: PROGRAM/ERASE DC OPERATING CHARACTERISTICS V_{DD} = 2.7-3.6V, V_{PP} = V_{PPH} (Ta=25°C±5°C)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	V_{DD} Erase or Program Current		20	mA	CE#=PGM#=V_{IL}, OE#=V_{IH}, V_{PP}=11.4-12.0V, $V_{DD}=V_{DD}$ Max
I_{PP}	V_{PP} Erase or Program Current		3	mA	CE#=PGM#=V_{IL}, OE#=V_{IH}, V_{PP}=11.4-12.0V, $V_{DD}=V_{DD}$ Max
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{DD}, $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{DD}, $V_{DD}=V_{DD}$ Max
V_H	Supervoltage for A_9	11.4	12.6	V	CE#=OE#=V_{IL},
I_H	Supervoltage Current for A_9		200	µA	CE#=OE#=V_{IL}, $A_9=V_H$ Max
V_{PPH}	High Voltage for V_{PP} Pin	11.4	12.0	V	

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TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T6.0 1251

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

T7.0 1251

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	1000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 78

T8.0 1251

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 9: READ CYCLE TIMING PARAMETERS V_{DD} = 2.7-3.6V (Ta = 0°C to +70°C (Commercial))

Symbol	Parameter	SST27VF010-70 SST27VF020-70		SST27VF010-90 SST27VF020-90		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	70		90		ns
T_{CE}	Chip Enable Access Time		70		90	ns
T_{AA}	Address Access Time		70		90	ns
T_{OE}	Output Enable Access Time		35		45	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		25		30	ns
T_{OHZ}[1]	OE# High to High-Z Output		25		30	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

T9.0 1251

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS (Ta = 25°C±5°C)

Symbol	Parameter	Min	Max	Units
T_{CES}	CE# Setup Time	1		µs
T_{CEH}	CE# Hold Time	1		µs
T_{AS}	Address Setup Time	1		µs
T_{AH}	Address Hold Time	1		µs
T_{PRT}	V_{PP} Pulse Rise Time	50		ns
T_{VPS}	V_{PP} Setup Time	1		µs
T_{VPH}	V_{PP} Hold Time	1		µs
T_{PW}	PGM# Program Pulse Width	15	25	µs
T_{EW}	PGM# Erase Pulse Width	100	200	ms
T_{DS}	Data Setup Time	1		µs
T_{DH}	Data Hold Time	1		µs
T_{VR}	A_9 Recovery Time for Erase	1		µs
T_{ART}	A_9 Rise Time to 12V during Erase	50		ns
T_{A9S}	A_9 Setup Time during Erase	1		µs
T_{A9H}	A_9 Hold Time during Erase	1		µs

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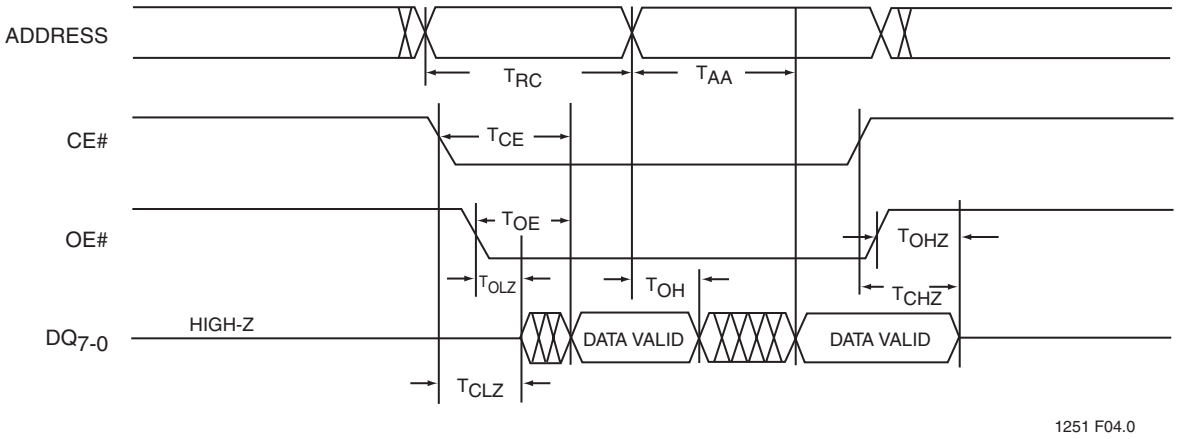


FIGURE 4: READ CYCLE TIMING DIAGRAM

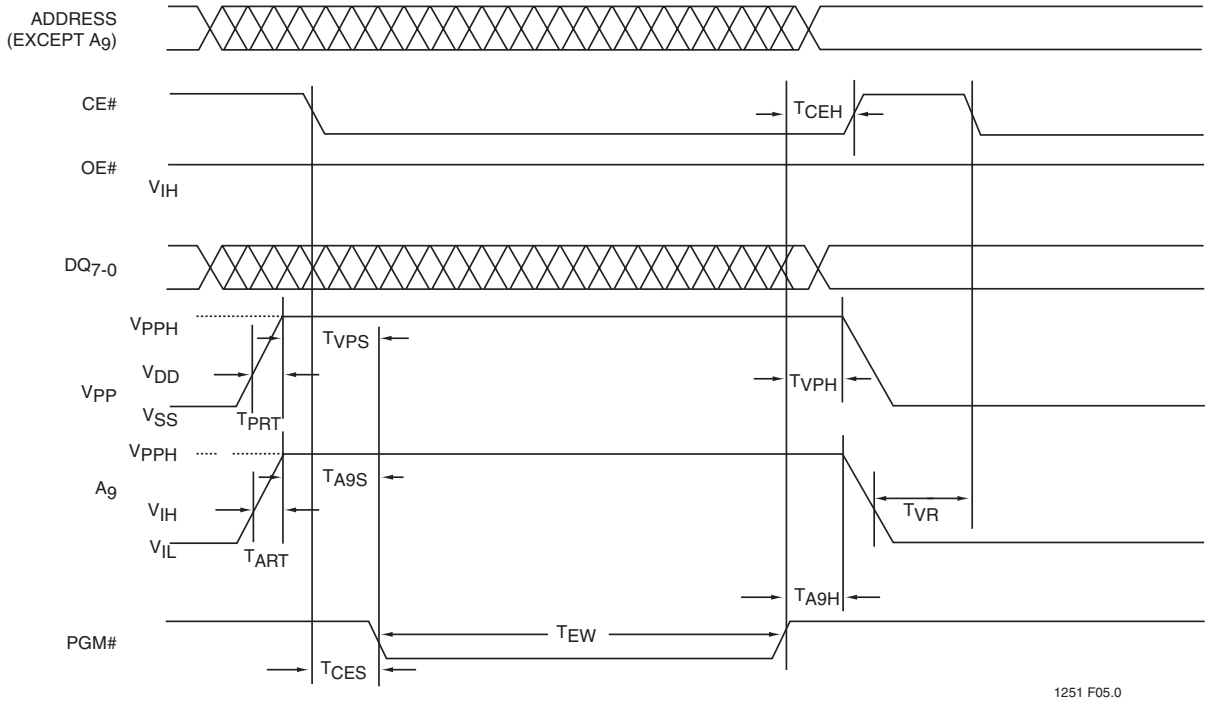


FIGURE 5: CHIP-ERASE TIMING DIAGRAM

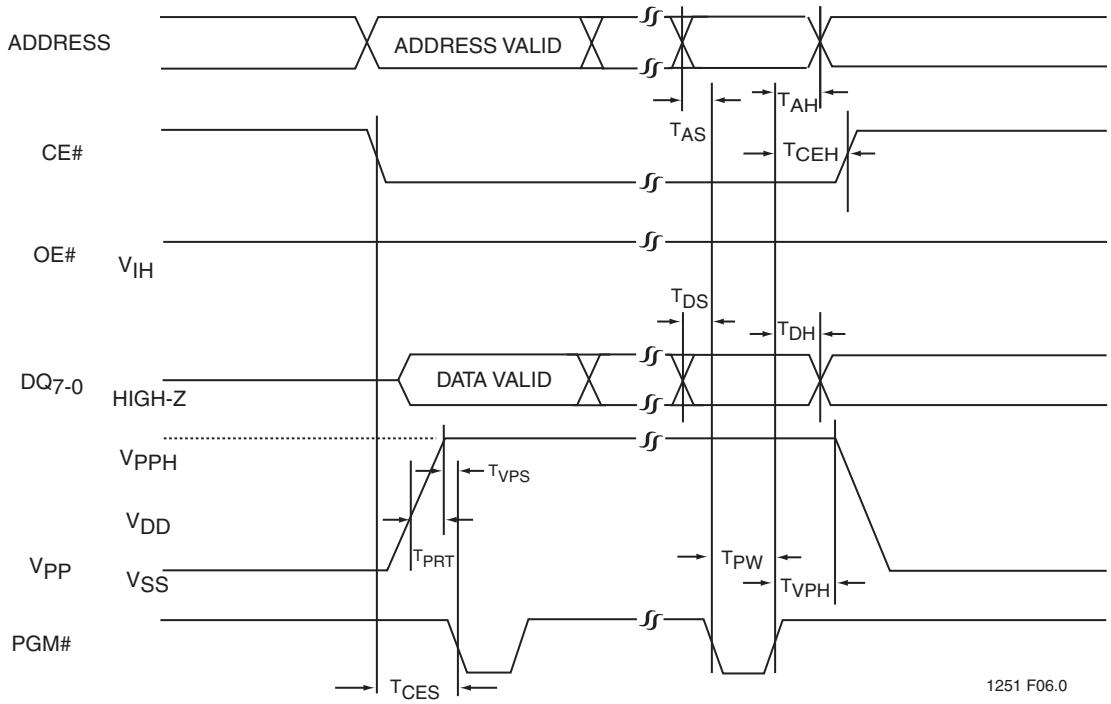
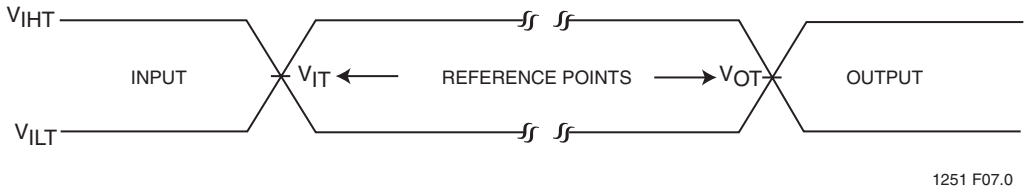


FIGURE 6: BYTE-PROGRAM TIMING DIAGRAM



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT}Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 7: AC INPUT/OUTPUT REFERENCE WAVEFORMS

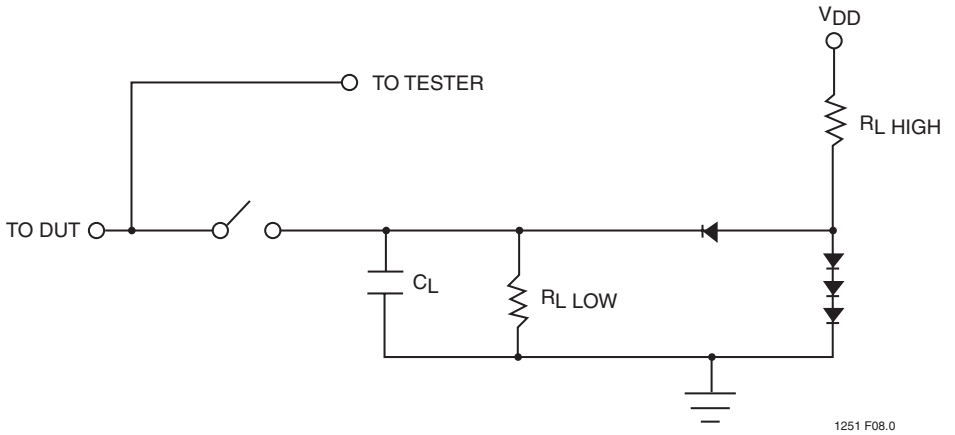


FIGURE 8: A TEST LOAD EXAMPLE

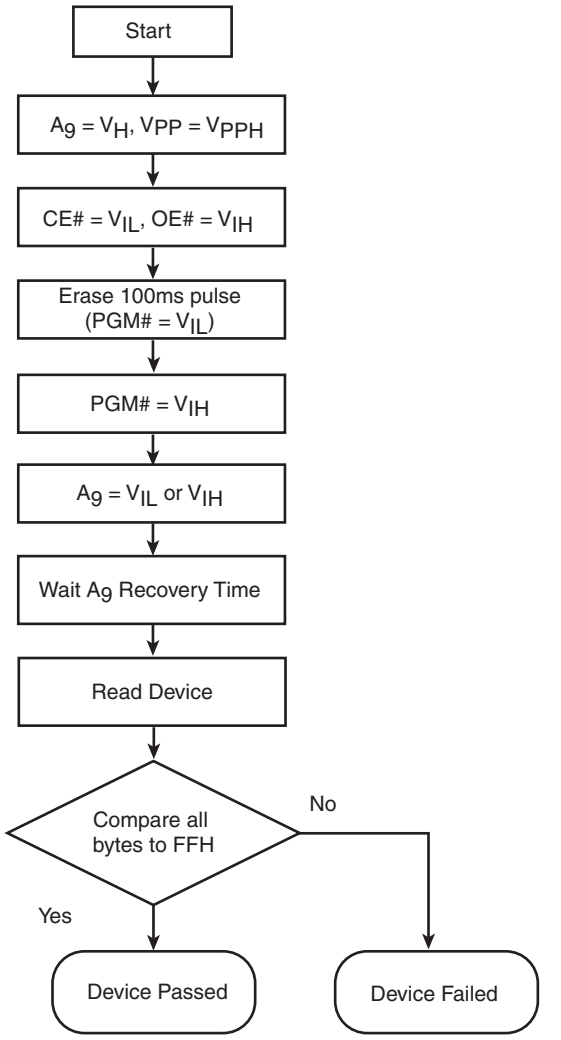
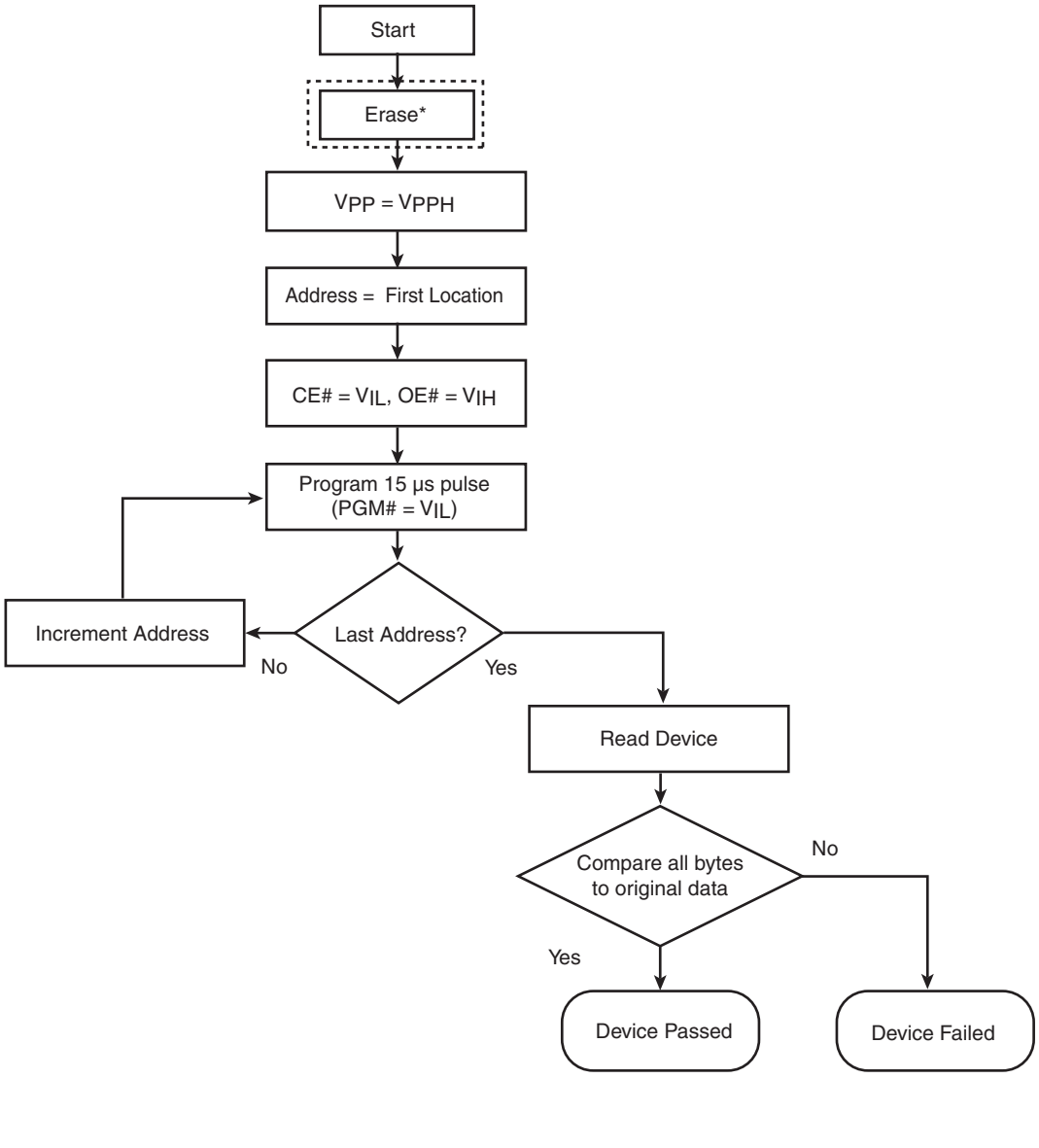


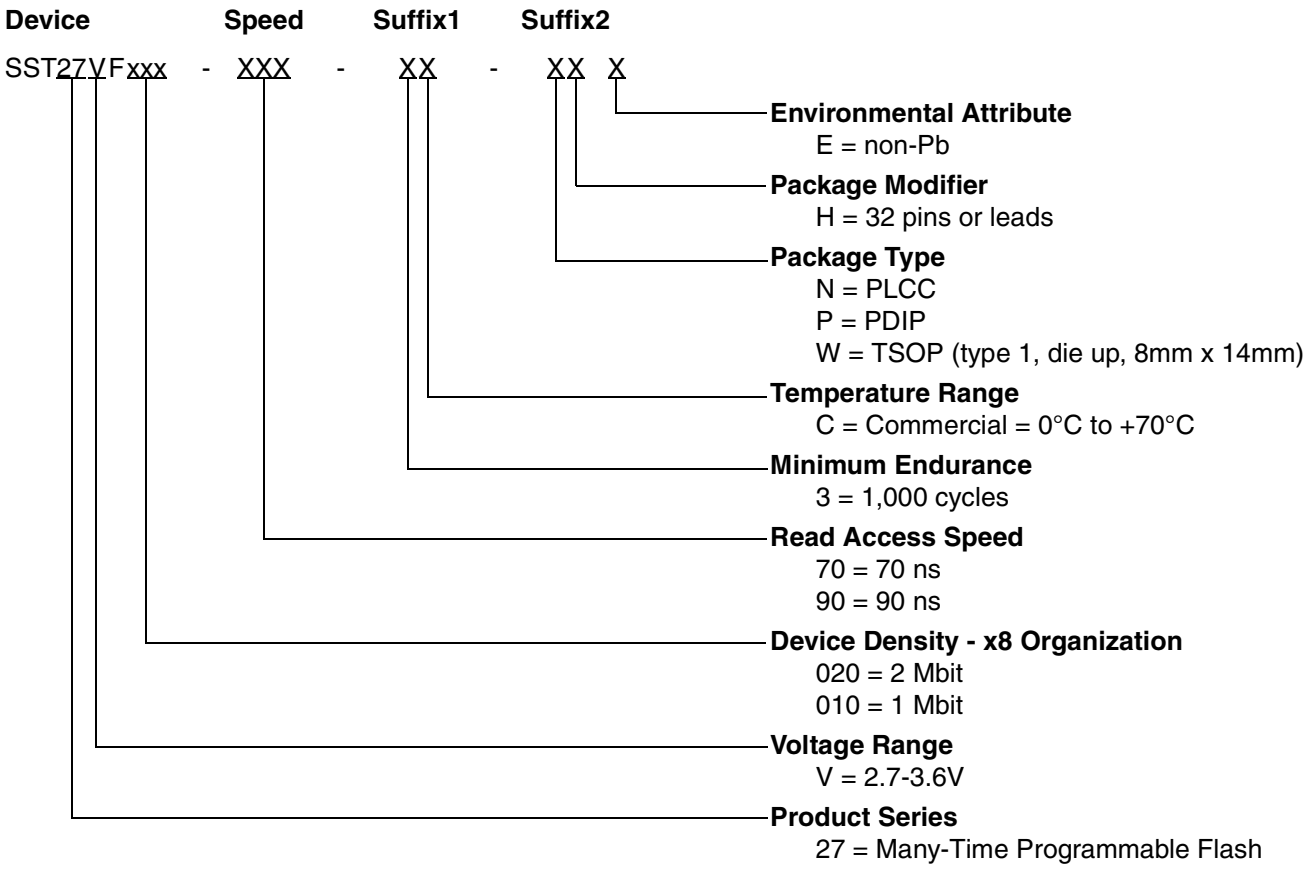
FIGURE 9: CHIP-ERASE ALGORITHM



* See Figure 9

FIGURE 10: BYTE-PROGRAM ALGORITHM

PRODUCT ORDERING INFORMATION



Valid combinations for SST27VF010

SST27VF010-70-3C-NH SST27VF010-70-3C-WH
SST27VF010-70-3C-NHE SST27VF010-70-3C-WHE
SST27VF010-90-3C-PH
SST27VF010-90-3C-PHE

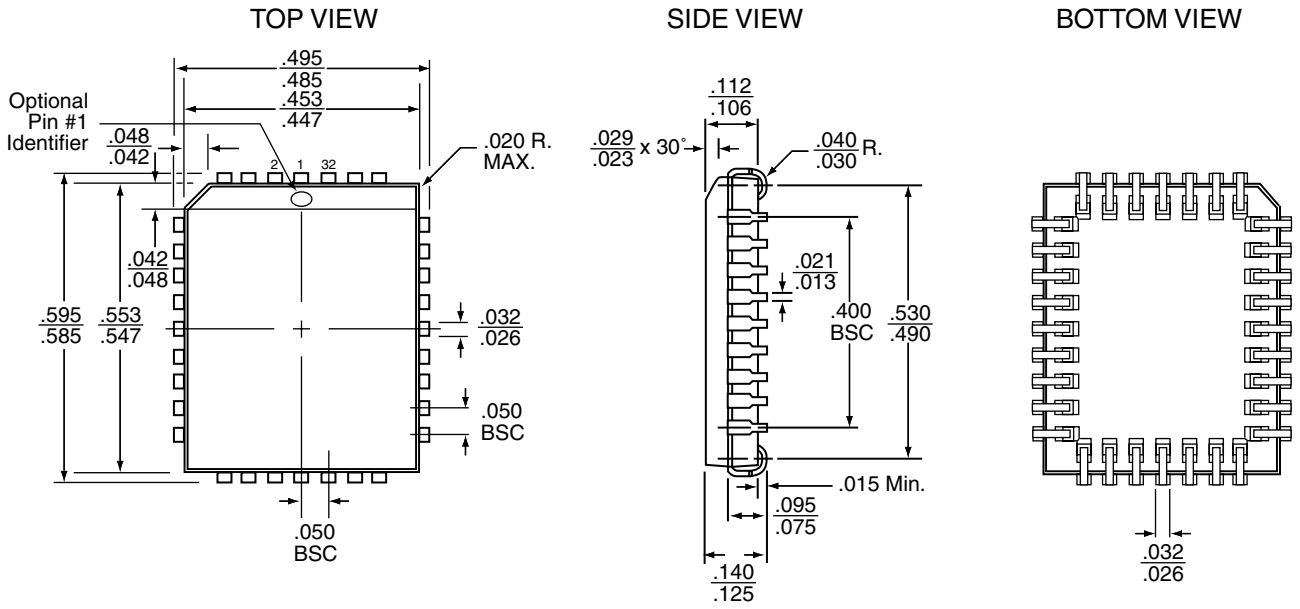
Valid combinations for SST27VF020

SST27VF020-70-3C-NH SST27VF020-70-3C-WH
SST27VF020-70-3C-NHE SST27VF020-70-3C-WHE
SST27VF020-90-3C-PH
SST27VF020-90-3C-PHE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Preliminary Specifications

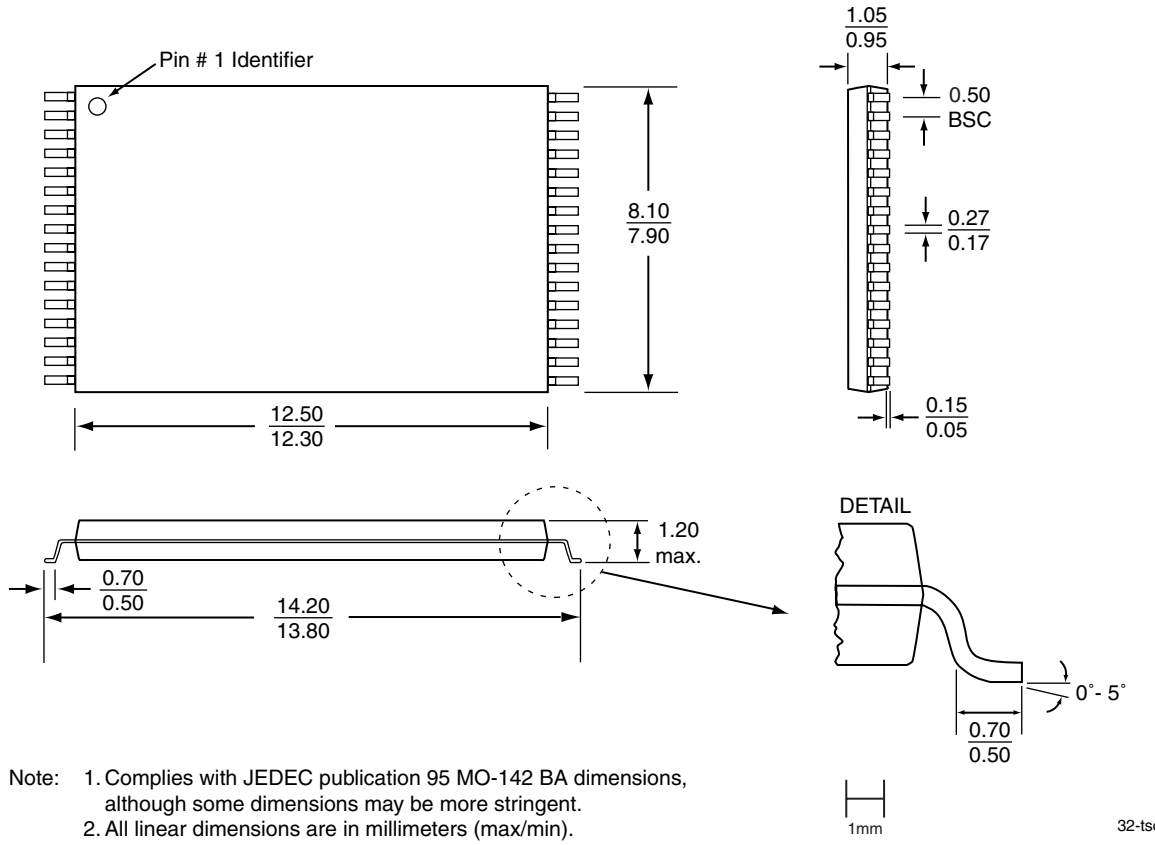
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

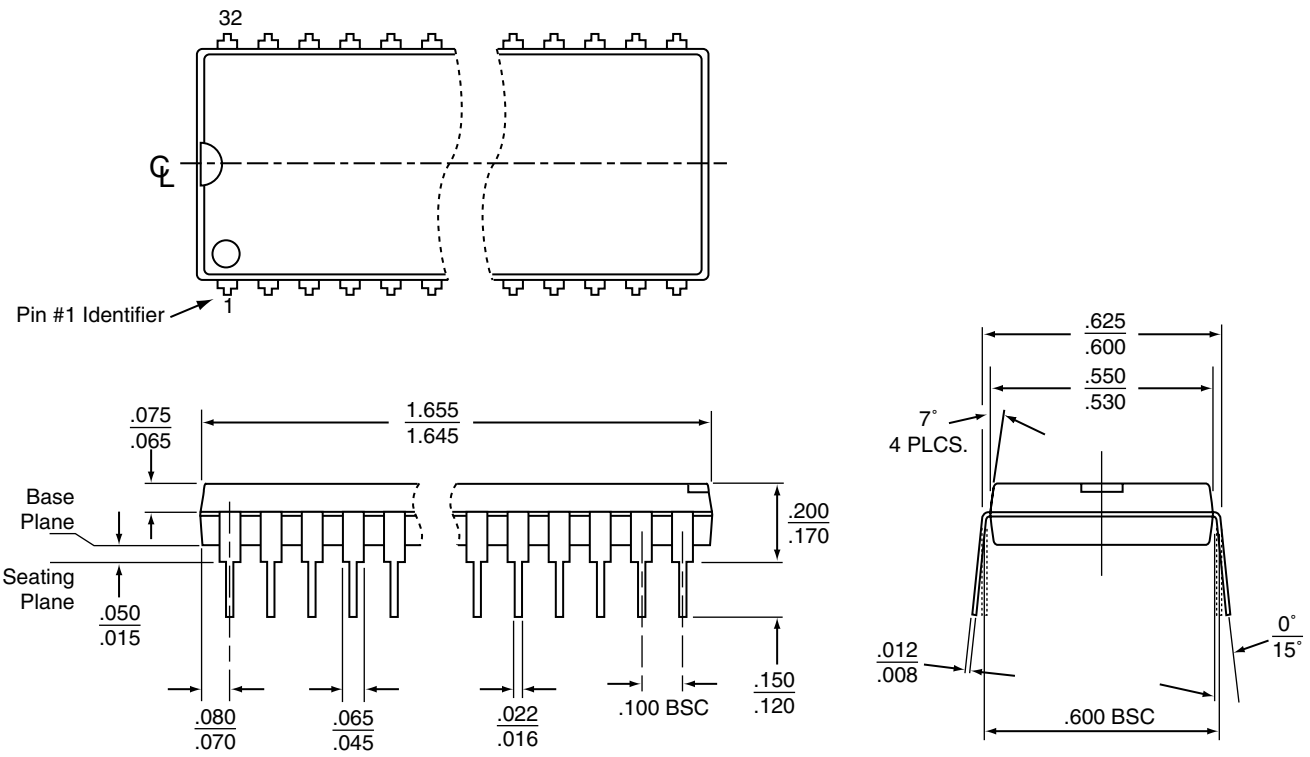
32-plcc-NH-3

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH



Note: 1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

32-pdip-PH-3

32-PIN PLASTIC DUAL IN-LINE PINS (PDIP)
SST PACKAGE CODE: PH

Revision History

Number	Description	Date
00	• Initial Release	Dec 2003