Synchronous Step Down Controller

DESCRIPTION

SiP12201 is a synchronous step down controller designed for use in dc-dc converter circuits requiring output currents as high as 10 amperes. SiP12201 is designed to require a minimum number of external components, simplifying design and layout. It accepts input voltages from 4.2 V to 26.0 V, providing an adjustable output with voltage ranging from 0.6 V to 5 V.

SiP12201 includes an combination Compensation/ Shutdown pin. Protection features include undervoltage lockout, output current limit, and thermal shutdown.

SiP12201 is available in a lead (Pb)-free MLP33-10 package and is specified to operate over the range of - 40 °C to 85 °C.

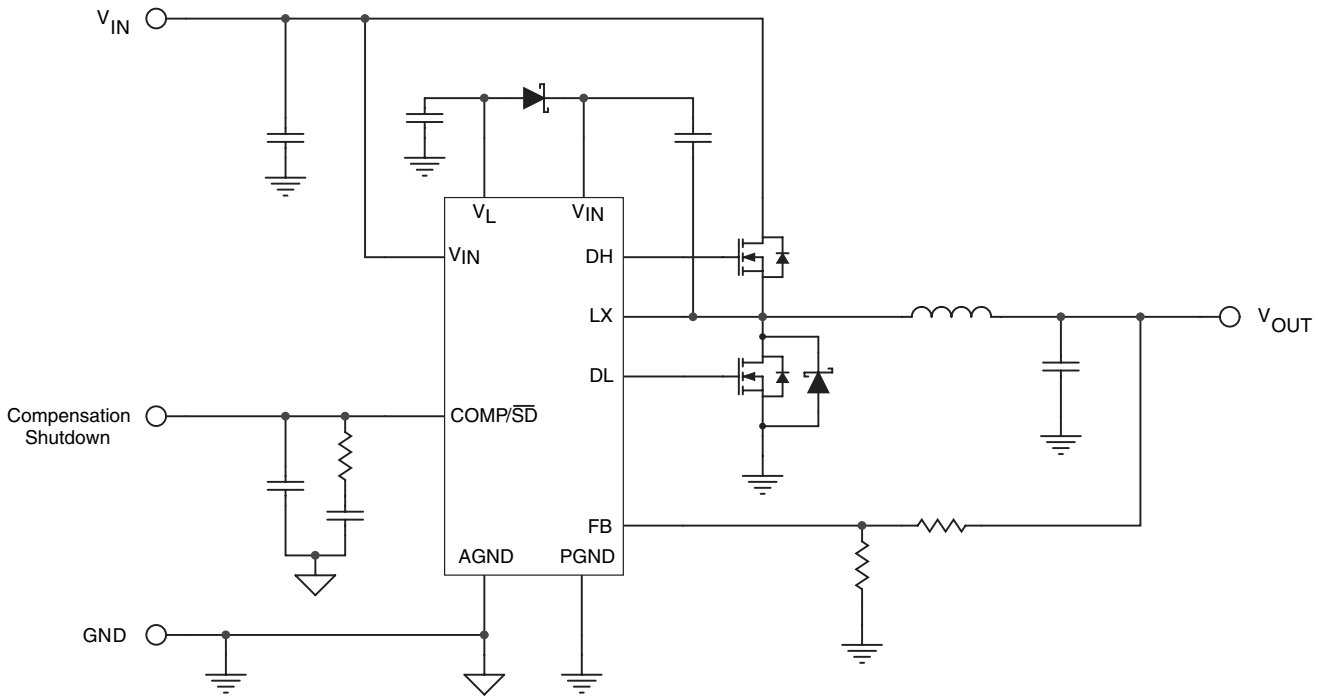
FEATURES

- 4.2 V to 26.0 V Input Voltage Range
- Adjustable Output Voltage - 0.6 to 5.5 V
- For Converter loads up to 10 A
- High efficiency - 93%
- Uses N-channel MOSFETs
- 500 kHz operation
- Internal Soft Start
- Shutdown pin
- Output Current Limit
- Minimum External Components
- MLP33-10 Package

APPLICATIONS

- Distributed Power
- Desktop & Notebook Computers
- Battery Operated Equipment
- Point of Load Regulation
- DSP Cores
- Automotive Entertainment

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit
V_{IN}, LX to GND	29	V
BST to LX	6	
FB, Comp/$\overline{SD}$ to GND	- 0.3 to 6	
Power Dissipation[a, b]	560	mW
Maximum Junction Temperature	125	°C
Storage Temperature	- 55 to + 150	

Notes
a. Device mounted with all leads soldered or welded to PC board
b. Derate 14 mW/°C above + 85 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
Input Voltage Range	4.2 to 26.0	V
Output Voltage Adjustment Range	0.6 to 5.5	
Operating Temperature Range	- 40 to + 85	°C

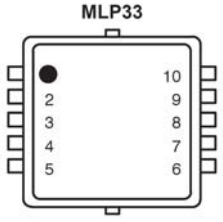
SPECIFICATIONS[a]

Parameter	Symbol	Test Condition Unless Specified V_{IN} = 5.5 to 26 V	Limits -40 to 85°C			Unit
			Min[a]	Typ[b]	Max[a]	
Controller						
Input Voltage	V_{IN}		4.2		26.0	V
Quiescent Current		Non switching		850	1250	µA
Internal Supply Voltage	V_L		4.8		5.5	V
Oscillator Frequency	f_{OSC}		400	500	600	kHz
Oscillator Ramp Amplitude	ΔV_{OSC}			1		V
Max Duty Cycle	DC		87	93		%
Feedback Voltage	V_{FB}	T_A = 25°C	0.591	0.600	0.609	V
			0.585		0.615	
FB input Bias Current	I_{FB}				100	nA
Transconductance	GM			2		mA/V
Soft Start				4		ms
Inputs and Outputs						
$\overline{SD}$ Input Voltage	V_{IL}				0.15	V
Shutdown Current	I_{SD}			120	225	µA
MOSFET Drivers						
Break-before-make time	t_{BBM}			10		ns
Highside Driver						
Output Voltage	V_{DH}		4.5			V
On resistance	$R_{DS_{HH}}$	$V_{IN} = V_{BST} = V_{LX}$ = 4.5 V		8.7	13	Ω
	$R_{DS_{HL}}$	$V_{IN} = V_{BST} = V_{LX}$ = 4.5 V		2.3	3.6	Ω
Rise time	t_{rH}	$V_{IN} = V_L = V_{BST}$ = 5 V, C_L = 2.7 nF		51		ns
Fall time	t_{fH}	$V_{IN} = V_L = V_{BST}$ = 5 V, C_L = 2.7 nF		15		

SPECIFICATIONS[a]						
Parameter	Symbol	Test Condition Unless Specified V_{IN} = 5.5 to 26 V	Limits -40 to 85°C			Unit
			Min[a]	Typ[b]	Max[a]	
Lowside Driver						
Output Voltage	V_{DL}		4.5			V
On resistance	$R_{DS_{LH}}$	V_{IN} = V_L = 4.5 V		2.5	3.9	Ω
	$R_{DS_{LL}}$	V_{IN} = V_L = 4.5 V		0.85	1.4	Ω
Rise time	t_{rL}	V_{IN} = V_L = 5 V, C_L= 2.7 nF		13.4		ns
Fall time	t_{fL}	V_{IN} = V_L = 5 V, C_L= 2.7 nF		5.8		
Protection						
Under voltage lockout	V_{UVLO}	Rising		3.6	3.9	V
UVLO-Hysteresis				0.180		
UVLO-High Side		Rising		2.0	2.3	
UVLO-High Side Hysteresis				0.15		
Thermal Shutdown Temperature		Rising		165		°C
Thermal Hysteresis				20		°C
Over Current Limit						
MOSFET on Voltage Sense Threshold	V_{DL}		-240	-170	-110	mV

NOTES:
a) The algebriac convention whereby the most negative value is a minimum and the most positive a maximum.
b) Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

PIN CONFIGURATION



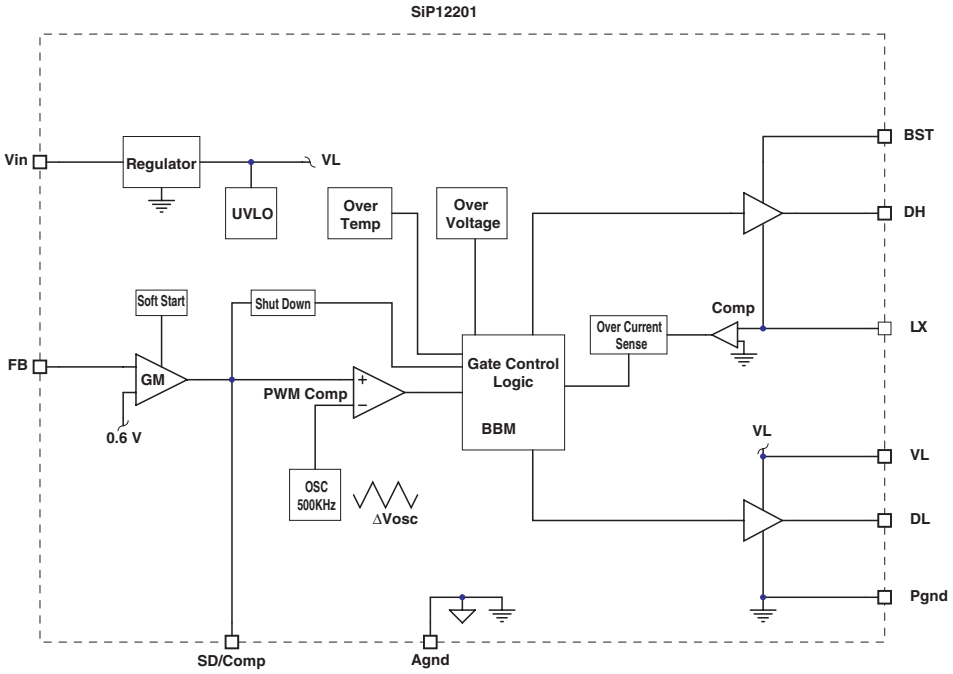
PIN DESCRIPTION

Pin Number	Name	Function
1	COMP/$\overline{SD}$	Combination Compensation and Shut down pin
2	FB	Feedback input
3	AGND	Analog Ground
4	V_{IN}	Input voltage for the power MOSFETs and their gate drive
5	VL	Internal Supply Voltage
6	DL	Lowside gate drive
7	PGND	Power Ground
8	BST	Connection for the bootstrap capacitor
9	DH	Highside gate drive
10	LX	Connection for the inductor node

ORDERING INFORMATION

Part Number	Temperature Range	Package
SiP12201DM-T1-E3	-40 to 85 °C	MLP33-10
Eva Kit	**Temperature Range**	**Board**
SiP12201DB	-40 to 85 °C	Surface Mount

FUNCTIONAL BLOCK DIAGRAM



DETAILED OPERATIONAL DESCRIPTION

Enable/ON State:

The COMP/$\overline{SD}$ pin has 10 µA pull up current to ensure auto startup as soon as the pin is released by the external pull down MOS. When the internal reference is ready, there will be a clamp current applied at COMP/$\overline{SD}$; this is to ensure the COMP/$\overline{SD}$ pin will not go below 600 mV inadvertently due to the amplifier excursion or noise. The COMP/$\overline{SD}$ has to go above 600 mV to enable the chip fully.

Disable/Shutdown/Off State

To disable the chip, the COMP/$\overline{SD}$ pin has to pulled below 150 mV typically and the external pull down MOSFET has to be able to sink at least 250 µA. Once the pin reaches a voltage below the 150 mV level, the chip will go into shutdown mode with only essential curcuitry alive and the current bias of the chip will be cut down to 120 µA level typically. Both High Side and Low Side Gates are off.

UVLO:

The chip enters into Under Voltage Lockout when VL is below 3.4 V (typical). Both High Side Gate and Low Side Gate will be turned off. The chip will go out of UVLO mode when VL is above 3.6 V (typical).

Soft Start:

Once the chip is out of shutdown and UVLO mode, the soft start is initiated. The soft start is accomplished done by ramping up the internal reference. During soft start mode the chip can not enter into fault mode. If there is an over current condition (current limit condition), the High Side Gate will be turned off and the Low Side will be turned on. Once the soft start timing elapses, the chip enters into a normal state of operation.

Output Over Voltage State:

When the Output voltage goes above 1.083 times nominal Output Voltage, the High Side Gate will be turned off and the Low Side Gate will be on. The condition will persist until the Output voltage drops below the trigger voltage minus a hysteresis.

Output Over Current State:

The SiP12201 will enter a cycle by cycle over current condition when the Low Side MOSFET is turned on, the LX voltage falls below -170 mV with respect to Power Ground. As long as the LX voltage remains below -170 mV the Low Side MOSFET is still turned on, the High Side MOSFET is off. If this condition remains for seven consecutive cycles the IC will go into a fault state. If the over current condition is removed before seven consecutive cycles the IC will revert to normal mode.

Fault State:

The IC can only enter into Fault mode after the soft start mode has ended and seven consecutive over current condition cycles has occurred. Once it enters the Fault state, with the High Side MOSFET turned off and the Low Side MOSFET turned on, any occurring over current condition will be ignored. The Fault State will last for seven soft start cycles. After which the IC will enter Soft Start mode. If the over current condition is removed the IC will operate normally, otherwise the over current sequence is repeated. This fault scheme minimizes thermal stress on the external power MOSFET switches.

Over Temperature:

When the temperature of the chip goes above 165 °C, the chip enters into over temperature shutdown. The High Side gate will be off and the Low Side gate will be on. Only system monitor circuitry will be active. Once the temperature of the chip drops below 145 °C, the chip enters into the normal operation mode.

Duty-Factor Limitations for Low V_{OUT} / V_{IN} Ratios

The SiP12201 output voltage is adjustable down to 0.6 V. However, the minimum duty factor may limit the ability to supply low-voltage outputs from high voltage inputs. With high-input voltages, the required duty factor is approximately:

$$\frac{\left(V_{OUT} + R_{DS(ON)} \times I_{LOAD}\right)}{V_{IN}}$$

where $R_{DS(ON)}$ x I_{LOAD} is the voltage drop across the synchronous rectifier. The SiP12201 minimum duty factor is 10%, so the maximum input voltage ($V_{IN(MAX)}$) that can supply a given output voltage is:

$$V_{IN(MAX)} \leq 10\ (V_{OUT} + R_{DS(ON)} \times I_{LOAD})$$

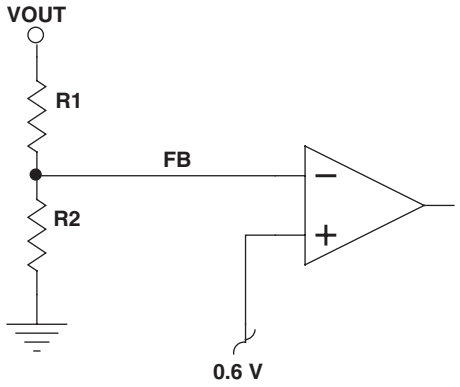
If the circuit cannot attain the required duty factor dictated by the input and output voltages, the output voltage still remains in regulation. However, there may be intermittent or continuous half-frequency operations as the controller attempts to lower the average duty factor by deleting pulses. This can increase output voltage ripple and inductor current ripple, which increases noise and reduces efficiency. Furthermore, circuit stability is not guaranteed.

Setting the Output Voltage:

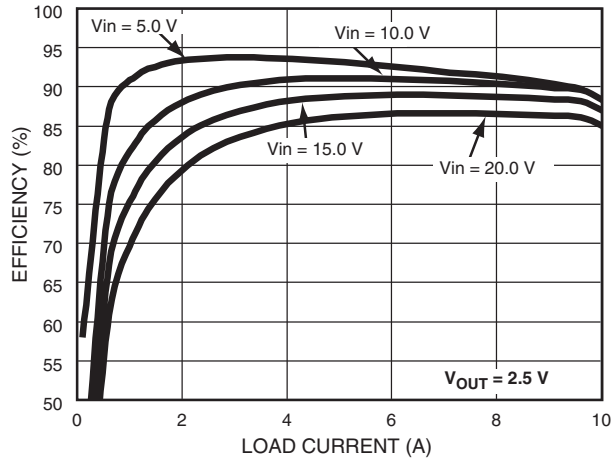
An output voltage between 0.6 V and 5.5 V (if V_{IN} is between 4.2 V and 6.0 V then the maximum V_{OUT} is 0.9* V_{IN}) and can be configured by connecting FB pin to a resistive divider between the output and GND. Select resistor R2 in the 1 kΩ to 10 kΩ range. R1 is then given by:

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

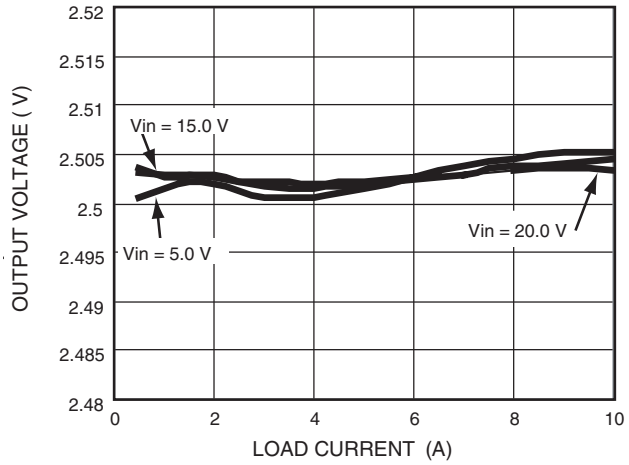
where V_{FB} = 0.6 V.



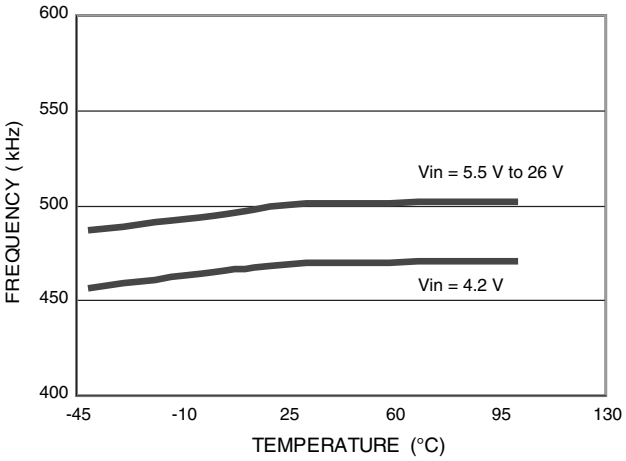
TYPICAL CHARACTERISTICS



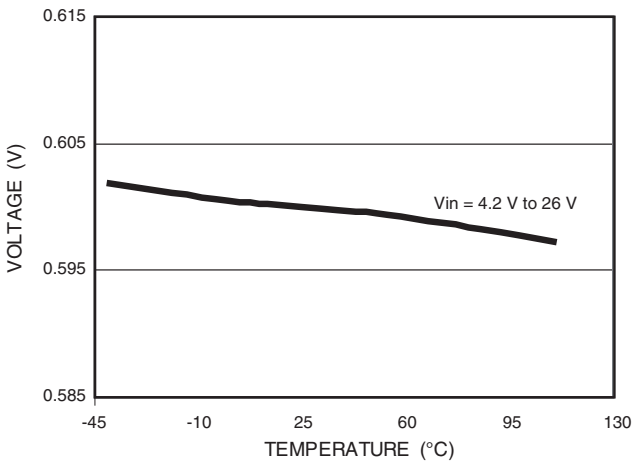
EFFICIENCY Vs. LOAD CURRENT



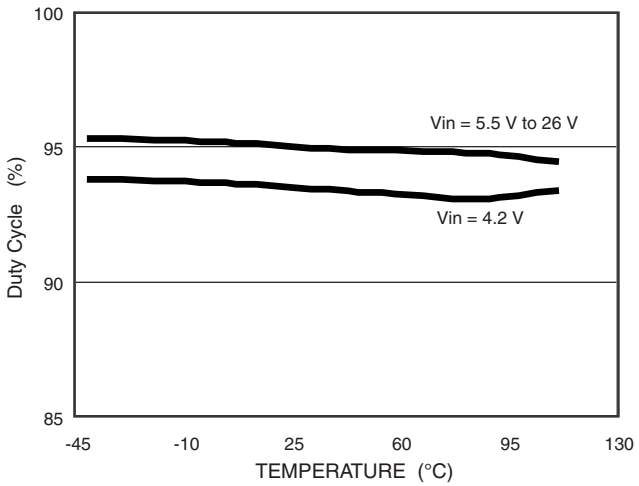
OUTPUT VOLTAGE Vs. LOAD CURRENT



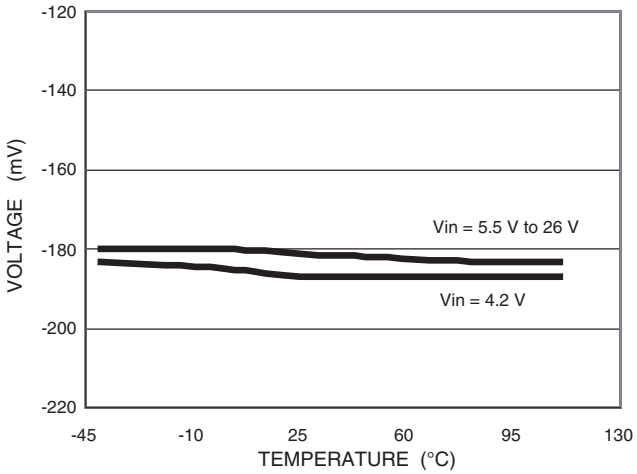
OSCILLATOR FREQUENCY Vs TEMPERATURE



FEEDBACK THRESHOLD Vs TEMPERATURE

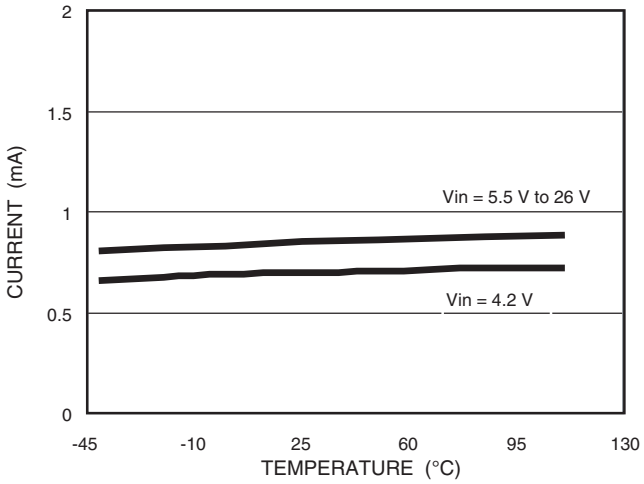


MAX DUTY CYCLE Vs TEMPERATURE

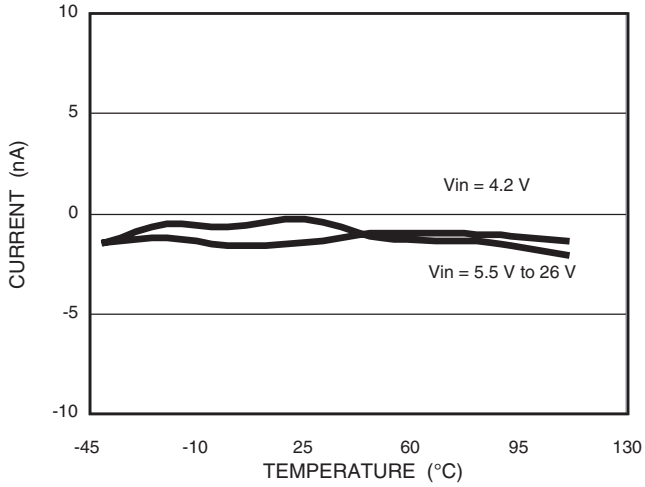


CURRENT SENSE VOLTAGE Vs TEMPERATURE

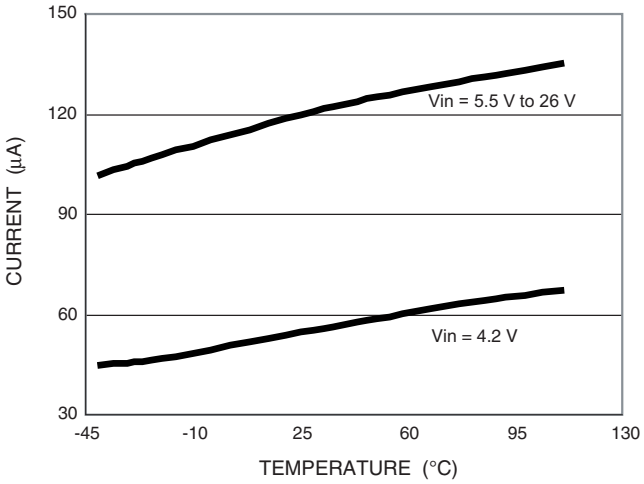
TYPICAL CHARACTERISTICS



QUIESCENT CURRENT Vs TEMPERATURE

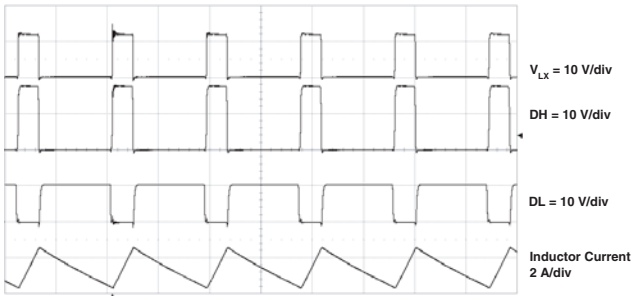


FB INPUT BIAS CURRENT Vs TEMPERATURE

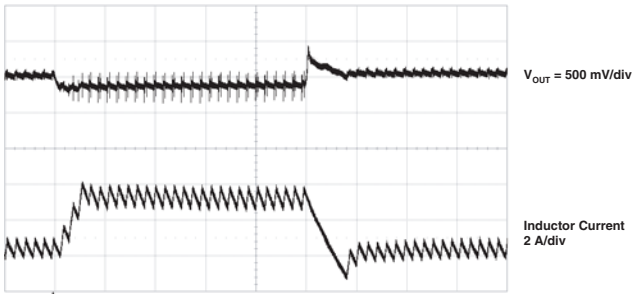


SHUTDOWN CURRENT Vs TEMPERATURE

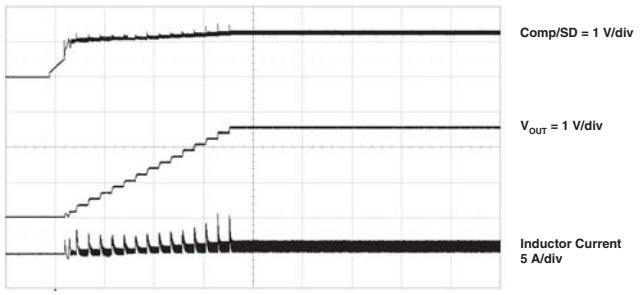
TYPICAL WAVEFORMS



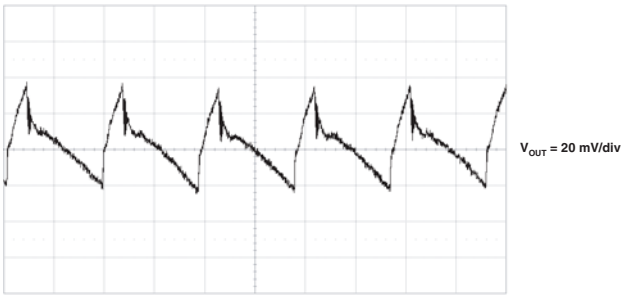
1 µs/div
V_{IN} = 12 V, V_{OUT} = 2.5 V, Load Current = 5 A, L = 1.5 µH,
C_{OUT} = 220 uF X 2
Typical Switching Waveform



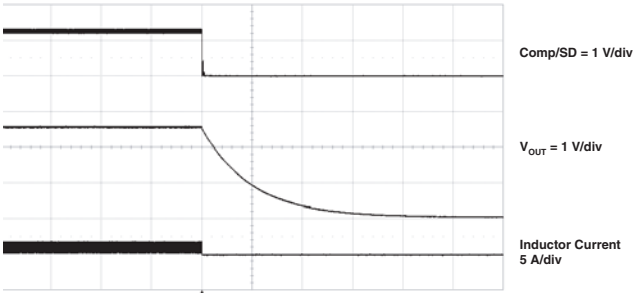
10 µs/div
V_{IN} = 12 V, V_{OUT} = 2.5 V, Load Current = 1 A to 8 A Step,
L = 1.5 µH, C_{OUT} = 220 uF X 2
Load Transient Response



1 ms/div
V_{IN} = 12 V, V_{OUT} = 2.5 V, Load Current = 1 A,
Output Filter Cap = 220 uF X 2
Soft Start



1 µs/div
V_{IN} = 12 V, V_{OUT} = 2.5 V, Load Current = 1 A,
L = 1.5 µH, C_{OUT} = 220 uF X 2
Output Voltage Ripple



1 ms/div
V_{IN} = 12 V, V_{OUT} = 2.5 V, Load Current = 1 A,
Output Filter Cap = 220 uF X 2
Shut Down

APPLICATION NOTES

Inductor Selection:

An inductor is one of the energy storage component in a converter. Choosing an inductor means specifying its size, structure, material, inductance, saturation level, DC-resistance (DCR), and core loss. Fortunately, there are many inductor vendors that offer wide selections with ample specifications and test data, such as Vishay Dale.

The following are some key parameters that users should focus on. In PWM mode, inductance has a direct impact on the ripple current. The peak-to-peak inductor ripple current can be calculated as

$$I_{P-P} = \frac{V_{OUT}\ (V_{IN} - V_{OUT})}{V_{IN}\,Lf}$$

where f = switching frequency.

Higher inductance means lower ripple current, lower rms current, lower voltage ripple on both input and output, and higher efficiency, unless the resistive loss of the inductor dominates the overall conduction loss. However, higher inductance also means a bigger inductor size and a slower response to transients. In PSM mode, inductance affects inductor peak current, and consequently impacts the load capability and switching frequency. For fixed line and load conditions, higher inductance results in a lower peak current for each pulse, a lower load capability, and a higher switching frequency.

The saturation level is another important parameter in choosing inductors. Note that the saturation levels specified in data sheets are maximum currents. For a dc-to-dc converter operating in PWM mode, it is the maximum peak inductor current that is relevant, and which can be calculated using these equations:

$$I_{PK} = I_{OUT} + \frac{I_{P-P}}{2}$$

This peak current varies with inductance tolerance and other errors, and the rated saturation level varies over temperature. So a sufficient design margin is required when choosing current ratings.

A high-frequency core material, such as ferrite, should be chosen, the core loss could lead to serious efficiency penalties. The DCR should be kept as low as possible to reduce conduction losses.

Input Capacitor Selection:

To minimize current pulse induced ripple caused by the step-down controller and interference of large voltage spikes from other circuits, a low-ESR input capacitor is required to filter the input voltage. The input capacitor should be rated for the maximum RMS input current:

$$I_{RMS} = I_{LOAD(max)}\sqrt{\frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

It is common practice to rate for the worst-case RMS ripple that occurs when the duty cycle is at 50%:

$$I_{RMS} = \frac{I_{LOAD(max)}}{2}$$

Output Capacitor Selection:

The selection of the output capacitor is primarily determined by the ESR required to minimize voltage ripple and current ripple. The desired output ripple ΔV_{OUT} can be calculated by:

$$\Delta V_{OUT} = (I_{max} - I_{min})\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

Current ripple can be calculated by:

$$(I_{max} - I_{min}) = \frac{T}{L}\frac{V_{OUT}}{V_{IN}}(V_{IN} - V_{OUT})$$

Where: ΔV_{OUT} = Desired Output Ripple Voltage

f = Switching frequency

I_{max} = Maximum Inductor Current

I_{min} = Minimum Inductor Current

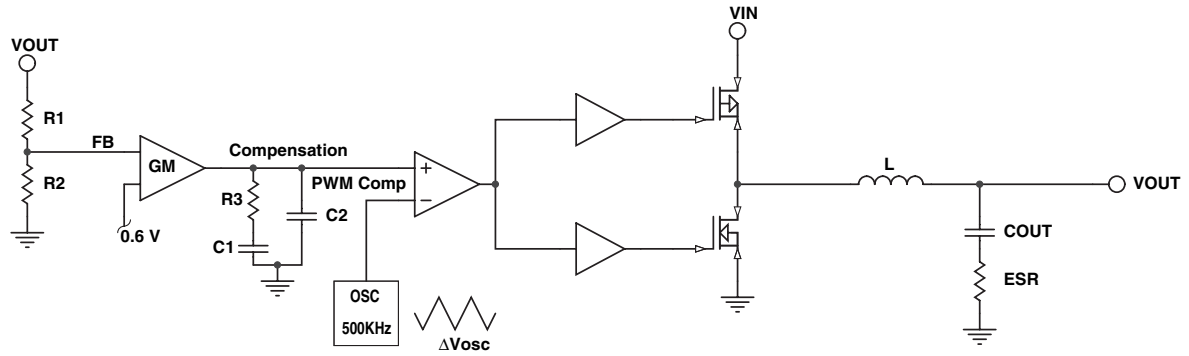
T = Switching Period

Multiple capacitors placed in parallel may be needed to meet the ESR requirements. However if the ESR is too low it can cause instability problems.

MOSFET Selection:

The key selection criteria for the MOSFETs include maximum specifications for on-resistance, drain-source voltage, gate source, current, and total gate charge Qg. While the voltage ratings are fairly straightforward, it is important to carefully balance on-resistance and gate charge. In typical MOSFETs, the lower the on-resistance, the higher the gate charge. The power loss of a MOSFET consists of conduction, gate charge, and crossover losses. For lower-current applications, gate charge losses become a significant factor, so low gate charge MOSFETs, such as Vishay Siliconix's LITTLE FOOT family of PWM-optimized devices, are desirable.

Compensation:



The SiP12201 uses voltage mode control in conjunction with a high frequency Transconductance error amplifier. The voltage feedback loop is compensated at the Comp/$\overline{SD}$ pin, which is the output node of the error amplifier. The feedback loop is generally compensated with an RC + C (one pole, one zero) network from comp to GND. Loop stability is affected by the values of the inductor, the output capacitor, the output capacitor ESR, and the error amplifier compensation network.

The ideal Bode plot for a compensated system would be gain that rolls off at a slope of -20 dB/decade, crossing 0dB at the desired bandwidth and a phase margin greater than 90° for all frequencies below the 0 dB crossing.

The compensation network used with the error amplifier must provide enough phase margin at the 0 dB crossover frequency for the overall open-loop transfer function to be stable. The following guidelines will calculate the compensation pole and zero to stabilize the SiP 12201.

The inductor and output capacitor values are usually determined by efficiency, voltage and current ripple requirements. The inductor and the output capacitor create a double pole at the frequency and a -180° phase change:

$$f_{p(LC)} = \frac{1}{2\pi\sqrt{L * C_{OUT}}}$$

The ESR of the output capacitor and the output capacitor value form a zero at the frequency:

$$f_{Z(ESR)} = \frac{1}{2\pi(ESR)(C_{OUT})}$$

The $f_{Z(ESR)}$ typically should be higher than the $f_{p(LC)}$ and give a 90° phase boost. R3 and C1 will establish the second zero of the system. The frequency of the zero should be 2X lower than the double pole frequency of the inductor and the output capacitor.

$$f_{Z(comp)} = \frac{1}{2\pi R3C1}$$

Choose a value for R3 usually between 1 kΩ and 10 kΩ.

This second zero will provide the second 90° phase boost and will stabilize the closed loop system.

The second pole should be placed at ½ the switching frequency.

$$C2 = \frac{C1}{2\pi * R1 * C1 * F_{SW}^{-1}}$$

Although a mathematical approach to frequency compensation can be used, the added complication of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage, load current variations, all suggest a more practical empirical method. This can be done by injecting at the load a variable frequency small signal voltage between the output and feedback network and using an RC network box to iterate toward the final values; or by obtaining the optimum loop response using a network analyzer to measure the loop Gain and Phase.

Layout:

As in the design of any switching dc-to-dc converter, driver careful layout will ensure that there is a successful transition from design to production. One of the few drawbacks of switching dc-to-dc converters is the noise induced by their high-frequency switching. Parasitic inductance and capacitance may become significant

when a converter is switching at 500 kHz. However, noise levels can be minimized by properly laying out the components. Here are some general guidelines for laying out a step-down converter with the SiP12201. Since power traces in step down converters carry pulsating current, energy stored in trace inductance during the pulse can cause high-frequency ringing with input and output capacitors. Minimizing the length of the power traces will minimize the parasitic inductance in the trace. The same pulsating currents can cause voltage drops due to the trace resistance and cause effects such as ground bounce. Increasing the width of the power trace, which in-creases the cross sectional area, will minimize the trace resistance. In all dc-to-dc converters the decoupling capacitors should be placed as close as possible to the pins being decoupled to reduce the noise. The connections to both terminals should be as short as possible with low-inductance (wide) traces. In the SiP12201 converters, the VIN is decoupled to PGND. It may be necessary to decouple VDD to AGND, with the decoupling capacitor being placed adjacent to the pin. AGND and PGND traces should be isolated from each other and only connected at a single node such as a "star ground".