Smart Power High-Side Switch

PRODUCT SUMMARY			
Overvoltage Protection $V_{bb(AZ)}$ (V)	**Operating Voltage $V_{bb(on)}$ (V)**	**On-State Resistance R_{ON} (mΩ)**	**Nominal Load Current $I_{L(nom)}$ (A)**
41	5 – 15	50	2.0

FEATURES

- Overload Protection
- Current Limitation
- Short Circuit Protection
- Thermal Shutdown with Restart
- Overvoltage Protection (Including Load Dump)
- Reverse Battery Protection with External Resistor
- CMOS Compatible Input
- Start A Cold Filament Lamp
- ESD Protection
- Low Standby Current

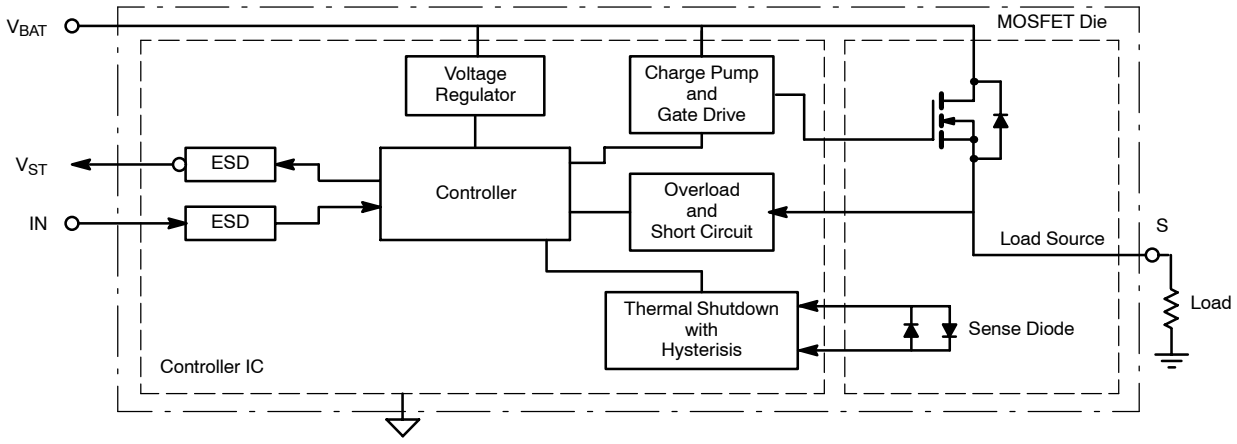
APPLICATIONS

- All Types of Resistive, Inductive and Capacitive Loads
- µC Compatible Power Switch for 12-V dc Applications
- Replaces Electromechanical Relays and Discrete Circuits

DESCRIPTION

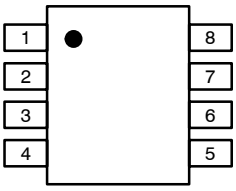
The Si4750DY is an n-channel verticle power FET with charge pump, ground referenced CMOS compatible input, and fully protected by embedded protection functions.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

SO-8



Top View

Ordering Information: Si4750DY—E3
Si4750DY-T1—E3 (with Tape and Reel)

TRUTH TABLE	
IN	**MOSFET**
H	ON
L	OFF

PIN DESCRIPTION		
Pin Number	**Symbol**	**Description**
1	IN	Input Logic Signal
2, 3, 4	V_{BAT}	V_{BAT}/MOSFET Drain, Bypass Cap is Mandatory
5, 6	S	MOSFET Source
7	GND	Ground
8	V_{ST}	Status Output Pin

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter		Symbol	Limit	Unit
Supply Voltage		V_{bb}	15	V
Supply Voltage For Full Short Circuit Protection (T_A = −40 to 150°C)		$V_{bb(SC)}$	15	
Continuous Input Voltage		V_{IN}	−0.7 to 7.5	
Load Current (Short Circuit Current—see page 3)		I_L	Self-Limit	A
Current Through Input Pin (dc)		I_{IN}	±1	mA
Operating Temperature		T_A	−40 to 150	°C
Storage Temperature		T_{stg}	−55 to 150	
Power Dissipation[a]		P_{tot}	1.14	W
Inductive Load Switch-Off Energy Dissipation Single Pluse (T_A = 25°C)		E_{AS}	20	mJ
Load Dump Protection[b, c] (t_d = 15 µs, V_{IN} = low or high, V_{bb} = 14.5 V)		$V_{LOADDUMP}$	25	V
Electrostatic Discharge Voltage (Human Body Model)[d]	Input Pin	V_{ESD}	±1.2	kV
	All Other Pins		±5	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		88	110	°C/W
Junction-to-Case (Drain)[a]	R_{thJC}		29	36	

Notes
a. When Mounted on 1" x 1" PCB FR4 Board.
b. Not tested, specified by design.
c. $V_{LOADDUMP}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839. Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND pin, e.g. witha 150-Ω resistor in GND connection. A resistor for the protection of the input is integrated.
d. According to ANSI EOS/ESD-S5.1-1983 ESD STM5.1-1998.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Noted T_A = 25°C, V_{bb} =14.5 V	Min	Typ	Max	Unit
Load Switching Capabilities and Characteristics						
On-State Resistance	r_{ON}	I_L = 2 A, V_{bb} = 9 to 14.5 V		34	50	mΩ
Nominal Load Current	$I_{L(nom)}$			2		A
Turn-On- Time to 90% V_{OUT}	t_{ON}	I_L = 2 A, C_L = 2 μA		70	150	μs
Turn-Off Time to 10% V_{OUT}	t_{off}			60	150	
Slew Rate On	dV/dt_{on}			0.22		V/μs
Slew Rate Off	$-dV/dt_{on}$			0.08		
Operating Parameters						
Operating Voltage	$V_{bb(on)}$		9		41	V
Undervoltage Shutdown of Charge Pump	$V_{bb(under)}$	T_A = −40 to 85°C		6.7	8	
Undervoltage Restart of Charge Pump	$V_{bb(ucp)}$			7.1	8	
Standby Current	$I_{bb(off)}$	T_A = −40 to 85°C, V_{IN} = 0 V		70		μA
Leakage Output Current (Included in $I_{bb(off)}$)	$I_{L(off)}$	V_{IN} = 0 V			0.5	
Protection Features						
Initial Peak Short Circuit Current Limit	$I_{L(SCp)}$	t_m = 500 μs, T_A = 25°C		21		A
		t_m = 500 μs, T_A = 25°C		19		
Thermal Overload Trip Temperature	T_J	I_L = 2 A	150			°C
Thermal Hysteresis	T_{HYS}			12		
Reverse Battery						
Reverse Battery[b]	$-V_{bb}$				25	V
Drain-Source Diode Voltage	$-V_{ON}$	$V_{OUT} > V_{bb}$, T_J = 150°C		600		mV
Input						
Input Turn-On Threshold Voltage	$V_{IN(T+)}$	See Figure 1		2.3	3.0	V
Input Turn-Off Threshold Voltage	$V_{IN(T-)}$		0.8			
Input Threshold Hysteresis	$\Delta V_{IN(T)}$			1		
Off-State Input Current	$I_{IN(off)}$	V_{IN} = 0.7 V, See Figure 1			2	μA
On-State Input Current	$I_{IN(on)}$	V_{IN} = 5 V, See Figure 1			2	
Input Resistance	R_L	Input Resistance, See Figure 1		3000		kΩ

Notes
a. Not to exceed T_{PULSE} = 50 ns.
b. Requires a 150-Ω resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Power dissipation is higher compared to normal operating conditions due to the voltage drop across the drain-source diode. The temperature protection is not active during reverse current operation. Input current has to be limited. (See Maximum Ratings, page 2.)

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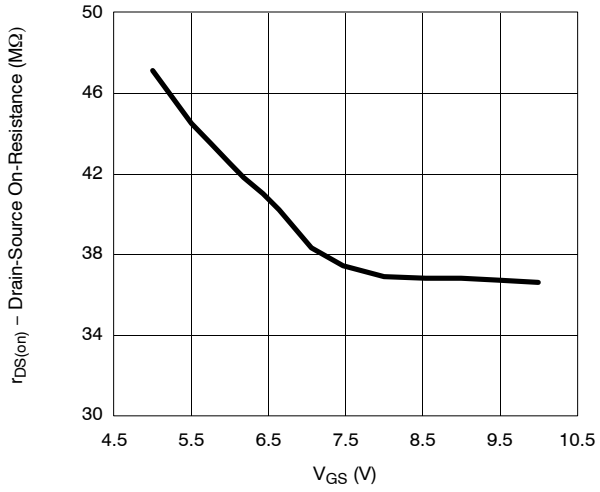
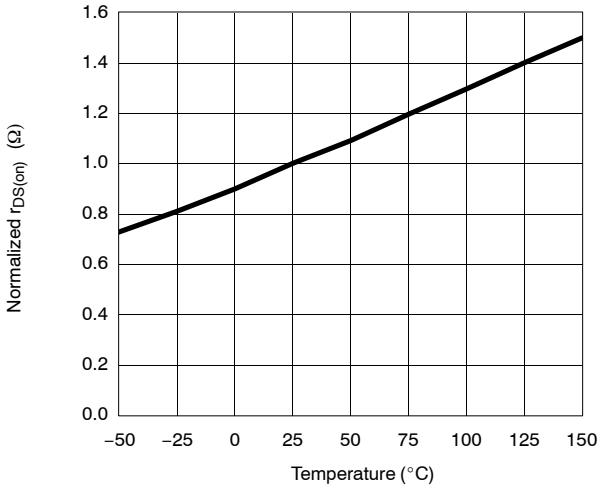
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

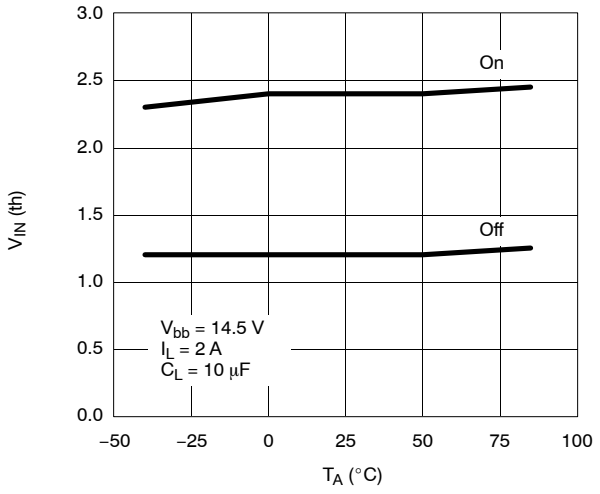
$r_{DS(on)}$ vs. V_{GS} @ 25°C



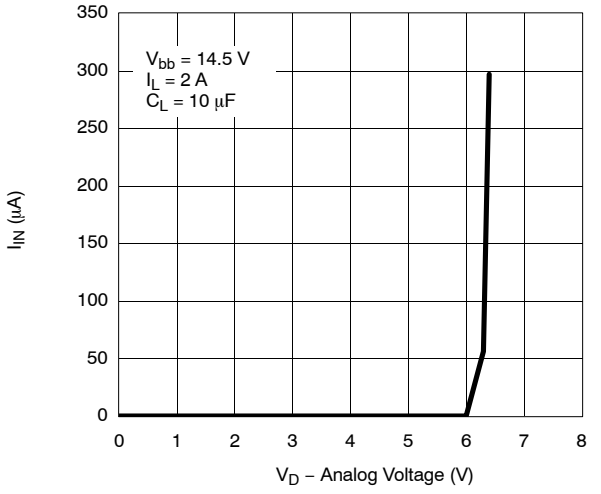
Normalized $r_{DS(on)}$ vs. Temperature



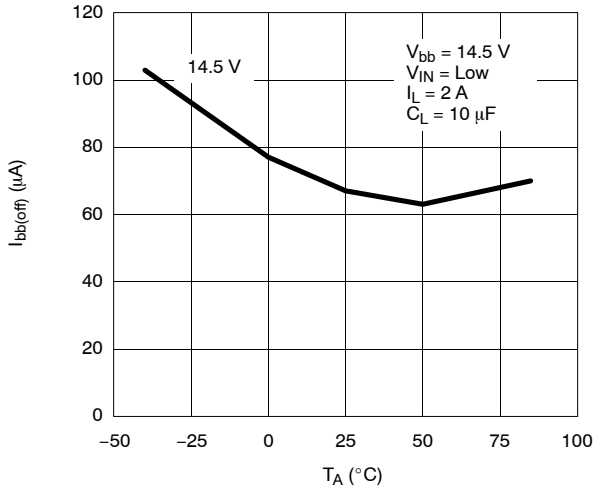
Typical Input Threshold Voltage



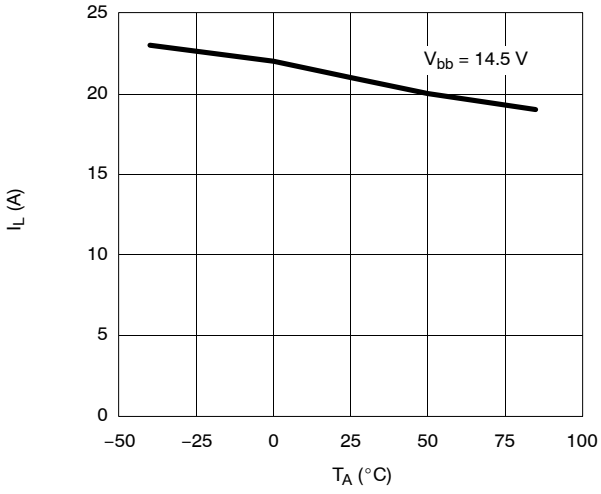
Typical Input Current



Typical Standby Current



Initial Peak Current Limit Under A 2-A Lamp Load



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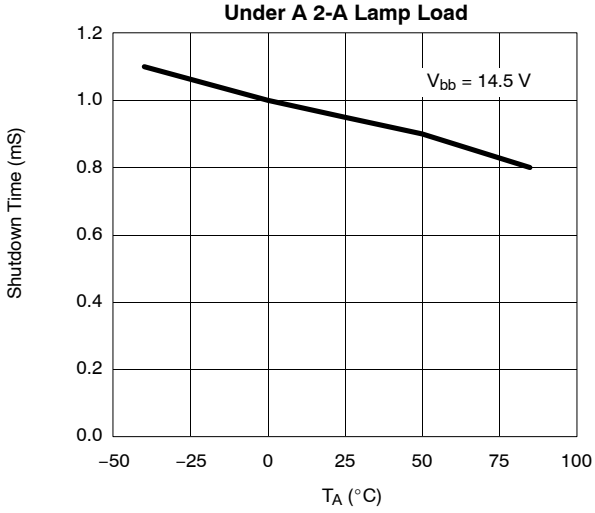
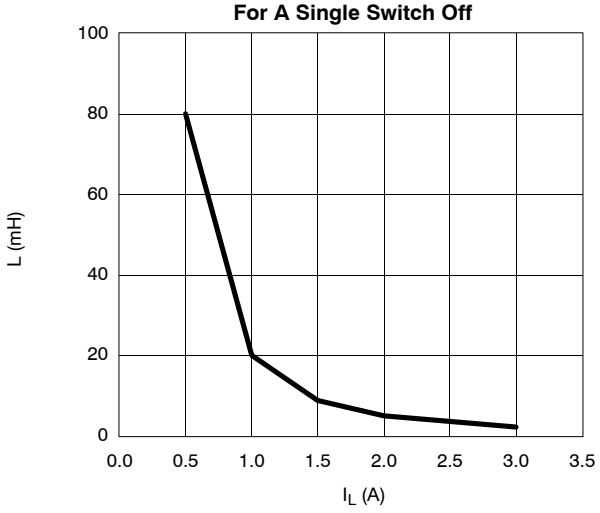
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

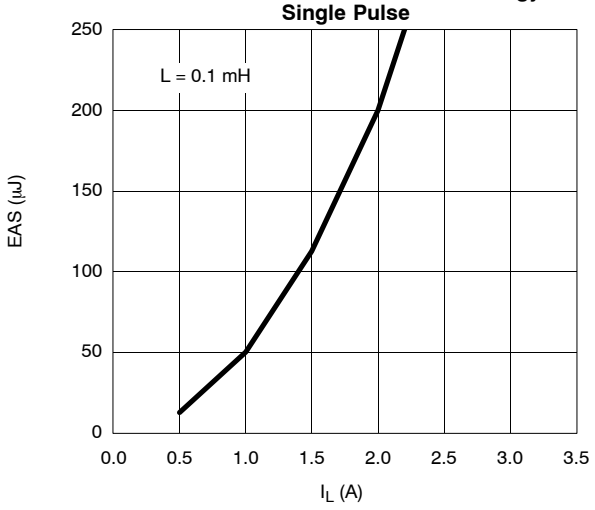
Initial Shutdown Time Under A 2-A Lamp Load



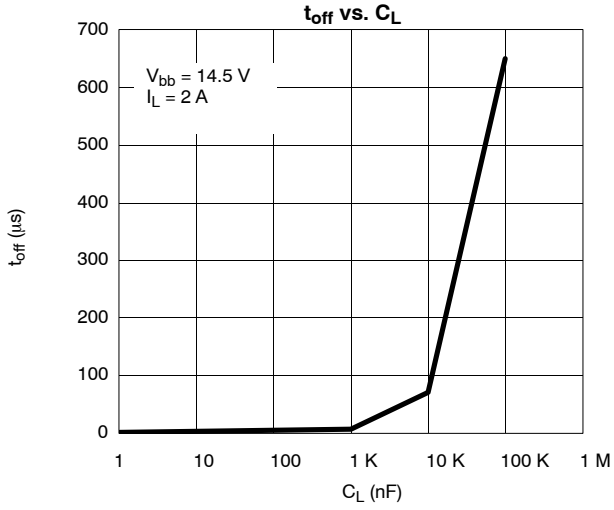
Maximum Allowable Load Inductance For A Single Switch Off



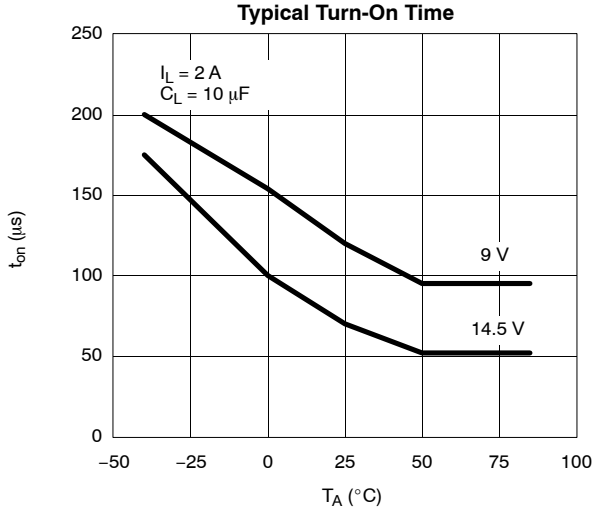
Maximum Inductive Switch Off Energy Single Pulse



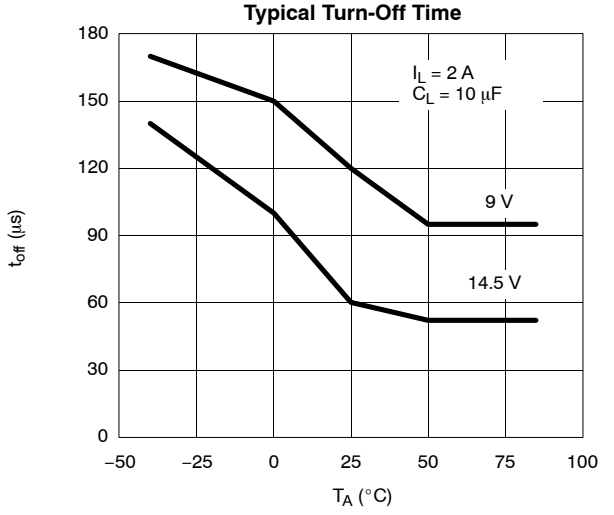
t_{off} vs. C_L



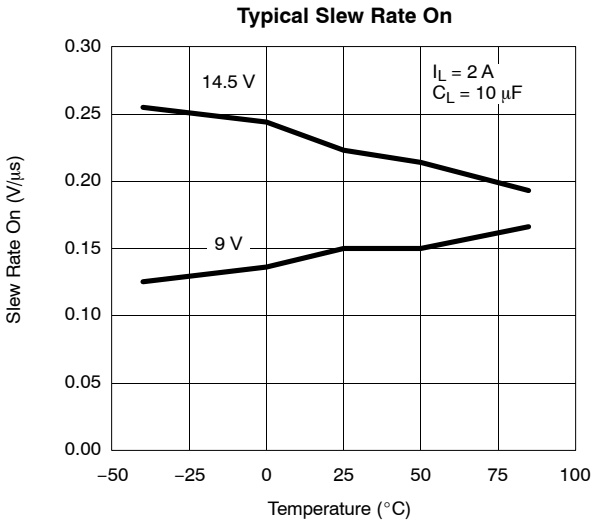
Typical Turn-On Time

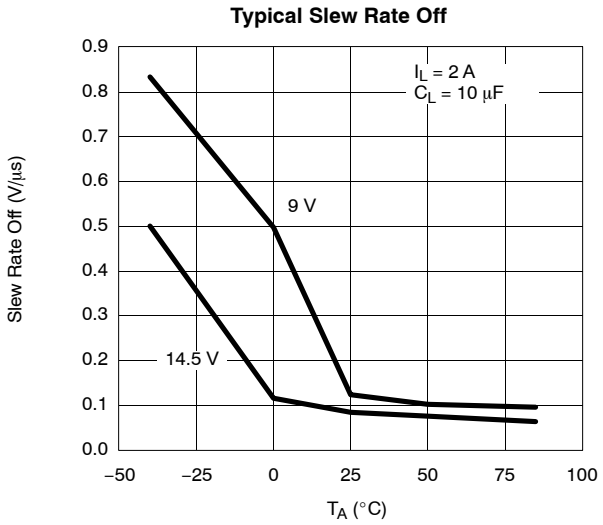


Typical Turn-Off Time



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





SETUP

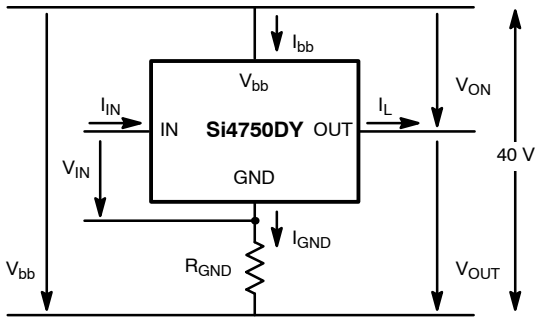


FIGURE 1.

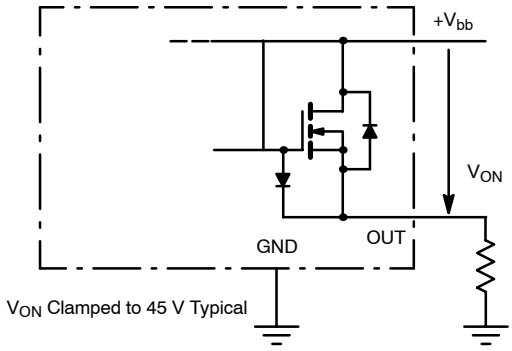


FIGURE 2. Inductive and Overvoltage Output Clamp

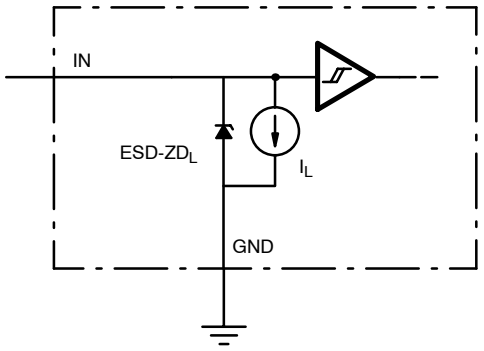


FIGURE 3. Input Circuit (ESD Protection)

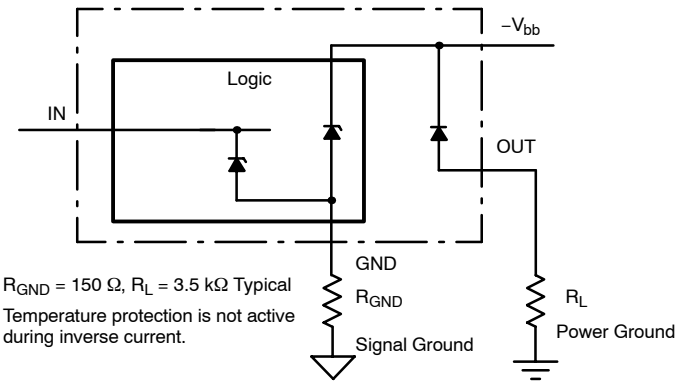


FIGURE 4. Reverse Patterv Protection

TIMING DIAGRAMS

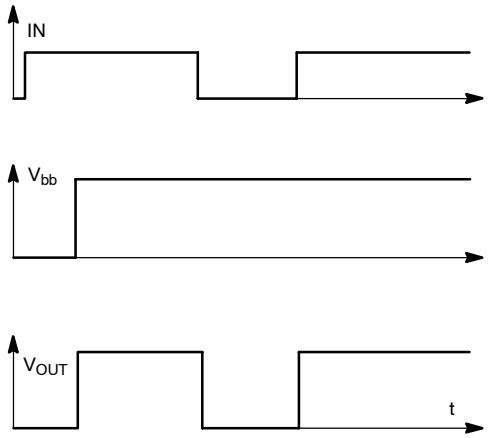


FIGURE 5. V_{bb} Turn-On

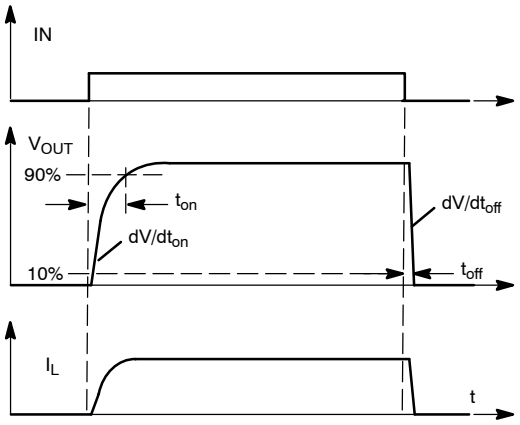


FIGURE 6. Switching A Resistive Load, Turn-on/0ff Time and Slew Rate Definition

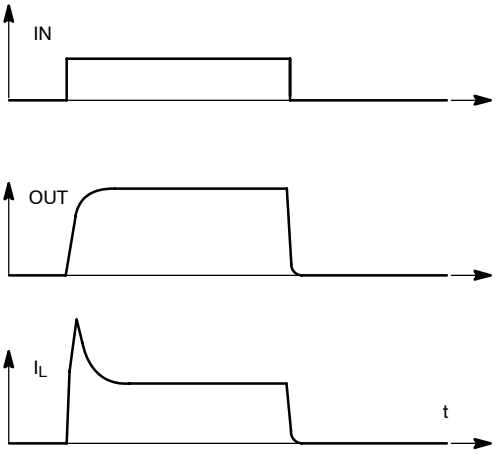


FIGURE 7. Switching A Lamp

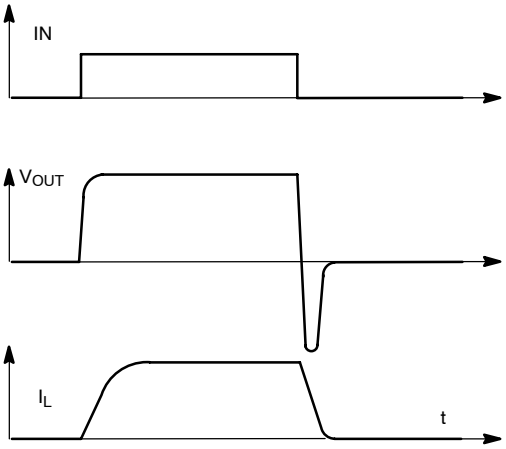


FIGURE 8. Switching An Inductive Load

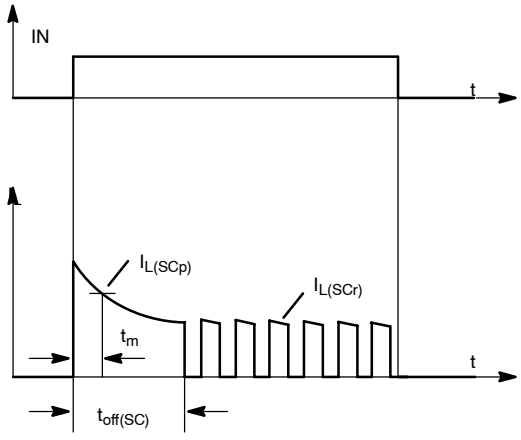


FIGURE 9. Turn-On Into Short Circuit Driving A Cold Filament

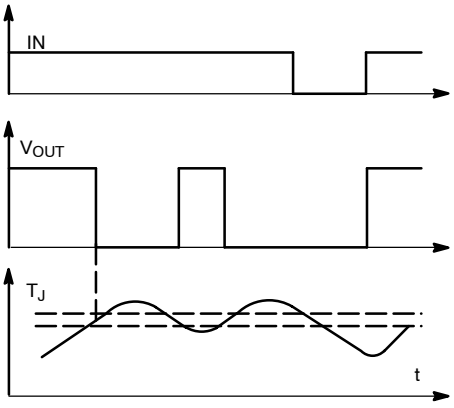


FIGURE 10. Overtemperature: Reset If $T_J < T_{JT}$

TIMING DIAGRAMS

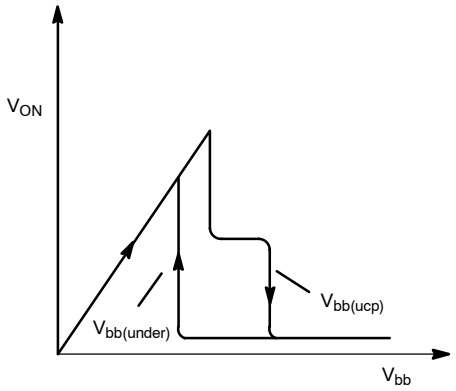


FIGURE 11. Undervoltage Restart of Charge Pump