

DATA SHEET

SA910

Variable gain RF predriver amplifier

Product specification

1997 Aug 12

Variable gain RF predriver amplifier

SA910

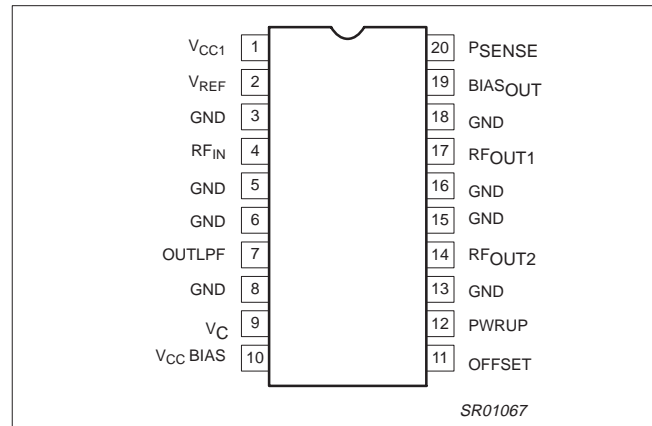
DESCRIPTION

The SA910 is a variable gain predriver amplifier designed for handheld analog cellular telephones. When used with a UHF power transistor, it forms a cost-effective, low-profile, surface mount power amplifier solution (1.2W maximum PAE > 50%). The SA910 integrates power detection and control circuitry that is stabilized over temperature and voltage. In power down mode, the SA910 draws less than 10 μ A of current. The SA910 is fabricated using Philips QUBiC BiCMOS process.

FEATURES

- MMIC BiCMOS predriver amplifier
- Low voltage 2.7 to 5.5V single supply operation
- 820 to 905MHz bandwidth
- High power gain >20dB
- High power output >23dBm (typical) @ 3V
- Efficiency = 35% (typical)
- Wide gain control range: >32dB
- Few external components required
- Integrated power detector and comparison gain control circuitry
- 50 Ω input, open-collector output
- SSOP-20 package
- Integrated regulator with offset adjustment for biasing an external output stage

PIN CONFIGURATION



APPLICATIONS

- 900MHz analog cellular
- Handheld transmitting equipment in the 820 to 905MHz frequency range
- Cordless phone

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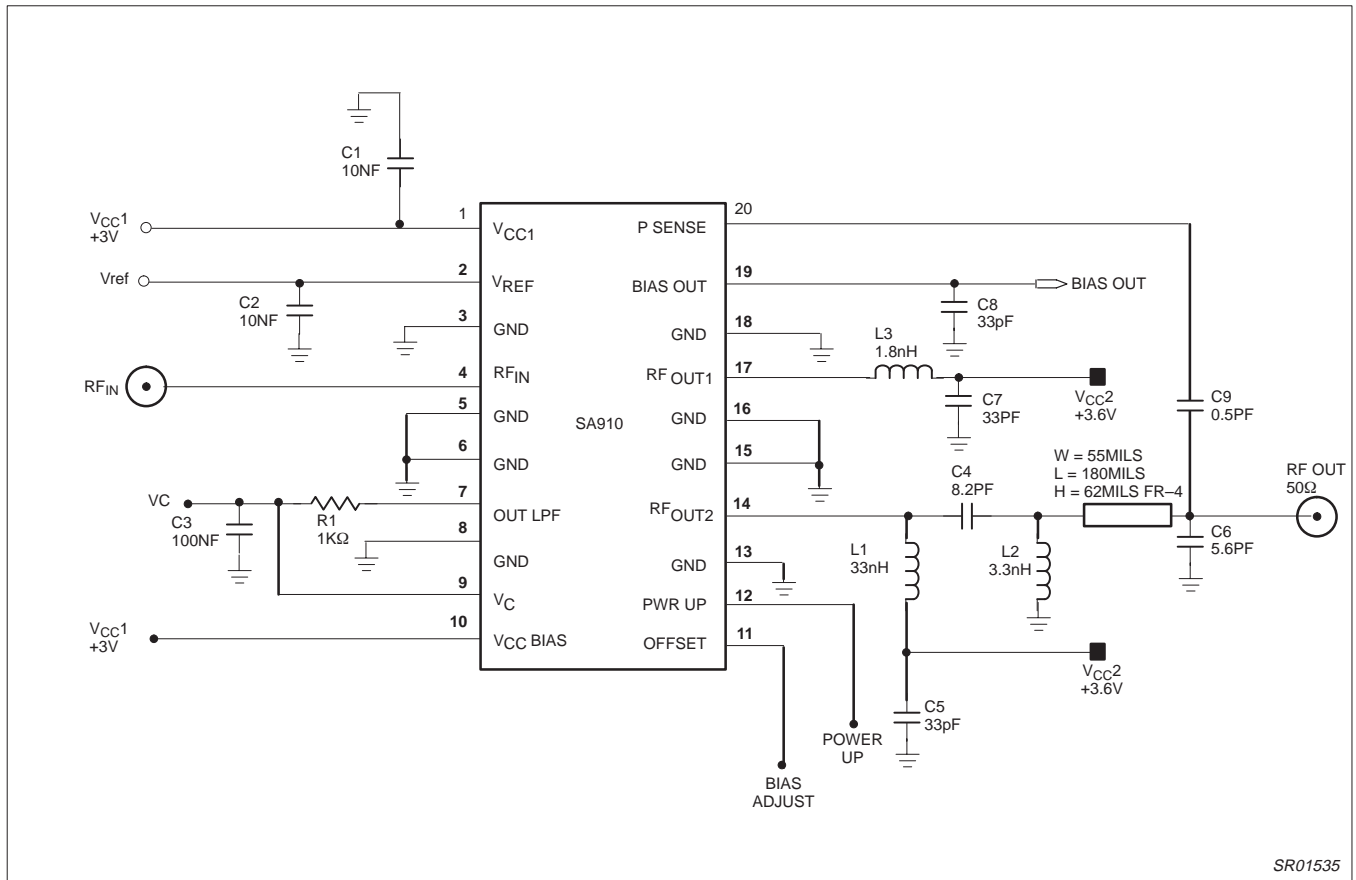


Figure 1. Application Diagram

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic SSOP (Shrink Small Outline Package)	-40 to +85°C	SA910	SOT266-1

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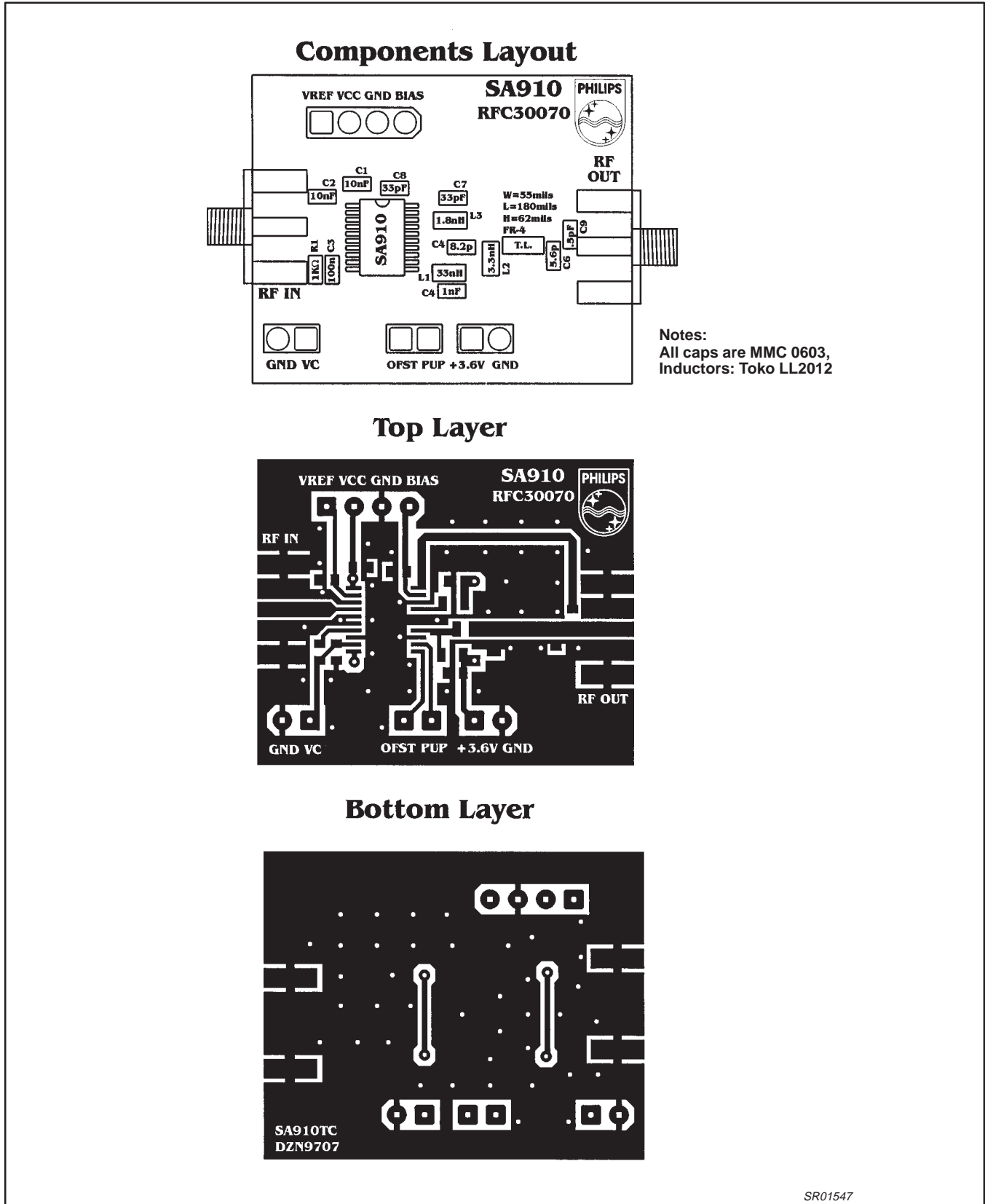


Figure 2. Application Board Layout of SA910

SR01547

Variable gain RF predriver amplifier

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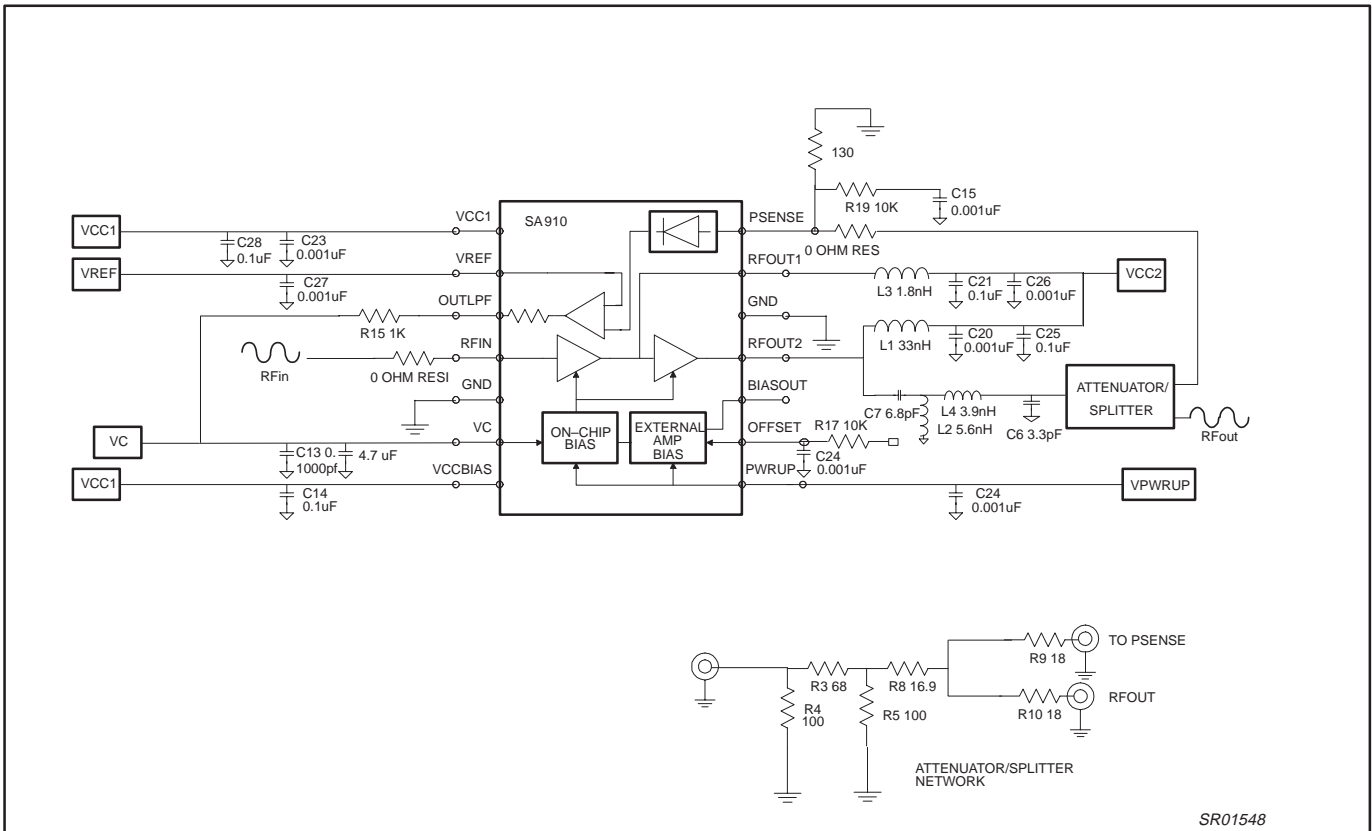


Figure 3. Test Circuit Used In Characterizing SA910

BLOCK DIAGRAM

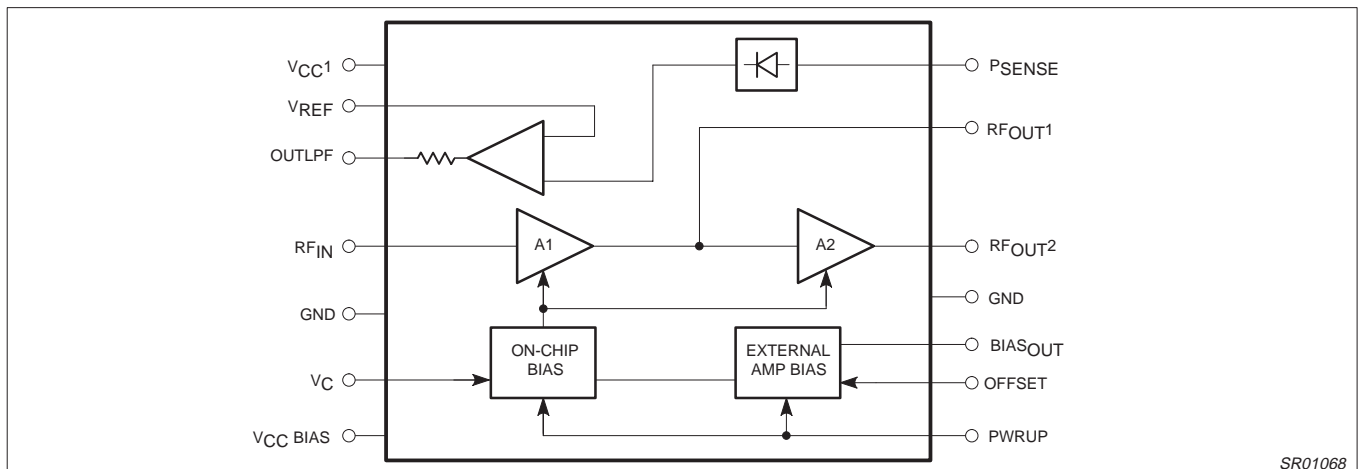


Figure 4. Block Diagram

SR01068

Variable gain RF predriver amplifier

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PIN DESCRIPTIONS

Pin No.	Mnemonic	Function
1	V _{CC1}	Power supply for power sense loop and off-chip bias
2	V _{REF}	Power sense reference voltage input
3	GND	Ground
4	RF _{IN}	Pre-driver input
5	GND	Ground
6	GND	Ground
7	OUTLPF	Power sense detected output
8	GND	Ground
9	VC	Gain control input
10	V _{CC} BIAS	Power supply for on-chip bias
11	OFFSET	External power amp bias offset adjustment
12	PWRUP	Power-up input
13	GND	Ground
14	RF _{OUT2}	Pre-driver output (open collector)
15	GND	Ground
16	GND	Ground
17	RF _{OUT1}	Output of first stage (open collector)
18	GND	Ground
19	BIAS _{OUT}	Output to bias external power amplifier stage
20	P _{SENSE}	Power sense input

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V _{CC1} /V _{CCBIAS}	DC supply voltages	-0.3 to +6.0	V
	Voltage applied to any other pin ¹	-0.3 to (V _{CC1} + 0.3)	V
P _D	Power dissipation	1.0	W
P _{IN}	Input drive power	5	mW
P _{DET}	Input detect power	20	mW
P _L	Load power	500	mW
T _{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Except RF_{OUT1} and RF_{OUT2} which can have 8V max.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V _{CC1} /V _{CCBIAS}	Supply voltage	3 to 3.6	V
T _A	Operating ambient temperature range	-40 to +85	°C

NOTE:

1. R_{th} = 75° c/w

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AC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CCBIAS} = +3V$; $V_{CC}(RF_{OUT1}, RF_{OUT2}) = 3.6V$; $T_A = 25^{\circ}C$, $Z_S = Z_L = 50\Omega$; $V_C = 2V$; $RF_{IN} = 0dBm$ @ 830MHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
f_{RF}	Frequency range		820	830	905	MHz
P_L	Load power at RF_{OUT2}	Saturated ¹	21.5	24		dBm
S_{21}	Small signal gain	$RF_{in} = -20dBm$		31		dB
η	Power added efficiency	$P_L = 24dBm$		35		%
S_{11}	Input return loss	$RF_{in} = 0dBm$		-12		dB
G_C	Gain control range from $V_C = 0.7$ to $2V$	$dP/dV < 120dB/V$	32			dB
S_{12}	Reverse isolation			-40		dB
GOFF	Gain at RF_{OUT2} during power-down ($RF_{IN} = -20dBm$)			-30		dB
PSENSE	Power detector range			25		dB

NOTE:

- Needs proper output matching.

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DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CCBIAS} = +3V$, $V_{CC} (RF_{OUT1}, RF_{OUT2}) = 3.6V$; $T_A = 25^\circ C$, $Z_S = Z_L = 50\Omega$, ; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-3 σ	TYP	+3 σ	MAX	
V_{CC}	Power supply voltage range		2.7		3.0		5.5	V
I_{CC}	Total DC current from all V_{CC}	Pin 12 = HIGH; Pin 9 > V_{BE}			210		300	mA
I_{ZB}	I_{CC} under zero bias mode	Pin 12 = HIGH; Pin 9 < V_{BE}					0.7	mA
I_{OFF}	Powerdown current	Pin 12 = LOW					10	μA
I_{PU}	Input current to PWRUP	Pin 12 = HIGH					100	μA
		Pin 12 = LOW					10	
V_{PU}	Input level for PWRUP (Pin 12)	Pin 12 = LOW	0				$0.3V_{CC}$	V
		Pin 12 = HIGH	$0.7V_{CC}$				V_{CC}	V
I_{REF}	Input current to V_{REF} (Pin 2)					1	μA	
V_{REF}	Power control reference voltage (Pin 1)		0				2.0	V
V_{BIAS}	Bias _{OUT} voltage (Pin 19) (unadjusted)	$V_C = 2.0V$			0.68			V
I_{BIAS}	DC current available @ Bias-OUT (Pin 19)		30					mA
V_C	Control voltage (Pin 9) range		0				2	V

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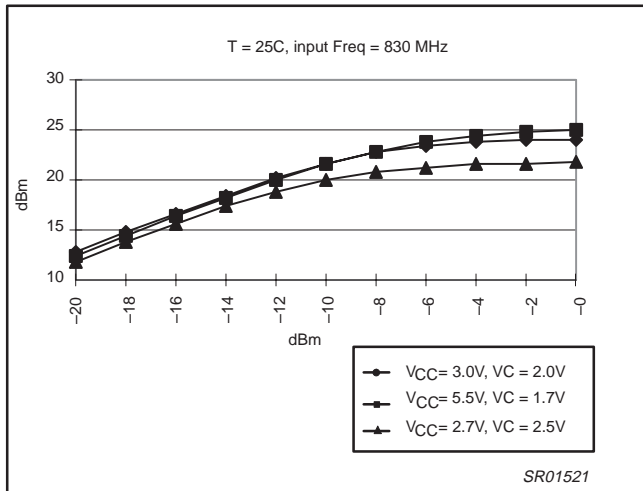


Figure 5. Output Power VS Input Power

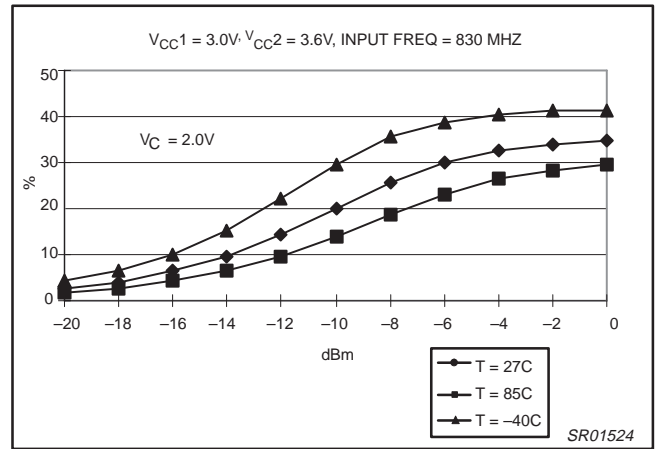


Figure 8. PAE VS Input Power

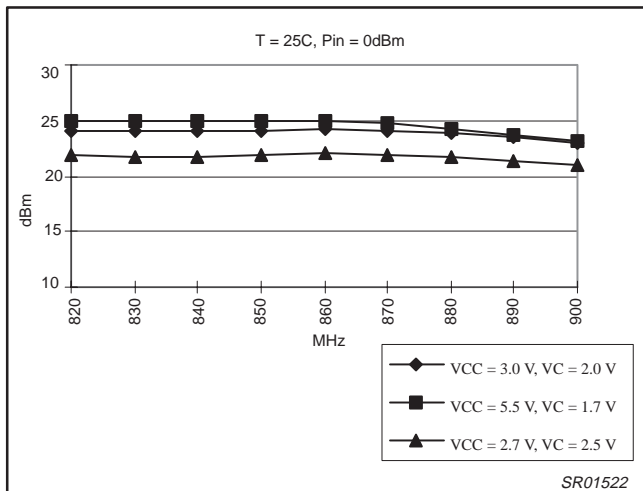


Figure 6. Output Power VS Input Frequency

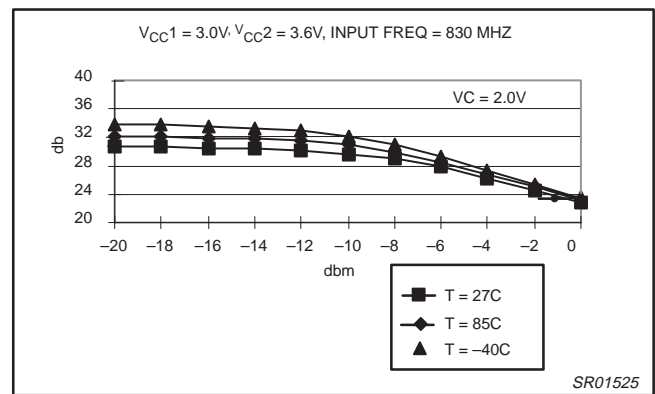


Figure 9. Signal Gain VS Input Power

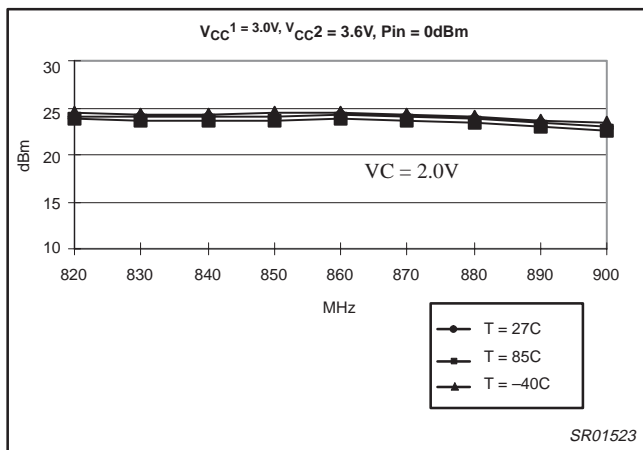


Figure 7. Output Power VS Input Frequency

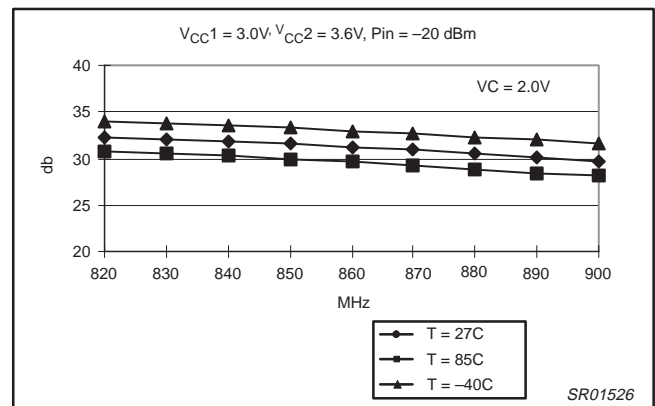


Figure 10. Signal Gain VS Input Frequency

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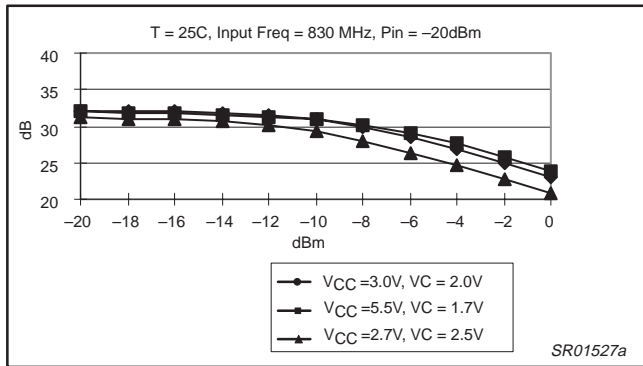


Figure 11. Signal Gain VS Input Power

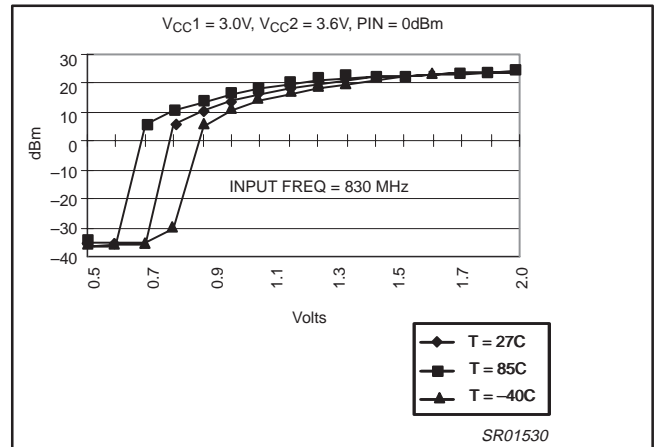


Figure 14. Output Power VS VC

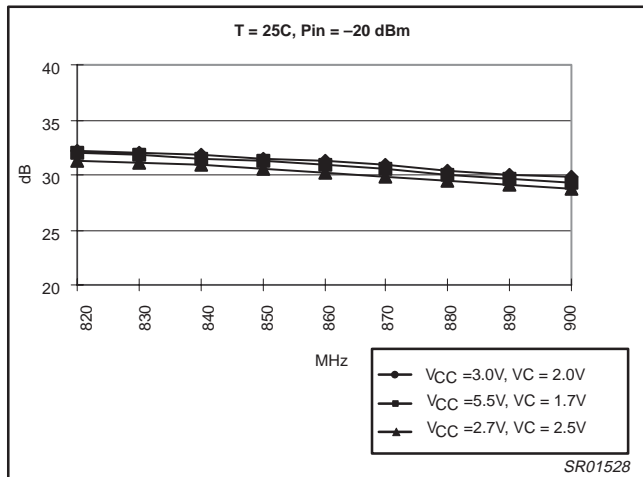


Figure 12. Signal Gain VS Input Frequency

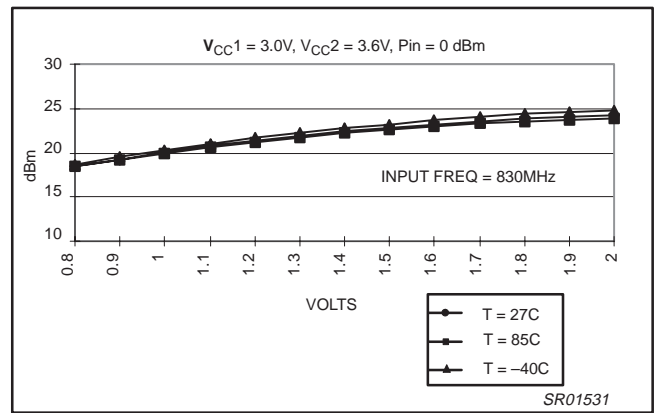


Figure 15. Output Power VS VREF (Closed Loop)

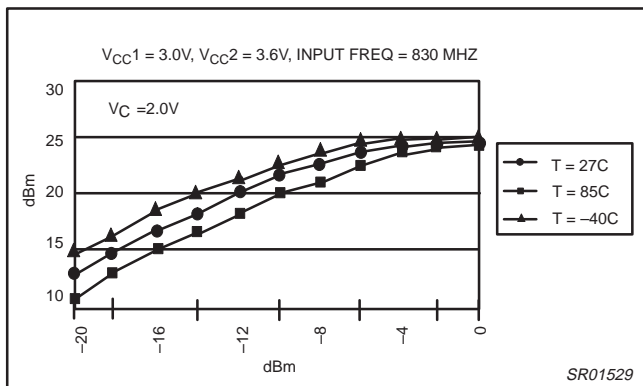


Figure 13. Output Power VS Input Power

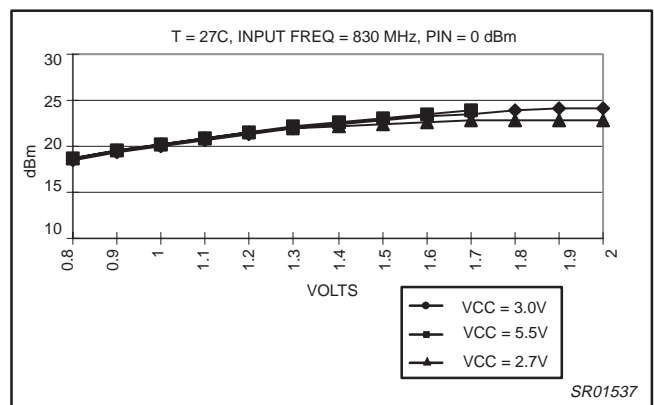


Figure 16. Output Power VS VREF (Closed Loop)

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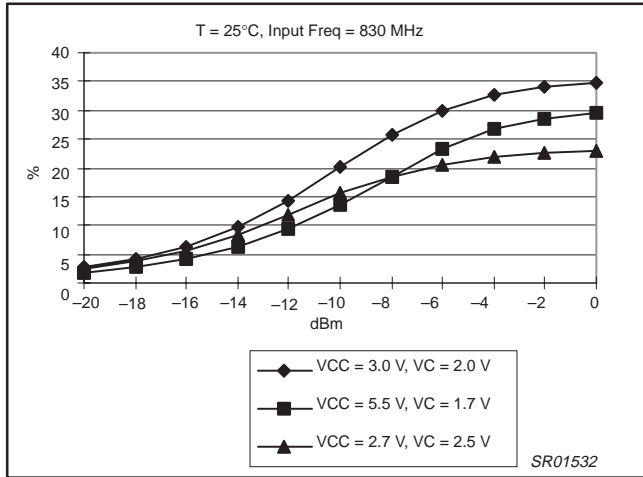


Figure 17. PAE VS Input Power

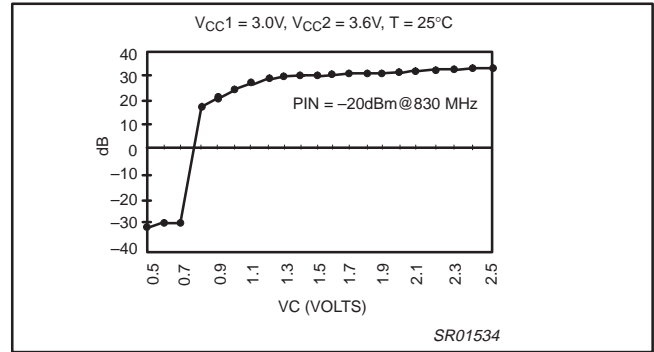


Figure 19. Small Signal Gain VS VC

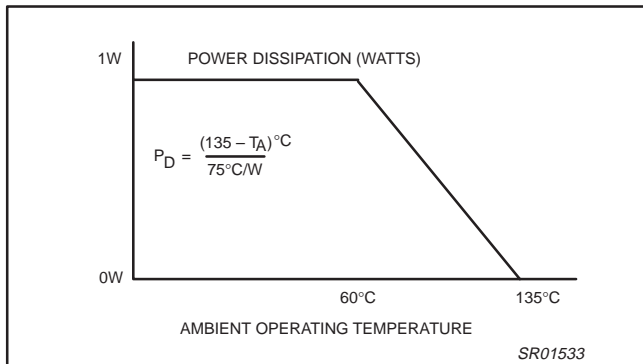


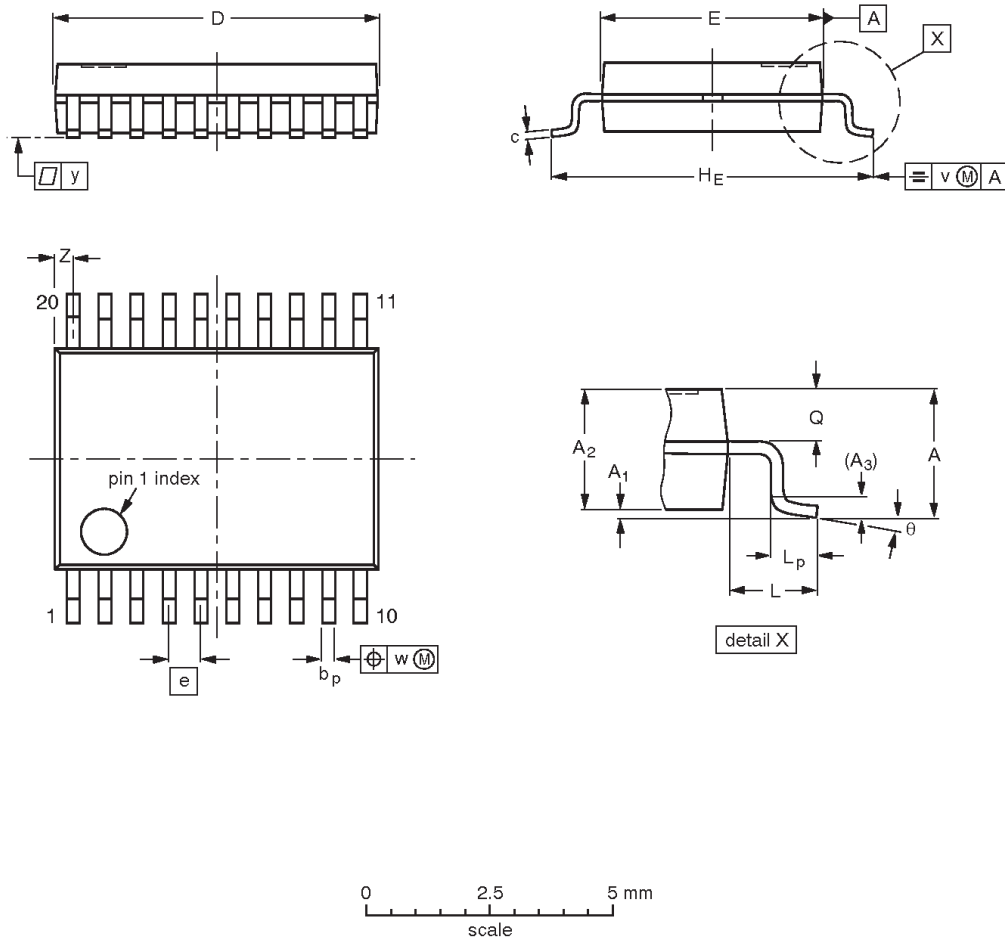
Figure 18. Power De-Rating Curve

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SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT266-1						90-04-05 95-02-25

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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