S6B33A2

128 RGB Segment & 129 Common Driver For 4,096 Color STN LCD

Sep. 06. 2002.
Ver. 1.3

S6B33A2 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Oct. 2001
0.1	1. Page11 - Added & Changed Test Pin 2. Page24 - Deleted “Data Bus Mode Set” Instruction - Deleted “Driving Current Mode & Bias Set” Instruction - Deleted “Row Vector Mode Set” Instruction - Added “DDRAM Burst Mode On/Off” Instruction 3. Page25 - Deleted “Data Bus Mode Set” description 4. Page26 - Reduced bus bandwidth of DIV(1) and DIV(2) 5. Page28 - Deleted “Driving Current Mode and Bias Set” description 6. Page33 - Deleted “Row Vector Mode Set” description - Added “DDRAM Burst Mode On/Off” description 7. Page37 - Deleted “MDI” bit in “Entry Mode Set” parameters 8. Page49 - Modified the register list and parameters according to modification	Nov. 2001
0.2	- Page2 - Deleted C24+, C24- pin in block diagram 2.Page 9 - Deleted C24+, C24- pin in pin description 3.Page12 - Deleted “REG_ENB” pin - Deleted “TEST2”, “TEST3” pin 4.Page23 - Delete “REG_ENB” pin on figure20 5.Page25 - Added “Red, Green and Blue Palette Set” instruction. 6.Page 28 - Changed DCDC clock division ratio 7.Page 35 - Added “GSM” bit for gray scale selection at “Gray Scale Mode Set” instruction - Page 37 - Added “Red, Green and Blue Palette Set” description - Page38 - Added “HL” bit at “Entry Mode Set” instruction - Page 50 - Modified the register list and parameters according to modification 11.Page 54 - Changed Oscillator frequency tolerance and range 12.Page41,43,44,55,56 - The duty of partial mode1 is changed from 1/69 to 1/66	Dec. 2001

S6B33A2 Specification Revision History		
Version	**Content**	**Date**
0.3	- Page4~9 - Added key coordinates, pad dimension, configuration and coordinates 2. Page59 - Added " the limitation of usage of analog circuit" in detail 3. Page65~66 - Added system application diagram	Jan. 2002
0.4	1. Page3 - Deleted CK Pin 2. Page10 - Modified pin description 3. Page16 - Collected the code of X,Y address 4. Page 50 - Described write/read data which is accessed by MCU I/F in 256 color mode	Jan. 2002
0.5	1. Page5 - Deleted *note about ILB, TOM align key	Jan.2002
0.6	- Page26, 50 - Added display format select command(60H/61H) 2. Page27 - Added " DIV2" bit at " Oscillation Mode Set" instruction 3. Page66 - Add maximum rating voltage of capacitors	Mar.2002
0.7	- Page 26,35,36 - Delete Burst mode on/off instruction 2. Page 59,60 – Add MPU 68/80 Parallel I/F AC Timing	May.2002
0.8	1. Page 65 - Add shot-key diode at application circuit	May.2002
0.9	1. Page 26, 35, 51 - Add ROW Vector Mode Set Command	May.2002
1.0	1. Page 65 - Add Values of Schottky barrier diode.	Jun.2002
1.1	1. Page 30 - Corrected Miss-typing.	Jul.2002
1.2	1. Page 53~61 - Filled TBD items	Jul.2002
1.3	1. Page 18 - Delete " Block NO" on figure15. 2. Page 59-60 - Delete a word of " 25°C" from condition item on table17. 3. Page 54 - Add DC Spec of DC2IN, VIN2 and VIN45 4. Page 55 - Add Current Measure data	Sep.2002

CONTENTS

INTRODUCTION

S6B33A2 is a mid-display-size-compatible driver for liquid crystal dot matrix gray-scale graphic systems. With on-chip RC oscillator circuit, the display-timing signal is generated without being sent from MPU. Also, it is capable of using 8bit/16bit data bus alternatively and operating with 68/80-series MPU in asynchronous. Due to the internal bit-map display RAM of 128 ×128 ×12-bit, S6B33A2 is capable of operating max. 128 RGB x 128 dot LCD panels in low-power consumption. Being the segment RGB 3-output, one pixel is 12-bit data and S6B33A2 can display 4,096 color.

FEATURES

Driver Output

– 129 COM X 128 RGB SEG

Gray Scale Function

– 4,096 color display of R: 16 gray scale, G: 16 gray scale, B: 16 gray scale
– 256 color display of R: 8 gray scale, G: 8 gray scale, B: 4 gray scale

On-chip Display Data RAM

– Capacity: 128 x 128 x 12 = 196,608 bits

Display Mode

– Normal display mode: Entire duty displaying
– Partial display mode: Partial displaying
– Standby mode: Internal display clocks off
– Area scroll mode: Particular area scrolling

Microprocessor Interface

– 8-bit/16 bit parallel bi-directional interface with 6800-series or 8080-series
– 3/4 Pin SPI (only write operation)

On-chip Low Power Analog Circuit

– On-chip RC oscillator (Internal cap. & external resistor), external clock available
– Voltage converter
– Voltage regulator
– Voltage follower
– On-chip electronic contrast control (256 steps)
– Bias ratio: 1/6

Operating Voltage Range

– VDD : 1.8 to 3.3 [V] (without Internal Regulator), 2.4 to 3.3 [V] (With internal Regulator)
– VIN1: 2.4 to 3.6 [V]
– Display operating voltage(V1): 2.0 to 3.3 V
– LCD Operating Voltage Range : 20 V

Low Power Consumption

- 650 uA Typ.

Package Type

- COG

Output Pad Pitch

- 38um Min.

BLOCK DIAGRAM

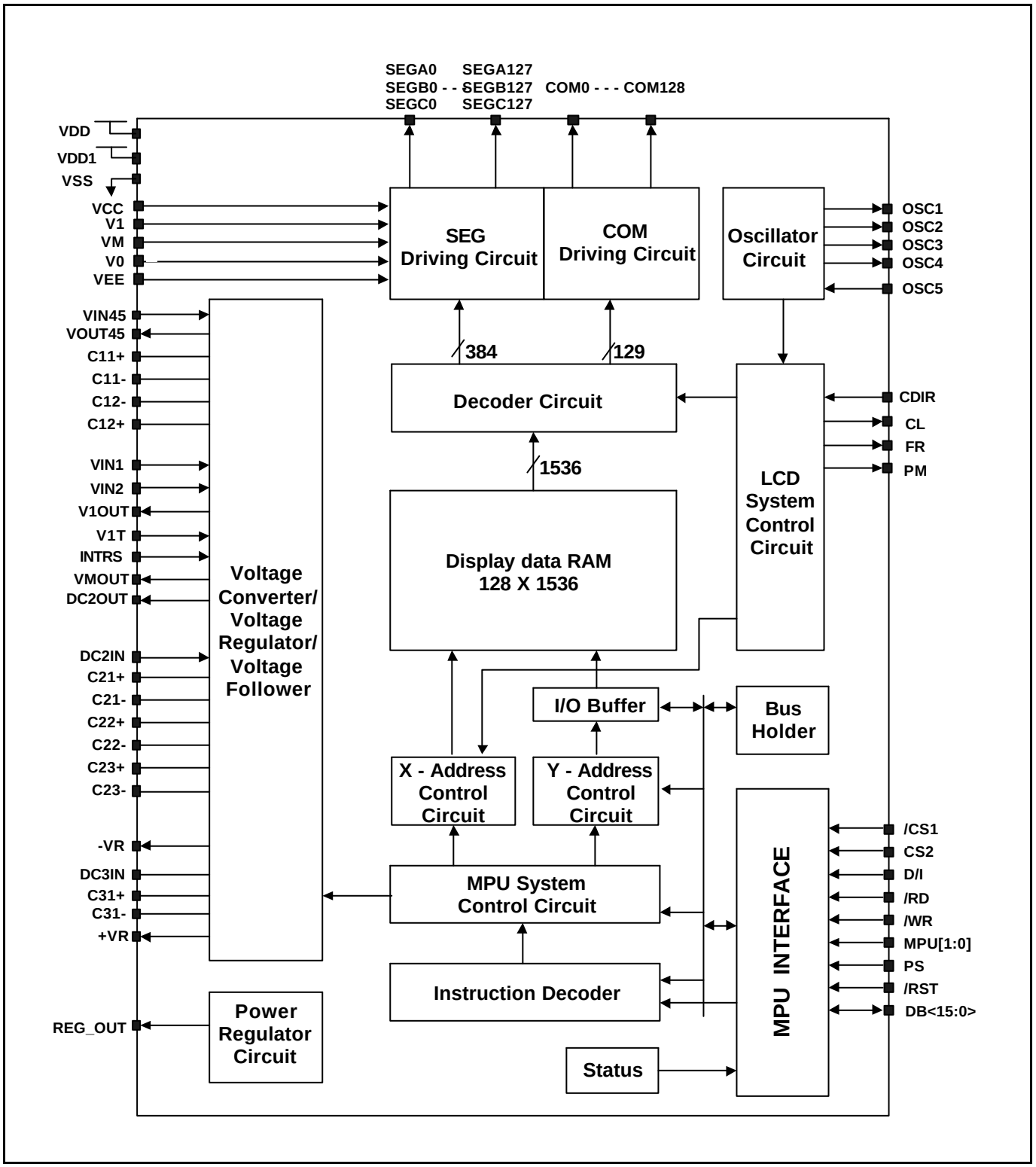


Figure 1. Block Diagram

PAD CONFIGURATION

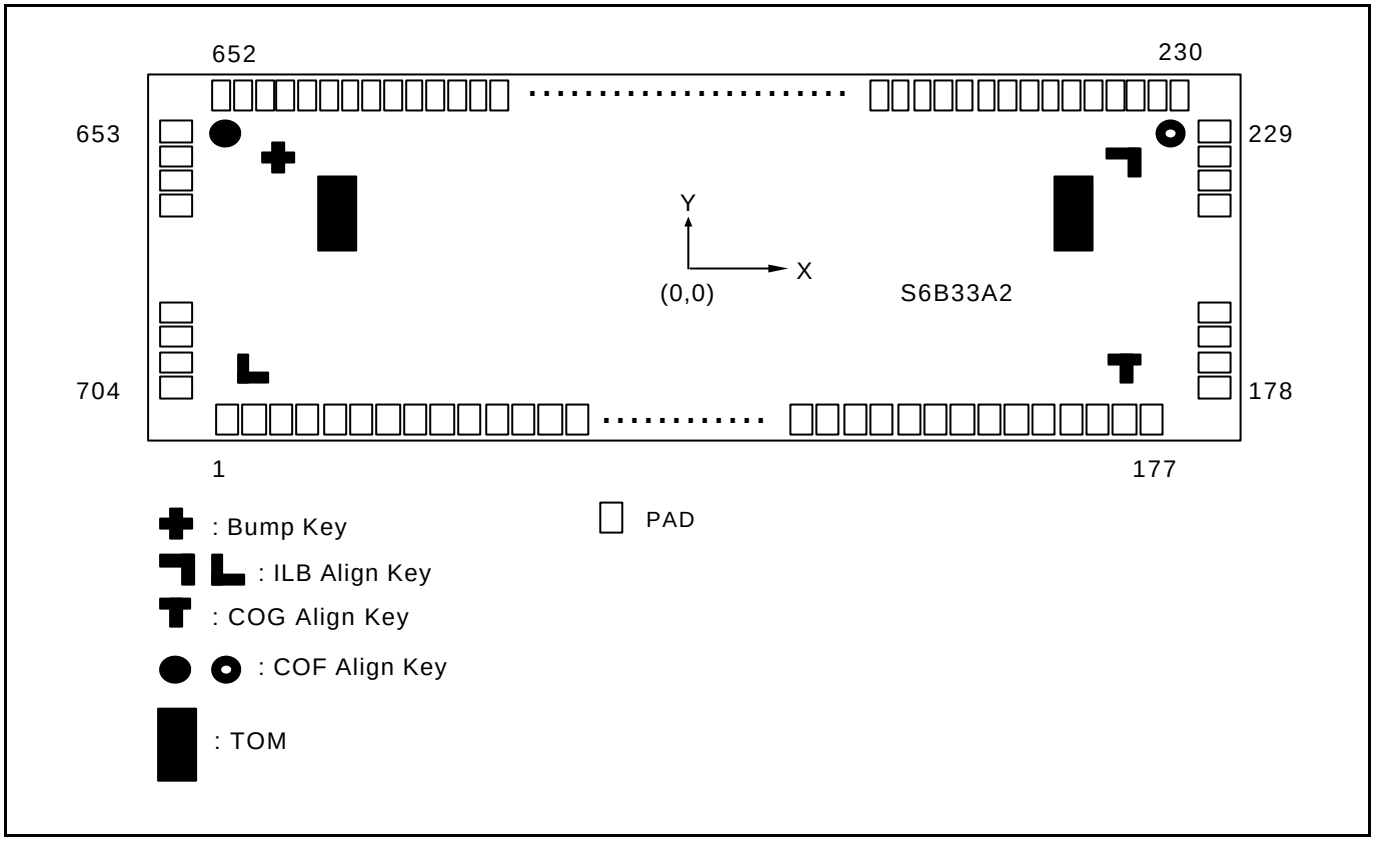
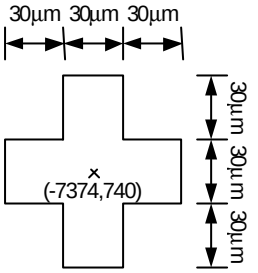


Figure 2. S6B33A2 Chip Pad Configuration

Table 1. S6B33A2 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	16670	2430	*m*m
Pad pitch	1 ~ 177	90		
	178 to 229, 230 to 652, 653 to 704	38		
Bumped pad size	1 ~ 177	70	70	
	178 to 229, , 653 to 704	170	23	
	230 to 652	23	170	
Bumped pad height	All Pad	17		

Figure 3. Bump, COG Align Key Coordinate



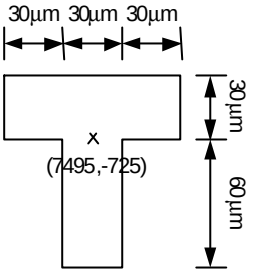
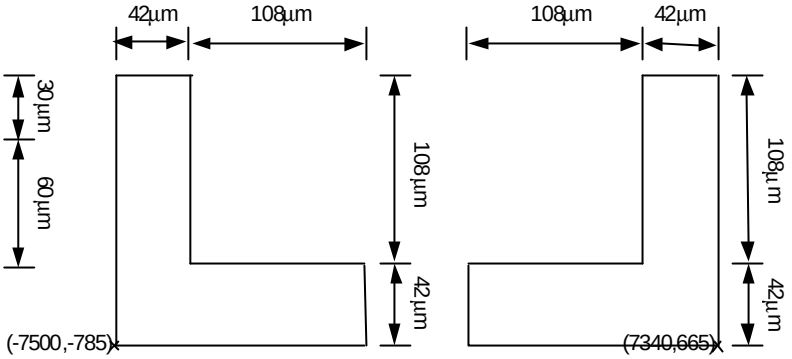


Figure 4. ILB Align Key Coordinate



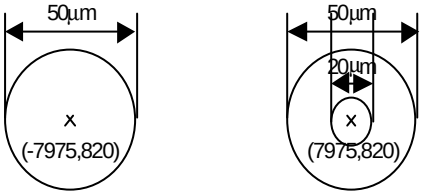


Figure 5. COF Align Key Coordinate

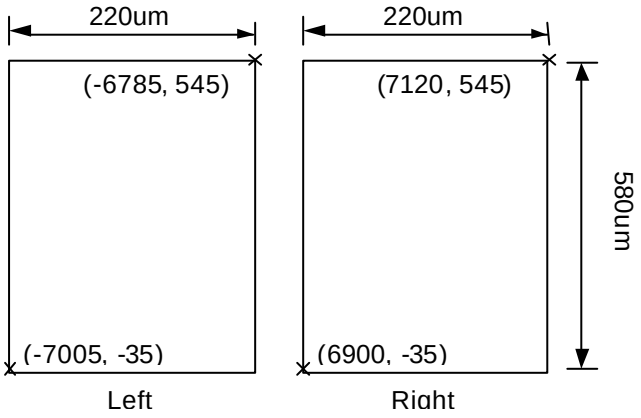


Figure 6. TOM Coordinate

PIN CONFIGURATION

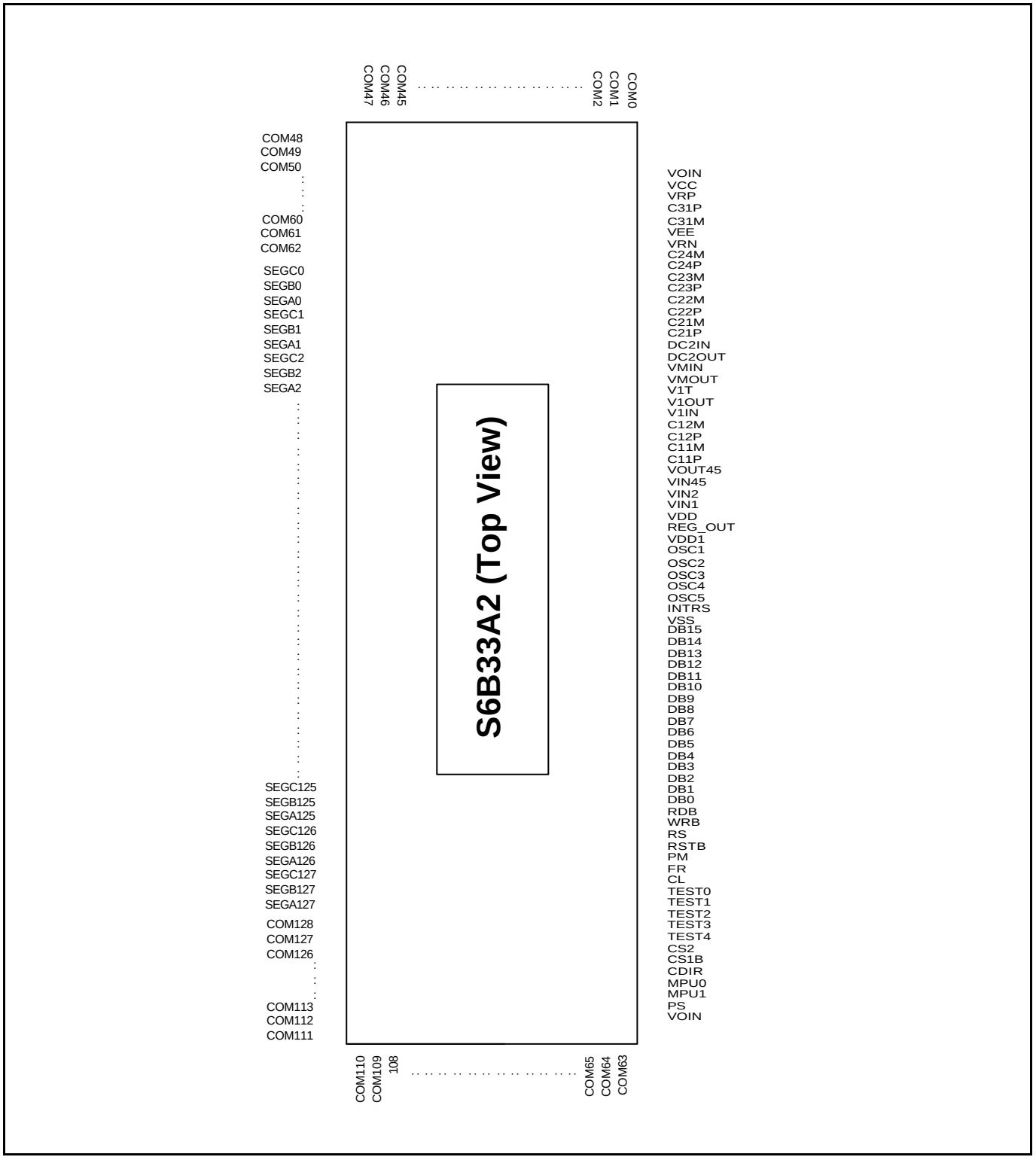


Figure 7. S6B33A2 Chip Pin Configuration

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	DUMMY	-7920	-1100	61	VSS	-2520	-1100	121	V1OUT	2880	-1100	181	COM<1>	8165	-955
2	DUMMY	-7830	-1100	62	VSS	-2430	-1100	122	V1OUT	2970	-1100	182	COM<2>	8165	-917
3	V0IN	-7740	-1100	63	VSS	-2340	-1100	123	V1T	3060	-1100	183	COM<3>	8165	-879
4	V0IN	-7650	-1100	64	VDD	-2250	-1100	124	VMOUT	3150	-1100	184	COM<4>	8165	-841
5	VSS	-7560	-1100	65	INTRS	-2160	-1100	125	VMOUT	3240	-1100	185	COM<5>	8165	-803
6	PS	-7470	-1100	66	OSC5	-2070	-1100	126	VMOUT	3330	-1100	186	COM<6>	8165	-765
7	VDD	-7380	-1100	67	VSS	-1980	-1100	127	VMIN	3420	-1100	187	COM<7>	8165	-727
8	MPU<1>	-7290	-1100	68	OSC4	-1890	-1100	128	VMIN	3510	-1100	188	COM<8>	8165	-689
9	VSS	-7200	-1100	69	OSC3	-1800	-1100	129	VMIN	3600	-1100	189	COM<9>	8165	-651
10	MPU<0>	-7110	-1100	70	OSC2	-1710	-1100	130	DC2OUT	3690	-1100	190	COM<10>	8165	-613
11	VDD	-7020	-1100	71	OSC1	-1620	-1100	131	DC2OUT	3780	-1100	191	COM<11>	8165	-575
12	CDIR	-6930	-1100	72	VDD1	-1530	-1100	132	DC2IN	3870	-1100	192	COM<12>	8165	-537
13	VSS	-6840	-1100	73	VDD1	-1440	-1100	133	DC2IN	3960	-1100	193	COM<13>	8165	-499
14	CS1B	-6750	-1100	74	VDD1	-1350	-1100	134	C21P	4050	-1100	194	COM<14>	8165	-461
15	CS2	-6660	-1100	75	VDD1	-1260	-1100	135	C21P	4140	-1100	195	COM<15>	8165	-423
16	TEST<4>	-6570	-1100	76	VDD1	-1170	-1100	136	C21P	4230	-1100	196	COM<16>	8165	-385
17	TEST<3>	-6480	-1100	77	VDD1	-1080	-1100	137	C21M	4320	-1100	197	COM<17>	8165	-347
18	TEST<2>	-6390	-1100	78	REG_OUT	-990	-1100	138	C21M	4410	-1100	198	COM<18>	8165	-309
19	TEST<1>	-6300	-1100	79	REG_OUT	-900	-1100	139	C21M	4500	-1100	199	COM<19>	8165	-271
20	TEST<0>	-6210	-1100	80	REG_OUT	-810	-1100	140	C22P	4590	-1100	200	COM<20>	8165	-233
21	VDD	-6120	-1100	81	VDD	-720	-1100	141	C22P	4680	-1100	201	COM<21>	8165	-195
22	CL	-6030	-1100	82	VDD	-630	-1100	142	C22P	4770	-1100	202	COM<22>	8165	-157
23	FR	-5940	-1100	83	VDD	-540	-1100	143	C22M	4860	-1100	203	COM<23>	8165	-119
24	PM	-5850	-1100	84	VDD	-450	-1100	144	C22M	4950	-1100	204	COM<24>	8165	-81
25	RSTB	-5760	-1100	85	VDD	-360	-1100	145	C22M	5040	-1100	205	COM<25>	8165	-43
26	RS	-5670	-1100	86	VDD	-270	-1100	146	C23P	5130	-1100	206	COM<26>	8165	-5
27	VSS	-5580	-1100	87	VDD	-180	-1100	147	C23P	5220	-1100	207	COM<27>	8165	33
28	WRB	-5490	-1100	88	VIN1	-90	-1100	148	C23P	5310	-1100	208	COM<28>	8165	71
29	RDB	-5400	-1100	89	VIN1	0	-1100	149	C23M	5400	-1100	209	COM<29>	8165	109
30	VDD	-5310	-1100	90	VIN1	90	-1100	150	C23M	5490	-1100	210	COM<30>	8165	147
31	DB<0>	-5220	-1100	91	VIN1	180	-1100	151	C23M	5580	-1100	211	COM<31>	8165	185
32	DB<1>	-5130	-1100	92	VIN1	270	-1100	152	VRN	5670	-1100	212	COM<32>	8165	223
33	DB<2>	-5040	-1100	93	VIN1	360	-1100	153	VRN	5760	-1100	213	COM<33>	8165	261
34	DB<3>	-4950	-1100	94	VIN1	450	-1100	154	VRN	5850	-1100	214	COM<34>	8165	299
35	DB<4>	-4860	-1100	95	VIN1	540	-1100	155	VEE	5940	-1100	215	COM<35>	8165	337
36	DB<5>	-4770	-1100	96	VIN1	630	-1100	156	VEE	6030	-1100	216	COM<36>	8165	375
37	DB<6>	-4680	-1100	97	VIN1	720	-1100	157	VEE	6120	-1100	217	COM<37>	8165	413
38	DB<7>	-4590	-1100	98	VIN1	810	-1100	158	VEE	6210	-1100	218	COM<38>	8165	451
39	DB<8>	-4500	-1100	99	VIN2	900	-1100	159	DUMMY	6300	-1100	219	COM<39>	8165	489
40	DB<9>	-4410	-1100	100	VIN2	990	-1100	160	C31M	6390	-1100	220	COM<40>	8165	527
41	DB<10>	-4320	-1100	101	VIN2	1080	-1100	161	C31M	6480	-1100	221	COM<41>	8165	565
42	DB<11>	-4230	-1100	102	VIN2	1170	-1100	162	C31M	6570	-1100	222	COM<42>	8165	603
43	DB<12>	-4140	-1100	103	VIN45	1260	-1100	163	DUMMY	6660	-1100	223	COM<43>	8165	641
44	DB<13>	-4050	-1100	104	VIN45	1350	-1100	164	C31P	6750	-1100	224	COM<44>	8165	679
45	DB<14>	-3960	-1100	105	VOUT45	1440	-1100	165	C31P	6840	-1100	225	COM<45>	8165	717
46	DB<15>	-3870	-1100	106	VOUT45	1530	-1100	166	C31P	6930	-1100	226	COM<46>	8165	755
47	VSS	-3780	-1100	107	C11P	1620	-1100	167	DUMMY	7020	-1100	227	COM<47>	8165	793
48	VSS	-3690	-1100	108	C11P	1710	-1100	168	VRP	7110	-1100	228	DUMMY	8165	831
49	VSS	-3600	-1100	109	C11P	1800	-1100	169	VRP	7200	-1100	229	DUMMY	8165	869
50	VSS	-3510	-1100	110	C11M	1890	-1100	170	VCC	7290	-1100	230	DUMMY	8018	1045
51	VSS	-3420	-1100	111	C11M	1980	-1100	171	VCC	7380	-1100	231	DUMMY	7980	1045
52	VSS	-3330	-1100	112	C11M	2070	-1100	172	DUMMY	7470	-1100	232	COM<48>	7942	1045
53	VSS	-3240	-1100	113	C12P	2160	-1100	173	VSS	7560	-1100	233	COM<49>	7904	1045
54	VSS	-3150	-1100	114	C12P	2250	-1100	174	V0IN	7650	-1100	234	COM<50>	7866	1045
55	VSS	-3060	-1100	115	C12P	2340	-1100	175	V0IN	7740	-1100	235	COM<51>	7828	1045
56	VSS	-2970	-1100	116	C12M	2430	-1100	176	DUMMY	7830	-1100	236	COM<52>	7790	1045
57	VSS	-2880	-1100	117	C12M	2520	-1100	177	DUMMY	7920	-1100	237	COM<53>	7752	1045
58	VSS	-2790	-1100	118	C12M	2610	-1100	178	DUMMY	8165	-1069	238	COM<54>	7714	1045
59	VSS	-2700	-1100	119	V1IN	2700	-1100	179	DUMMY	8165	-1031	239	COM<55>	7676	1045
60	VSS	-2610	-1100	120	V1IN	2790	-1100	180	COM<0>	8165	-993	240	COM<56>	7638	1045

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
241	COM<57>	7600	1045	301	SEGA<17>	5320	1045	361	SEGA<37>	3040	1045	421	SEGA<57>	760	1045
242	COM<58>	7562	1045	302	SEGC<18>	5282	1045	362	SEGC<38>	3002	1045	422	SEGC<58>	722	1045
243	COM<59>	7524	1045	303	SEGB<18>	5244	1045	363	SEGB<38>	2964	1045	423	SEGB<58>	684	1045
244	COM<60>	7486	1045	304	SEGA<18>	5206	1045	364	SEGA<38>	2926	1045	424	SEGA<58>	646	1045
245	COM<61>	7448	1045	305	SEGC<19>	5168	1045	365	SEGC<39>	2888	1045	425	SEGC<59>	608	1045
246	COM<62>	7410	1045	306	SEGB<19>	5130	1045	366	SEGB<39>	2850	1045	426	SEGB<59>	570	1045
247	DUMMY	7372	1045	307	SEGA<19>	5092	1045	367	SEGA<39>	2812	1045	427	SEGA<59>	532	1045
248	SEGC<0>	7334	1045	308	SEGC<20>	5054	1045	368	SEGC<40>	2774	1045	428	SEGC<60>	494	1045
249	SEGB<0>	7296	1045	309	SEGB<20>	5016	1045	369	SEGB<40>	2736	1045	429	SEGB<60>	456	1045
250	SEGA<0>	7258	1045	310	SEGA<20>	4978	1045	370	SEGA<40>	2698	1045	430	SEGA<60>	418	1045
251	SEGC<1>	7220	1045	311	SEGC<21>	4940	1045	371	SEGC<41>	2660	1045	431	SEGC<61>	380	1045
252	SEGB<1>	7182	1045	312	SEGB<21>	4902	1045	372	SEGB<41>	2622	1045	432	SEGB<61>	342	1045
253	SEGA<1>	7144	1045	313	SEGA<21>	4864	1045	373	SEGA<41>	2584	1045	433	SEGA<61>	304	1045
254	SEGC<2>	7106	1045	314	SEGC<22>	4826	1045	374	SEGC<42>	2546	1045	434	SEGC<62>	266	1045
255	SEGB<2>	7068	1045	315	SEGB<22>	4788	1045	375	SEGB<42>	2508	1045	435	SEGB<62>	228	1045
256	SEGA<2>	7030	1045	316	SEGA<22>	4750	1045	376	SEGA<42>	2470	1045	436	SEGA<62>	190	1045
257	SEGC<3>	6992	1045	317	SEGC<23>	4712	1045	377	SEGC<43>	2432	1045	437	SEGC<63>	152	1045
258	SEGB<3>	6954	1045	318	SEGB<23>	4674	1045	378	SEGB<43>	2394	1045	438	SEGB<63>	114	1045
259	SEGA<3>	6916	1045	319	SEGA<23>	4636	1045	379	SEGA<43>	2356	1045	439	SEGA<63>	76	1045
260	SEGC<4>	6878	1045	320	SEGC<24>	4598	1045	380	SEGC<44>	2318	1045	440	SEGC<64>	38	1045
261	SEGB<4>	6840	1045	321	SEGB<24>	4560	1045	381	SEGB<44>	2280	1045	441	SEGB<64>	0	1045
262	SEGA<4>	6802	1045	322	SEGA<24>	4522	1045	382	SEGA<44>	2242	1045	442	SEGA<64>	-38	1045
263	SEGC<5>	6764	1045	323	SEGC<25>	4484	1045	383	SEGC<45>	2204	1045	443	SEGC<65>	-76	1045
264	SEGB<5>	6726	1045	324	SEGB<25>	4446	1045	384	SEGB<45>	2166	1045	444	SEGB<65>	-114	1045
265	SEGA<5>	6688	1045	325	SEGA<25>	4408	1045	385	SEGA<45>	2128	1045	445	SEGA<65>	-152	1045
266	SEGC<6>	6650	1045	326	SEGC<26>	4370	1045	386	SEGC<46>	2090	1045	446	SEGC<66>	-190	1045
267	SEGB<6>	6612	1045	327	SEGB<26>	4332	1045	387	SEGB<46>	2052	1045	447	SEGB<66>	-228	1045
268	SEGA<6>	6574	1045	328	SEGA<26>	4294	1045	388	SEGA<46>	2014	1045	448	SEGA<66>	-266	1045
269	SEGC<7>	6536	1045	329	SEGC<27>	4256	1045	389	SEGC<47>	1976	1045	449	SEGC<67>	-304	1045
270	SEGB<7>	6498	1045	330	SEGB<27>	4218	1045	390	SEGB<47>	1938	1045	450	SEGB<67>	-342	1045
271	SEGA<7>	6460	1045	331	SEGA<27>	4180	1045	391	SEGA<47>	1900	1045	451	SEGA<67>	-380	1045
272	SEGC<8>	6422	1045	332	SEGC<28>	4142	1045	392	SEGC<48>	1862	1045	452	SEGC<68>	-418	1045
273	SEGB<8>	6384	1045	333	SEGB<28>	4104	1045	393	SEGB<48>	1824	1045	453	SEGB<68>	-456	1045
274	SEGA<8>	6346	1045	334	SEGA<28>	4066	1045	394	SEGA<48>	1786	1045	454	SEGA<68>	-494	1045
275	SEGC<9>	6308	1045	335	SEGC<29>	4028	1045	395	SEGC<49>	1748	1045	455	SEGC<69>	-532	1045
276	SEGB<9>	6270	1045	336	SEGB<29>	3990	1045	396	SEGB<49>	1710	1045	456	SEGB<69>	-570	1045
277	SEGA<9>	6232	1045	337	SEGA<29>	3952	1045	397	SEGA<49>	1672	1045	457	SEGA<69>	-608	1045
278	SEGC<10>	6194	1045	338	SEGC<30>	3914	1045	398	SEGC<50>	1634	1045	458	SEGC<70>	-646	1045
279	SEGB<10>	6156	1045	339	SEGB<30>	3876	1045	399	SEGB<50>	1596	1045	459	SEGB<70>	-684	1045
280	SEGA<10>	6118	1045	340	SEGA<30>	3838	1045	400	SEGA<50>	1558	1045	460	SEGA<70>	-722	1045
281	SEGC<11>	6080	1045	341	SEGC<31>	3800	1045	401	SEGC<51>	1520	1045	461	SEGC<71>	-760	1045
282	SEGB<11>	6042	1045	342	SEGB<31>	3762	1045	402	SEGB<51>	1482	1045	462	SEGB<71>	-798	1045
283	SEGA<11>	6004	1045	343	SEGA<31>	3724	1045	403	SEGA<51>	1444	1045	463	SEGA<71>	-836	1045
284	SEGC<12>	5966	1045	344	SEGC<32>	3686	1045	404	SEGC<52>	1406	1045	464	SEGC<72>	-874	1045
285	SEGB<12>	5928	1045	345	SEGB<32>	3648	1045	405	SEGB<52>	1368	1045	465	SEGB<72>	-912	1045
286	SEGA<12>	5890	1045	346	SEGA<32>	3610	1045	406	SEGA<52>	1330	1045	466	SEGA<72>	-950	1045
287	SEGC<13>	5852	1045	347	SEGC<33>	3572	1045	407	SEGC<53>	1292	1045	467	SEGC<73>	-988	1045
288	SEGB<13>	5814	1045	348	SEGB<33>	3534	1045	408	SEGB<53>	1254	1045	468	SEGB<73>	-1026	1045
289	SEGA<13>	5776	1045	349	SEGA<33>	3496	1045	409	SEGA<53>	1216	1045	469	SEGA<73>	-1064	1045
290	SEGC<14>	5738	1045	350	SEGC<34>	3458	1045	410	SEGC<54>	1178	1045	470	SEGC<74>	-1102	1045
291	SEGB<14>	5700	1045	351	SEGB<34>	3420	1045	411	SEGB<54>	1140	1045	471	SEGB<74>	-1140	1045
292	SEGA<14>	5662	1045	352	SEGA<34>	3382	1045	412	SEGA<54>	1102	1045	472	SEGA<74>	-1178	1045
293	SEGC<15>	5624	1045	353	SEGC<35>	3344	1045	413	SEGC<55>	1064	1045	473	SEGC<75>	-1216	1045
294	SEGB<15>	5586	1045	354	SEGB<35>	3306	1045	414	SEGB<55>	1026	1045	474	SEGB<75>	-1254	1045
295	SEGA<15>	5548	1045	355	SEGA<35>	3268	1045	415	SEGA<55>	988	1045	475	SEGA<75>	-1292	1045
296	SEGC<16>	5510	1045	356	SEGC<36>	3230	1045	416	SEGC<56>	950	1045	476	SEGC<76>	-1330	1045
297	SEGB<16>	5472	1045	357	SEGB<36>	3192	1045	417	SEGB<56>	912	1045	477	SEGB<76>	-1368	1045
298	SEGA<16>	5434	1045	358	SEGA<36>	3154	1045	418	SEGA<56>	874	1045	478	SEGA<76>	-1406	1045
299	SEGC<17>	5396	1045	359	SEGC<37>	3116	1045	419	SEGC<57>	836	1045	479	SEGC<77>	-1444	1045
300	SEGB<17>	5358	1045	360	SEGB<37>	3078	1045	420	SEGB<57>	798	1045	480	SEGB<77>	-1482	1045

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y
481	SEGA<77>	-1520	1045
482	SEGC<78>	-1558	1045
483	SEGB<78>	-1596	1045
484	SEGA<78>	-1634	1045
485	SEGC<79>	-1672	1045
486	SEGB<79>	-1710	1045
487	SEGA<79>	-1748	1045
488	SEGC<80>	-1786	1045
489	SEGB<80>	-1824	1045
490	SEGA<80>	-1862	1045
491	SEGC<81>	-1900	1045
492	SEGB<81>	-1938	1045
493	SEGA<81>	-1976	1045
494	SEGC<82>	-2014	1045
495	SEGB<82>	-2052	1045
496	SEGA<82>	-2090	1045
497	SEGC<83>	-2128	1045
498	SEGB<83>	-2166	1045
499	SEGA<83>	-2204	1045
500	SEGC<84>	-2242	1045
501	SEGB<84>	-2280	1045
502	SEGA<84>	-2318	1045
503	SEGC<85>	-2356	1045
504	SEGB<85>	-2394	1045
505	SEGA<85>	-2432	1045
506	SEGC<86>	-2470	1045
507	SEGB<86>	-2508	1045
508	SEGA<86>	-2546	1045
509	SEGC<87>	-2584	1045
510	SEGB<87>	-2622	1045
511	SEGA<87>	-2660	1045
512	SEGC<88>	-2698	1045
513	SEGB<88>	-2736	1045
514	SEGA<88>	-2774	1045
515	SEGC<89>	-2812	1045
516	SEGB<89>	-2850	1045
517	SEGA<89>	-2888	1045
518	SEGC<90>	-2926	1045
519	SEGB<90>	-2964	1045
520	SEGA<90>	-3002	1045
521	SEGC<91>	-3040	1045
522	SEGB<91>	-3078	1045
523	SEGA<91>	-3116	1045
524	SEGC<92>	-3154	1045
525	SEGB<92>	-3192	1045
526	SEGA<92>	-3230	1045
527	SEGC<93>	-3268	1045
528	SEGB<93>	-3306	1045
529	SEGA<93>	-3344	1045
530	SEGC<94>	-3382	1045
531	SEGB<94>	-3420	1045
532	SEGA<94>	-3458	1045
533	SEGC<95>	-3496	1045
534	SEGB<95>	-3534	1045
535	SEGA<95>	-3572	1045
536	SEGC<96>	-3610	1045
537	SEGB<96>	-3648	1045
538	SEGA<96>	-3686	1045
539	SEGC<97>	-3724	1045
540	SEGB<97>	-3762	1045
541	SEGA<97>	-3800	1045
542	SEGC<98>	-3838	1045
543	SEGB<98>	-3876	1045
544	SEGA<98>	-3914	1045
545	SEGC<99>	-3952	1045
546	SEGB<99>	-3990	1045
547	SEGA<99>	-4028	1045
548	SEGC<100>	-4066	1045
549	SEGB<100>	-4104	1045
550	SEGA<100>	-4142	1045
551	SEGC<101>	-4180	1045
552	SEGB<101>	-4218	1045
553	SEGA<101>	-4256	1045
554	SEGC<102>	-4294	1045
555	SEGB<102>	-4332	1045
556	SEGA<102>	-4370	1045
557	SEGC<103>	-4408	1045
558	SEGB<103>	-4446	1045
559	SEGA<103>	-4484	1045
560	SEGC<104>	-4522	1045
561	SEGB<104>	-4560	1045
562	SEGA<104>	-4598	1045
563	SEGC<105>	-4636	1045
564	SEGB<105>	-4674	1045
565	SEGA<105>	-4712	1045
566	SEGC<106>	-4750	1045
567	SEGB<106>	-4788	1045
568	SEGA<106>	-4826	1045
569	SEGC<107>	-4864	1045
570	SEGB<107>	-4902	1045
571	SEGA<107>	-4940	1045
572	SEGC<108>	-4978	1045
573	SEGB<108>	-5016	1045
574	SEGA<108>	-5054	1045
575	SEGC<109>	-5092	1045
576	SEGB<109>	-5130	1045
577	SEGA<109>	-5168	1045
578	SEGC<110>	-5206	1045
579	SEGB<110>	-5244	1045
580	SEGA<110>	-5282	1045
581	SEGC<111>	-5320	1045
582	SEGB<111>	-5358	1045
583	SEGA<111>	-5396	1045
584	SEGC<112>	-5434	1045
585	SEGB<112>	-5472	1045
586	SEGA<112>	-5510	1045
587	SEGC<113>	-5548	1045
588	SEGB<113>	-5586	1045
589	SEGA<113>	-5624	1045
590	SEGC<114>	-5662	1045
591	SEGB<114>	-5700	1045
592	SEGA<114>	-5738	1045
593	SEGC<115>	-5776	1045
594	SEGB<115>	-5814	1045
595	SEGA<115>	-5852	1045
596	SEGC<116>	-5890	1045
597	SEGB<116>	-5928	1045
598	SEGA<116>	-5966	1045
599	SEGC<117>	-6004	1045
600	SEGB<117>	-6042	1045
601	SEGA<117>	-6080	1045
602	SEGC<118>	-6118	1045
603	SEGB<118>	-6156	1045
604	SEGA<118>	-6194	1045
605	SEGC<119>	-6232	1045
606	SEGB<119>	-6270	1045
607	SEGA<119>	-6308	1045
608	SEGC<120>	-6346	1045
609	SEGB<120>	-6384	1045
610	SEGA<120>	-6422	1045
611	SEGC<121>	-6460	1045
612	SEGB<121>	-6498	1045
613	SEGA<121>	-6536	1045
614	SEGC<122>	-6574	1045
615	SEGB<122>	-6612	1045
616	SEGA<122>	-6650	1045
617	SEGC<123>	-6688	1045
618	SEGB<123>	-6726	1045
619	SEGA<123>	-6764	1045
620	SEGC<124>	-6802	1045
621	SEGB<124>	-6840	1045
622	SEGA<124>	-6878	1045
623	SEGC<125>	-6916	1045
624	SEGB<125>	-6954	1045
625	SEGA<125>	-6992	1045
626	SEGC<126>	-7030	1045
627	SEGB<126>	-7068	1045
628	SEGA<126>	-7106	1045
629	SEGC<127>	-7144	1045
630	SEGB<127>	-7182	1045
631	SEGA<127>	-7220	1045
632	DUMMY	-7258	1045
633	COM<128>	-7296	1045
634	COM<127>	-7334	1045
635	COM<126>	-7372	1045
636	COM<125>	-7410	1045
637	COM<124>	-7448	1045
638	COM<123>	-7486	1045
639	COM<122>	-7524	1045
640	COM<121>	-7562	1045
641	COM<120>	-7600	1045
642	COM<119>	-7638	1045
643	COM<118>	-7676	1045
644	COM<117>	-7714	1045
645	COM<116>	-7752	1045
646	COM<115>	-7790	1045
647	COM<114>	-7828	1045
648	COM<113>	-7866	1045
649	COM<112>	-7904	1045
650	COM<111>	-7942	1045
651	DUMMY	-7980	1045
652	DUMMY	-8018	1045
653	DUMMY	-8165	869
654	DUMMY	-8165	831
655	COM<110>	-8165	793
656	COM<109>	-8165	755
657	COM<108>	-8165	717
658	COM<107>	-8165	679
659	COM<106>	-8165	641
660	COM<105>	-8165	603
661	COM<104>	-8165	565
662	COM<103>	-8165	527
663	COM<102>	-8165	489
664	COM<101>	-8165	451
665	COM<100>	-8165	413
666	COM<99>	-8165	375
667	COM<98>	-8165	337
668	COM<97>	-8165	299
669	COM<96>	-8165	261
670	COM<95>	-8165	223
671	COM<94>	-8165	185
672	COM<93>	-8165	147
673	COM<92>	-8165	109
674	COM<91>	-8165	71
675	COM<90>	-8165	33
676	COM<89>	-8165	-5
677	COM<88>	-8165	-43
678	COM<87>	-8165	-81
679	COM<86>	-8165	-119
680	COM<85>	-8165	-157
681	COM<84>	-8165	-195
682	COM<83>	-8165	-233
683	COM<82>	-8165	-271
684	COM<81>	-8165	-309
685	COM<80>	-8165	-347
686	COM<79>	-8165	-385
687	COM<78>	-8165	-423
688	COM<77>	-8165	-461
689	COM<76>	-8165	-499
690	COM<75>	-8165	-537
691	COM<74>	-8165	-575
692	COM<73>	-8165	-613
693	COM<72>	-8165	-651
694	COM<71>	-8165	-689
695	COM<70>	-8165	-727
696	COM<69>	-8165	-765
697	COM<68>	-8165	-803
698	COM<67>	-8165	-841
699	COM<66>	-8165	-879
700	COM<65>	-8165	-917
701	COM<64>	-8165	-955
702	COM<63>	-8165	-993
703	DUMMY	-8165	-1031
704	DUMMY	-8165	-1069

PIN DESCRIPTION

Table 3. Power Supply Pins

Name	I/O	Description
VDD	Supply	Power supply(Logic)
VDD3R	Supply	Internal regulator power supply This pin is connected to VDD.
VDD1	Supply	Regulated power supply input pin for internal digital and DDRAM block. This pin is connected to REG_OUT outside the chip with stabilization capacitor. When the internal regulator is not used, VDD1 should be tied to VDD directly.
VSS,VSSA VSSB,VSSO	GND	Ground
VCC	I	LCD common high selected driving voltage input pin
V1IN	I	LCD segment high selected driving voltage input pin
VMIN	I	LCD common/segment non-selected driving voltage input pin
V0IN	I	LCD segment low selected driving voltage input pin
VEE,VEES	I	LCD common low selected driving voltage input pin The relationship between VCC, V1, VM, V0 and VEE: VCC > V1 > VM > V0(=VSS) > VEE (V1 – VM = VM – V0, VCC –VM = VM – VEE)
VIN1,VIN1A	I	Power supply for 1’ st booster circuit and VM amp
VIN2	I	Power supply for 2’ nd booster circuit
VOUT45	O	1’ st booster output pin
VIN45	I	Power supply for V1. Connect to VOUT45 or VIN1
C11+ C11- C12+ C12-	O	External capacitor connection pins used for 1’ st booster circuit
V1OUT	O	LCD segment high driving voltage output pin
V1T	I	Thermistor resistor connection pin
INTRS	I	External resister select pin for temperature compensation circuit – INTRS = L : External resistor mode, INTRS = H : Internal resistor mode
VMOUT	O	LCD common/segment non-selected driving voltage output pin
DC2OUT	O	Power output pin for 2’ nd booster input
DC2IN	I	Power supply for 2’ nd booster. Connect to DC2OUT pin
C21+ C21- C22+ C22- C23+ C23-	O	External capacitor connection pins used for 2’ nd booster circuit
-VR	O	LCD common low selected driving voltage output pin
C31+ C31-	O	External capacitor connection pins used for 3’ rd booster circuit
+VR	O	LCD common high selected driving voltage output pin

Table 4. MPU Interface Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>/RST</td><td>I</td><td>Reset input pin.
When /RST is “L”, initialization is executed.</td></tr>
<tr><td>PS
MPU[1:0]</td><td>I</td><td>MPU interface select pin
<table>
<tr><th>PS</th><th>MPU[1]</th><th>MPU[0]</th><th>Description</th></tr>
<tr><td>H</td><td>L</td><td>L</td><td>8080-series 8bit interface</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>8080-series 16bit interface</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>6800-series 8bit interface</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>6800-series 16bit interface</td></tr>
<tr><td>L</td><td>L</td><td>X</td><td>3 pin SPI(Write only)</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>4 pin SPI(Write only)</td></tr>
</table></td></tr>
<tr><td>/CS1
CS2</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when /CS1 is “L” and CS2 is “H”. When chip select is non-active, DB0 to DB15 may be high impedance.</td></tr>
<tr><td>D/I</td><td>I</td><td>Data / Instruction select input pin
– D/I = “H”: DB0 to DB15 are display data
– D/I = “L”: DB0 to DB7 are instruction data</td></tr>
<tr><td>/WR
(R/W)</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>PS</th><th>MPU</th><th>MPU Type</th><th>/WR</th><th>Description</th></tr>
<tr><td>H</td><td>H</td><td>6800-series</td><td>R/W</td><td>Read/Write control input pin
– R/W = “H”: read
– R/W = “L”: write</td></tr>
<tr><td>H</td><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB15 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td>/RD
(E)</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU[1]</th><th>MPU type</th><th>/RD</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– R/W = “H”: When E is “H”, DB0 to DB15 are in an output status.
– R/W = “L”: The data on DB0 to DB15 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB15 are in an output status.</td></tr>
</table></td></tr>
<tr><td>DB[15:8]
DB[7]/SDI
DB[6]/SCL
DB[5:0]</td><td>I/O</td><td>-DB[15:0]: 16-bit bi-directional data bus.
-SDI: Serial data input pin. The data is latched at the rising edge of SCL.
-SCL: Serial clock input pin.</td></tr>
<tr><td>CDIR</td><td>I</td><td>Common direction select pin.</td></tr>
</table>

Table 5. Oscillator and Power Regulator Pins

Name	I/O	Description
OSC1 OSC2 OSC3 OSC4	O	CR oscillator output pin When the internal CR oscillator is used, connect to OSC1, OSC3 through a resistor. OSC1 – OSC2: Using in normal display mode, partial display mode 0 OSC3 – OSC4: Using in partial display mode 1 When an external oscillator is used, OSC1 pin is connected to VDD or VSS.
OSC5	I	External clock input pin When an external input is used, it is input to this pin. But the internal oscillator is used, this pin is connected to VDD or VSS.
REG_OUT	O	Internal voltage regulator output pin The regulator output port from this pin is used as a power supplier for an internal digital block via VDD1 pins.

Table 6. Timing signal Pins for monitoring

Name	I/O	Description
CL	O	Shift clock output pin
PM	O	Field delimiter output pin
FR	O	Liquid crystal alternating current output pin

Table 7. LCD driver output pins

Name	I/O	Description
SEGA0 to 127	O	LCD driving segment output (Red or Blue)
SEGB0 to 127	O	LCD driving segment output (Green)
SEGC0 to127	O	LCD driving segment output (Blue or Red)
COM0 to 128	O	LCD common outputs

Table 8. Test pins

Name	I/O	Description
TEST [4:0]	I	Don’ t use these pins. IC maker’ s test pins. Fix “ High” in normal mode.

FUNCTIONAL DESCRIPTION

MPU INTERFACE

Chip Select Input

There are /CS1 and CS2 pins for chip selection. The S6B33A2 can interface with an MPU only when /CS1 is "L" and CS2 is "H". When these pins are set to any other combination, D/I, /RD, and /WR inputs are disabled and DB0 to DB15 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel/Serial Interface

The S6B33A2 has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in Table9.

Table 9. Parallel / Serial Interface Mode.

PS	MPU[1]	/CS1	CS2	MPU bus type
H	L	/CS1	CS2	8080-Series MPU
	H			6800-Series MPU
L	L	/CS1	CS2	3–Pin SPI
	H			4-Pin SPI

Parallel Interface (PS="H")

The 8-bit/16-bit bi-directional data bus is used in parallel interface. The type of MPU is selected by MPU[1] and the mode of data-bus is controlled by MPU[0] as shown in below. In accessing internal registers (D/I = "L"), only DB[7:0] are valid.

Table 10. Microprocessor Selection for Parallel Int erface

MPU[1]	MPU[0]	/CS1	CS2	/RD	/WR	Data Bus	MPU bus type
L	L	/CS1	CS2	E	R/W	DB[7:0]	8080-series MPU
	H					DB[15:0]	
H	L	/CS1	CS2	/RD	/WR	DB[7:0]	6800-series MPU
	H					DB[15:0]	

Table 11. Parallel Data Transfer

D/I	6800-series		8080-series		Description
	/RD	/WR	/RD	/WR	
H	H	H	L	H	Read display data
H	H	L	H	L	Write display data
L	H	H	L	H	Read out internal status register
L	H	L	H	L	Write instruction data

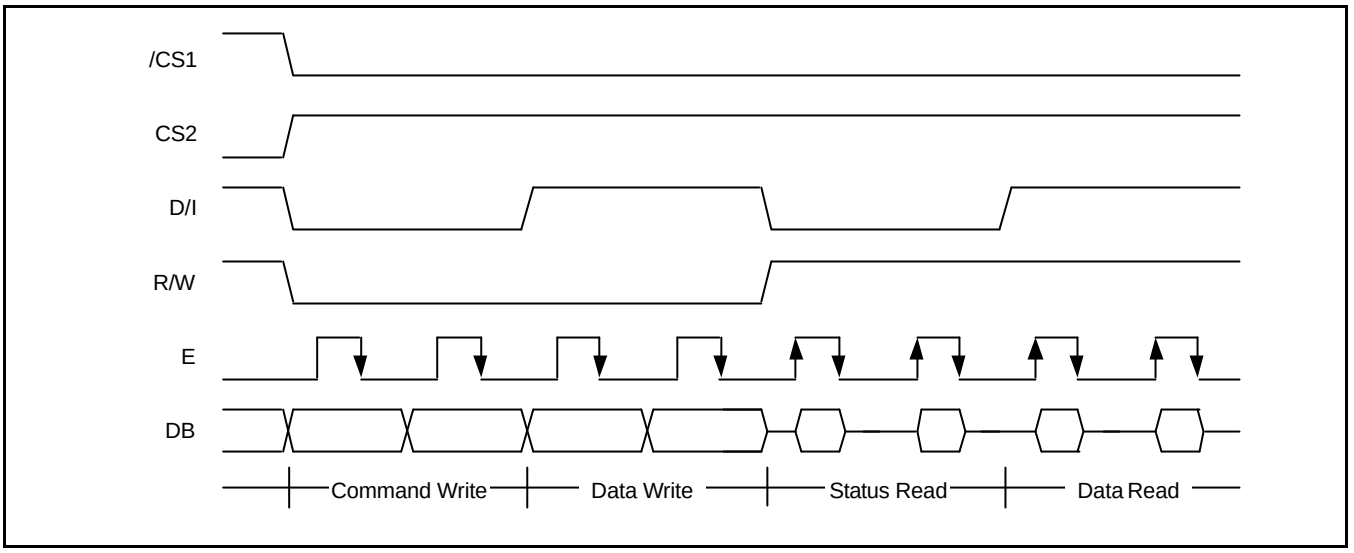


Figure 8. 6800-Series MPU Interface protocol (MPU[1]="H")

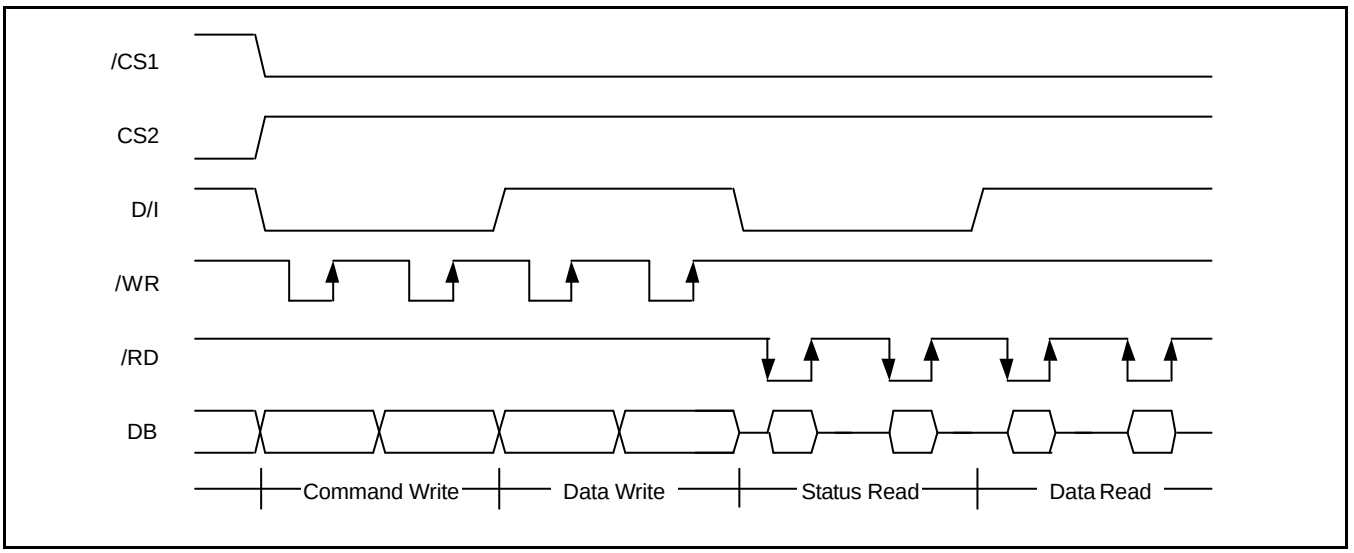


Figure 9. 8080-Series MPU Interface Protocol (MPU[1]="L")

Serial Interface(PS="L")

Communication with the microprocessor occurs via a clock-synchronized serial peripheral interface when PS is low. When using the serial interface, read operations are not allowed. When the chip select inputs are valid (/CS1 = "L" & CS2 = "H"), the serial data is sent most significant bit first on the rising edge of a serial clock going into DB6 and processed as 8 bit parallel data on the eighth clock. Since the clock signal is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended. And Invalid, the internal shift register and the counter are reset.

The serial interface type is selected by setting PS as shown in Table12.

Table 12. Microprocessor Selection for Serial Interface

PS	MPU[1]	/CS1	CS2	D/I	Serial Data	Serial Clock	SPI Mode
L	L	/CS1	CS2	D/I	DB[7]	DB[6]	3-Pin
	H	/CS1	CS2	S/W			4-Pin

3-Pin SPI Interface (PS = "L" & MPU[1] = "L")

In 3-Pin SPI Interface mode, the pre-defined instruction called Display Data Length is used to indicate whether serial data input is display or instruction data instead of D/I pin. The data is handled as instruction data until the Display Data Length instruction is issued. This Display Data Length instruction consists of three bytes instruction. The first byte instruction enables the next two instructions to be valid, and the data of the next two bytes indicate that a specified number of display data bytes(1 to 65536) are to be transmitted. For details, refer the Figure 8.

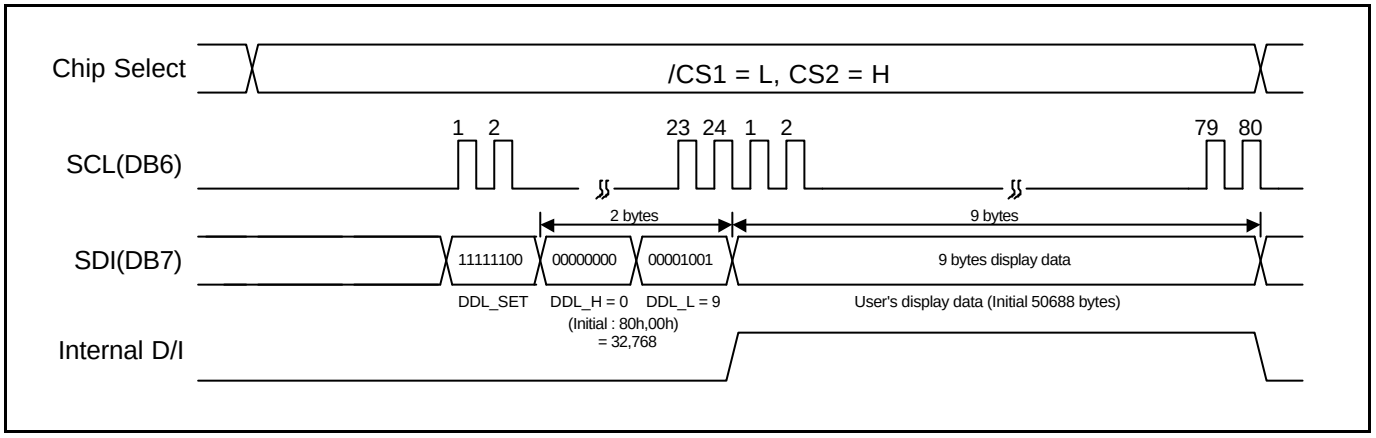


Figure 10. 3-Pin SPI Timing (D/I is not used)

4-Pin Serial Interface (PS="L" & MPU[1]="H")

In 4-pin SPI interface mode, D/I pin is used for indicating whether serial data input is display or instruction data. Data is display data when D/I is high and instruction data when D/I is low.
Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock.

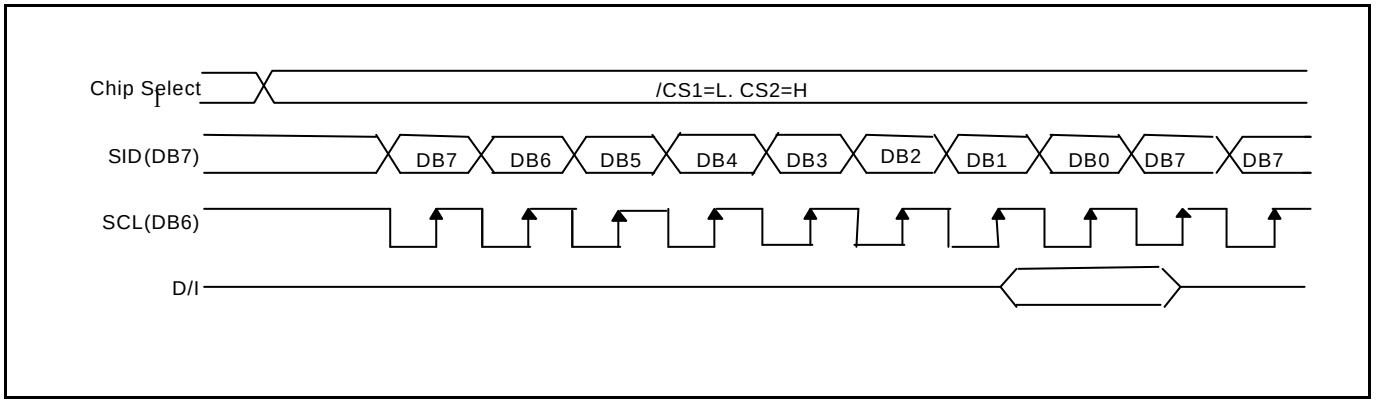


Figure 11. 4-Pin Serial Interface Timing

DISPLAY DATA RAM

The on-chip display data RAM of S6B33A2 is a static RAM that is stored the data for the display. It is a 1,536x 128 structure. It is controlled by 2 addresses, X and Y. And, RAM area selection and automatic address count up functions are accomplished by the internal instructions.

DDRAM Address Area Selection

A part of DDRAM address area of S6B33A2 can be accessed by X and Y address area settings. After setting RAM area, the addresses become the start address.

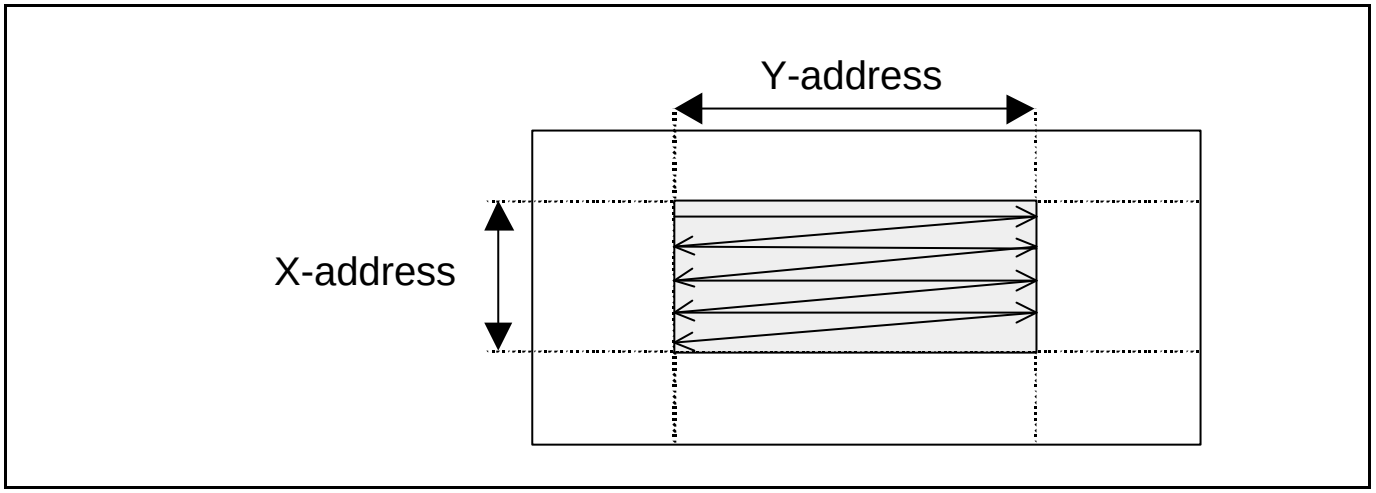


Figure 12. DDRAM Address Area

Table 13. X address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	0	0	1	0
P1	0	X start address set(Initial Status = 00H)						
P2		X end address set(Initial Status = 7FH)						

Table 14. Y address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	1	0	0	1	1
P1	0	Y start address set (Initial status = 00H)						
P2	0	Y end address set (Initial status =7FH)						

RAM Addressing Count up

By selecting the X address and Y address area by the internal instructions, the address counts up from its start address to end address after data access operation. When one address is equal to the end address, it returns to the start address. At this time, the other address is increased by 1.

Y address count mode (Y address = 00h to7Fh, X address = 00h to 7Fh, 16 bit access mode)

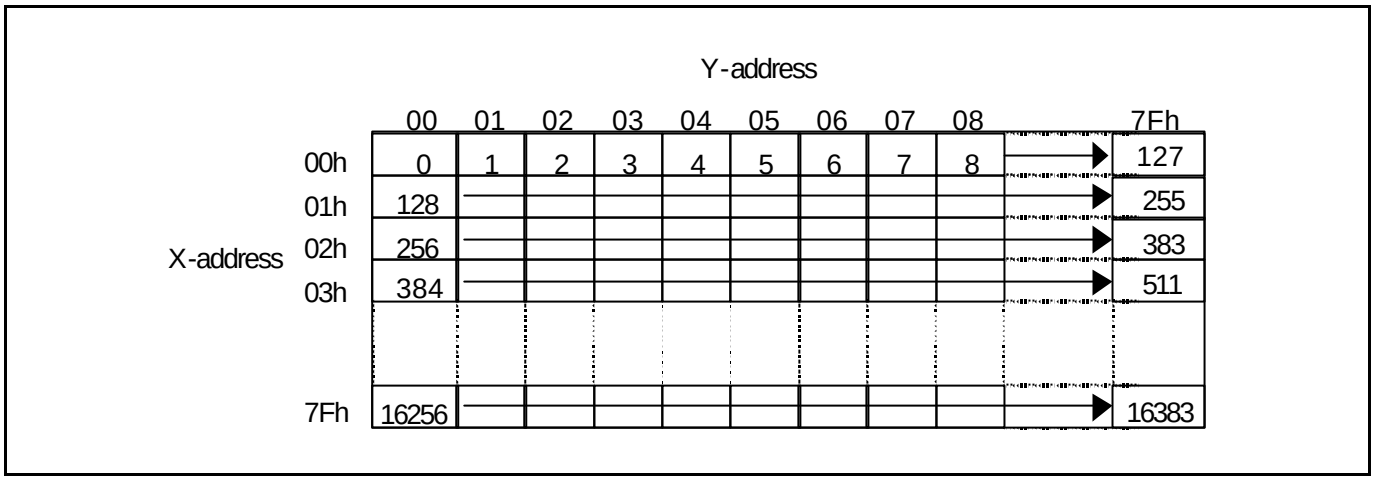


Figure 13. Y address count mode

X address count mode (Y address =00h to 7Fh, X address = 00h to 7Fh, 16 bit access mode)

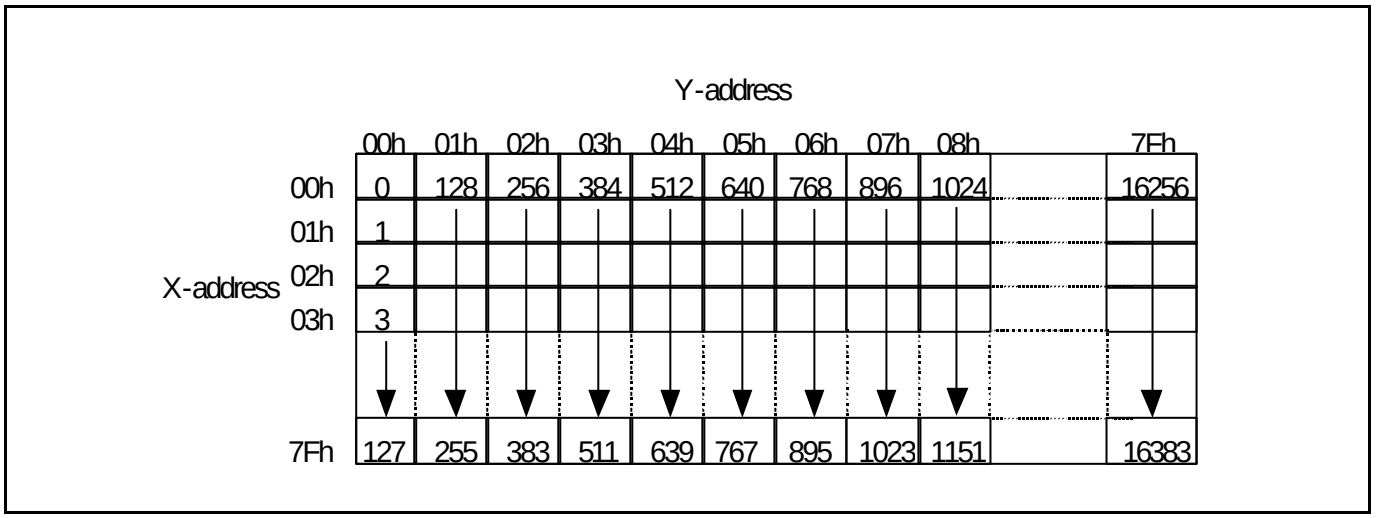


Figure 14. X address count mode

XA Address	YA Address																
	00H	01H	02H	03H	04H	05H	06H	07H	08H	- - - - - - -	79H	7AH	7BH	7CH	7DH	7EH	7FH
00H										- - - - - - -							
01H										- - - - - - -							
02H										- - - - - - -							
03H										- - - - - - -							
04H										- - - - - - -							
05H										- - - - - - -							
06H										- - - - - - -							
07H										- - - - - - -							
08H										- - - - - - -							
09H										- - - - - - -							
0AH										- - - - - - -							
0BH										- - - - - - -							
0CH										- - - - - - -							
0DH										- - - - - - -							
0EH										- - - - - - -							
0FH										- - - - - - -							
⋮										⋮							
70H										- - - - - - -							
71H										- - - - - - -							
72H										- - - - - - -							
73H										- - - - - - -							
74H										- - - - - - -							
75H										- - - - - - -							
76H										- - - - - - -							
77H										- - - - - - -							
78H										- - - - - - -							
79H										- - - - - - -							
7AH										- - - - - - -							
7BH										- - - - - - -							
7CH										- - - - - - -							
7DH										- - - - - - -							
7EH										- - - - - - -							
7FH										- - - - - - -							

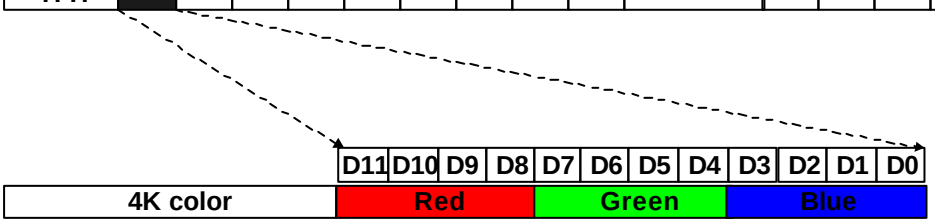


Figure 15. Display Data RAM Map

Partial Display Mode

The S6B33A2 realizes the partial display function with low duty driving for saving power consumption and showing the various display duties. It is set as display start/end line number.

Area Scroll Function

The S6B33A2 realizes the specific area scroll function. (1/128 duty case).

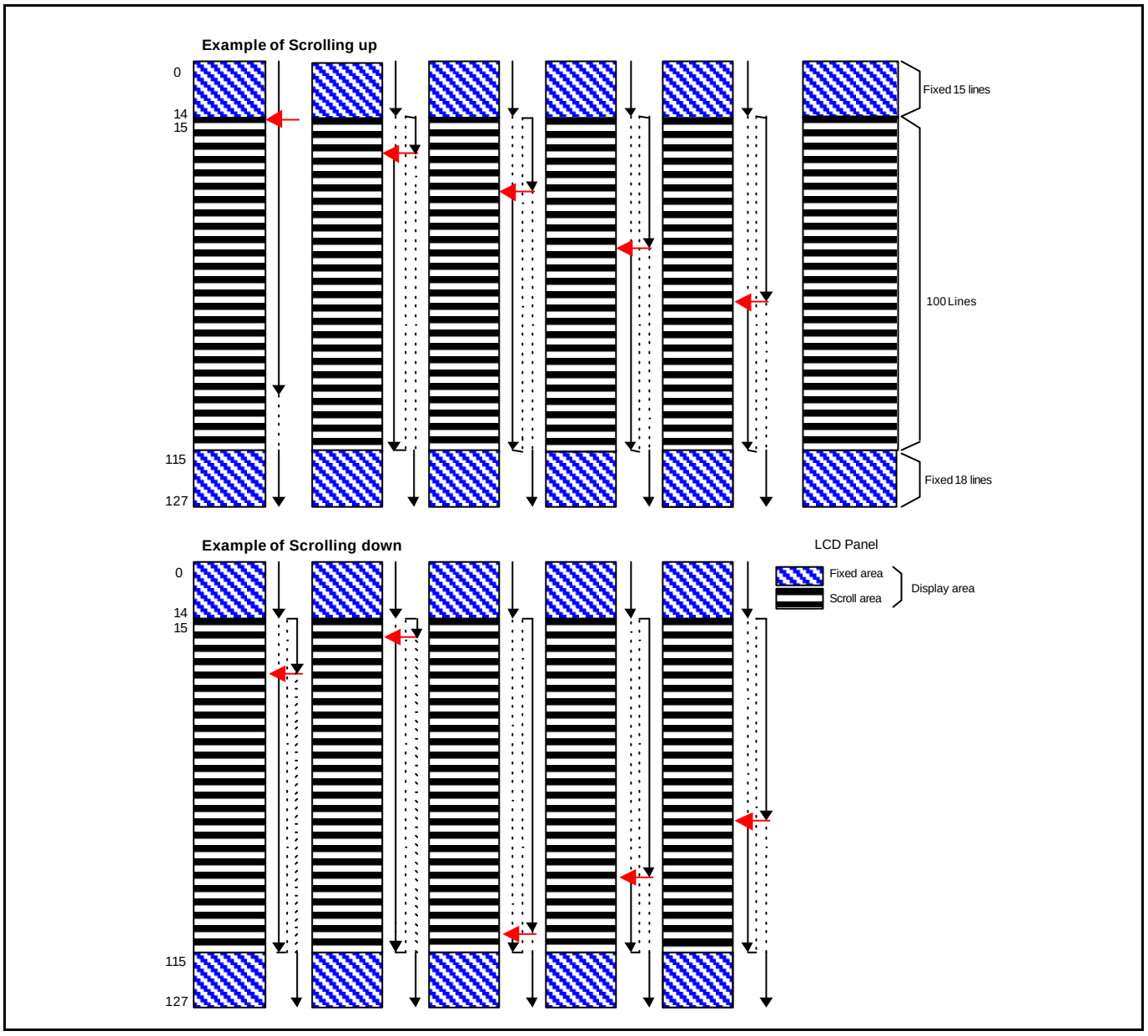


Figure 16. Area scroll examples (duty = 1/128, center scroll mode)

Display Direction

SDIR

The direction of segment display is selected by SDIR which is a bit in internal register.

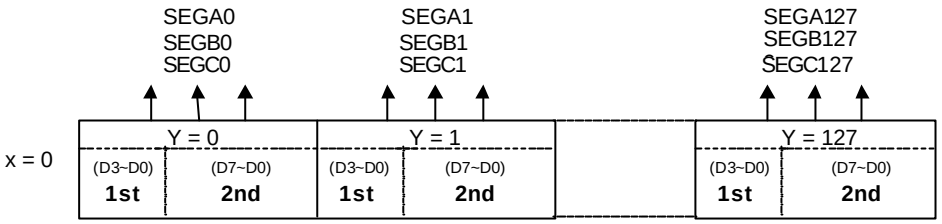


Figure 17. 8-bit data bus mode when SDIR = "0"

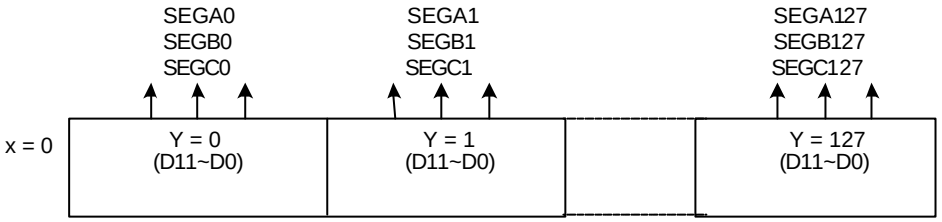


Figure 18. 16-bit data bus mode when SDIR = "0"

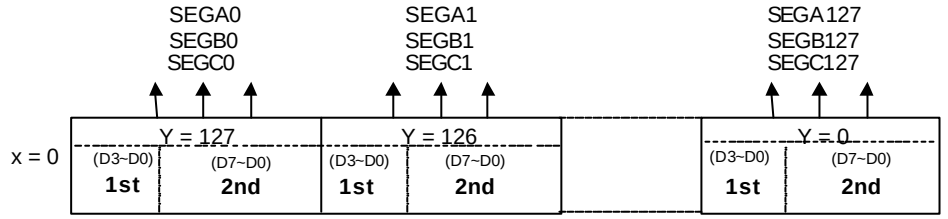


Figure 19. 8-bit data bus mode when SDIR = "1"

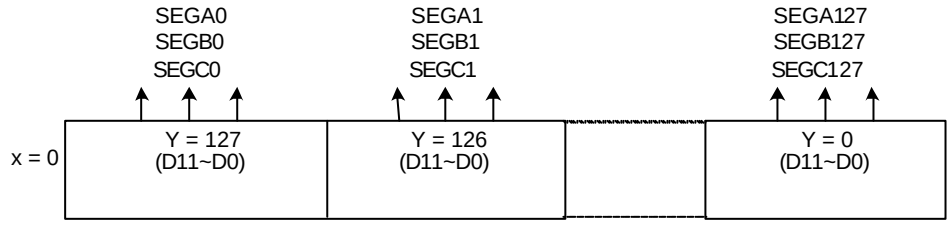
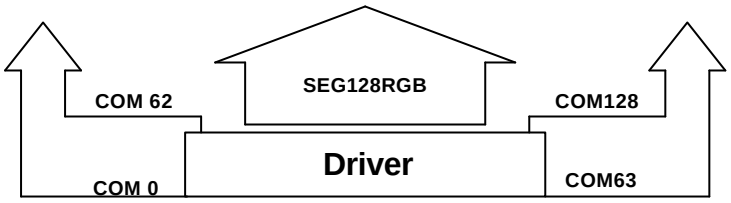


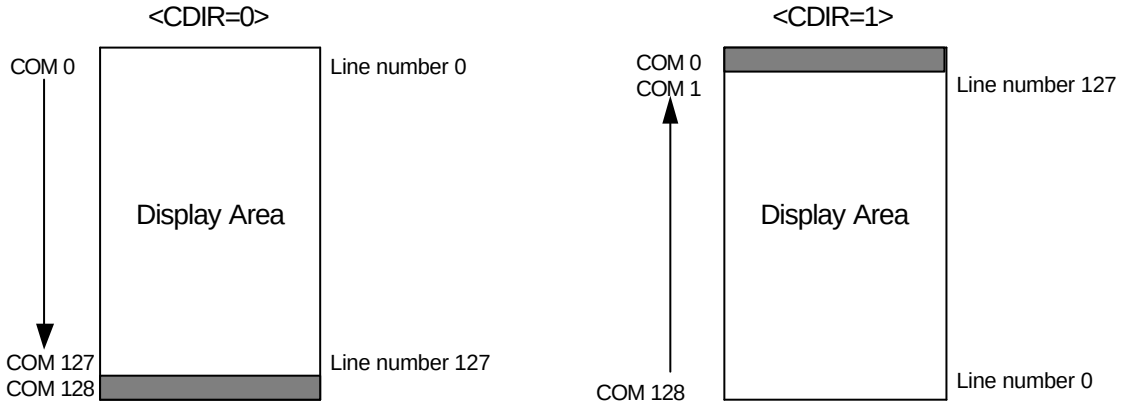
Figure 20. 16-bit data bus mode when SDIR = "1"

CDIR

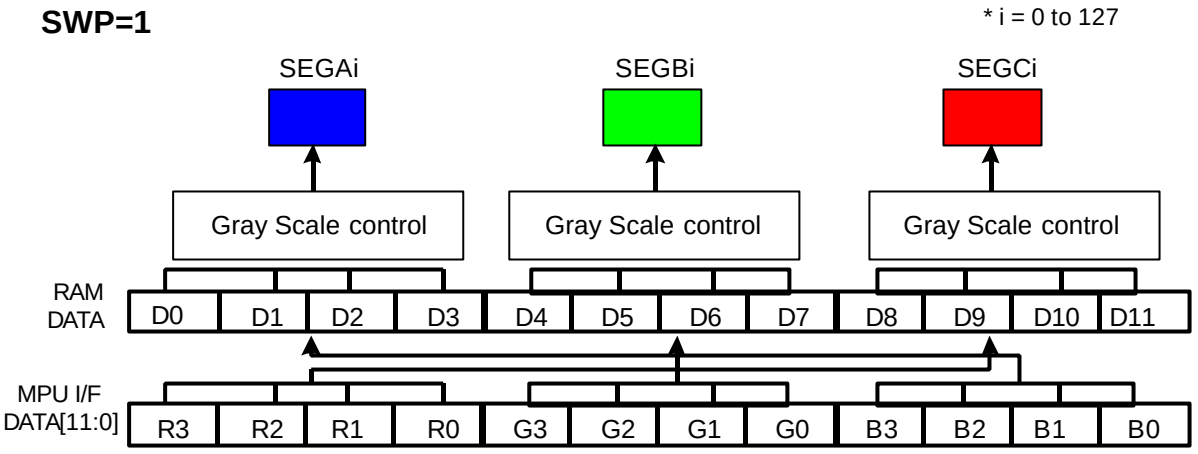
The direction of common scanning is selected by CDIR pin.



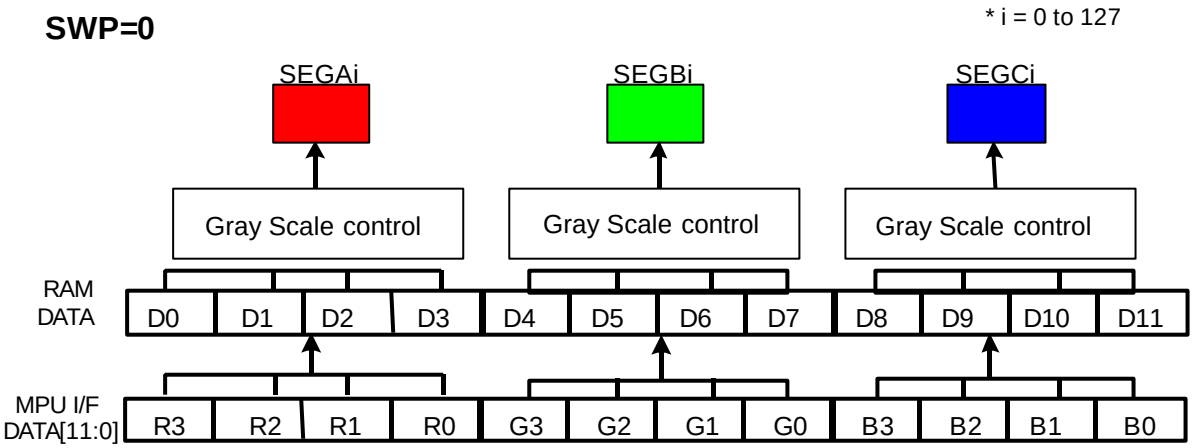
128Display Lines



SWP=1



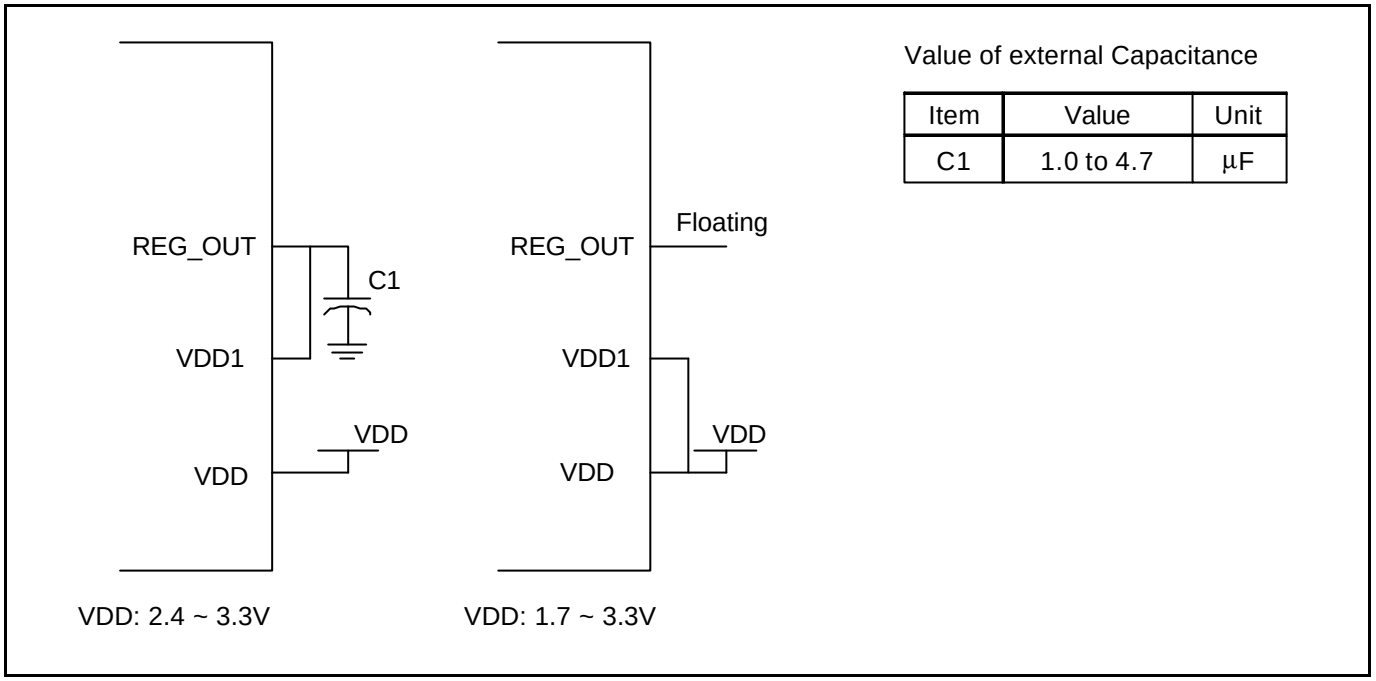
SWP=0



	SEGAi	SEGBi	SEGCi	
SWP = 0	RED	GREEN	BLUE	Color
	D11 ~ D8	D7 ~ D4	D3 ~ D0	Assigned Bit
SWP = 1	BLUE	GREEN	RED	Color
	D3~ D0	D7 ~ D4	D11 ~ D8	Assigned Bit

Figure 21. The relationship between SEG outputs and RGB color

On-Chip Regulator Configuration



Value of external Capacitance

Item	Value	Unit
C1	1.0 to 4.7	µF

Figure 22. Regulator Application

Oscillator Circuit

When internal oscillator is used(EXT=0), the selection of oscillator resistor is determined by display mode.

- Normal display mode/ Partial display mode 0 : resistor1 between OSC1 and OSC2
- Partial display mode 1 : resistor2 between OSC3 and OSC4
-

When external clock is used (EXT=1), clock frequency should be adjusted to display mode which is selected.

Example of external oscillator application

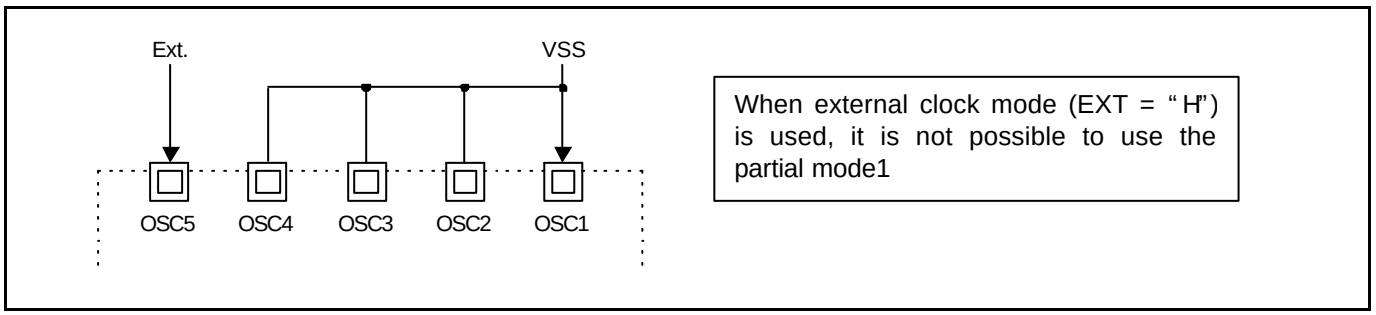
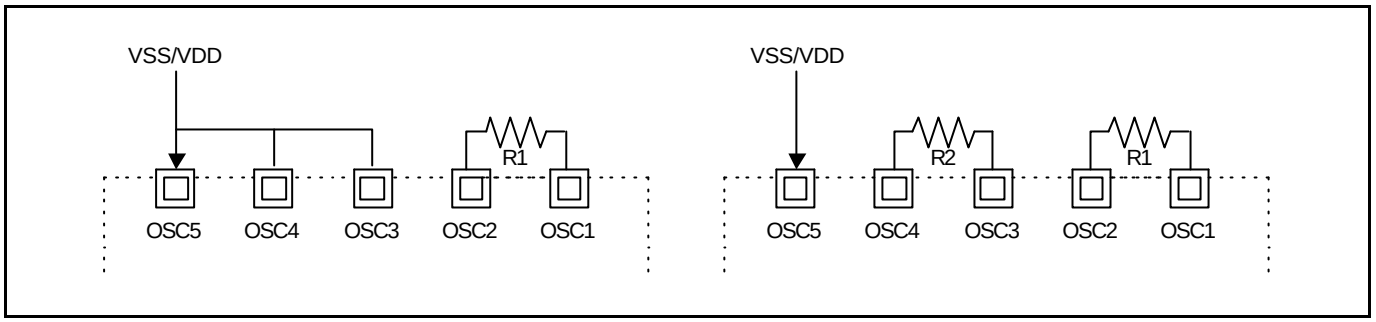


Figure 23. External oscillator application

Example of internal oscillator application

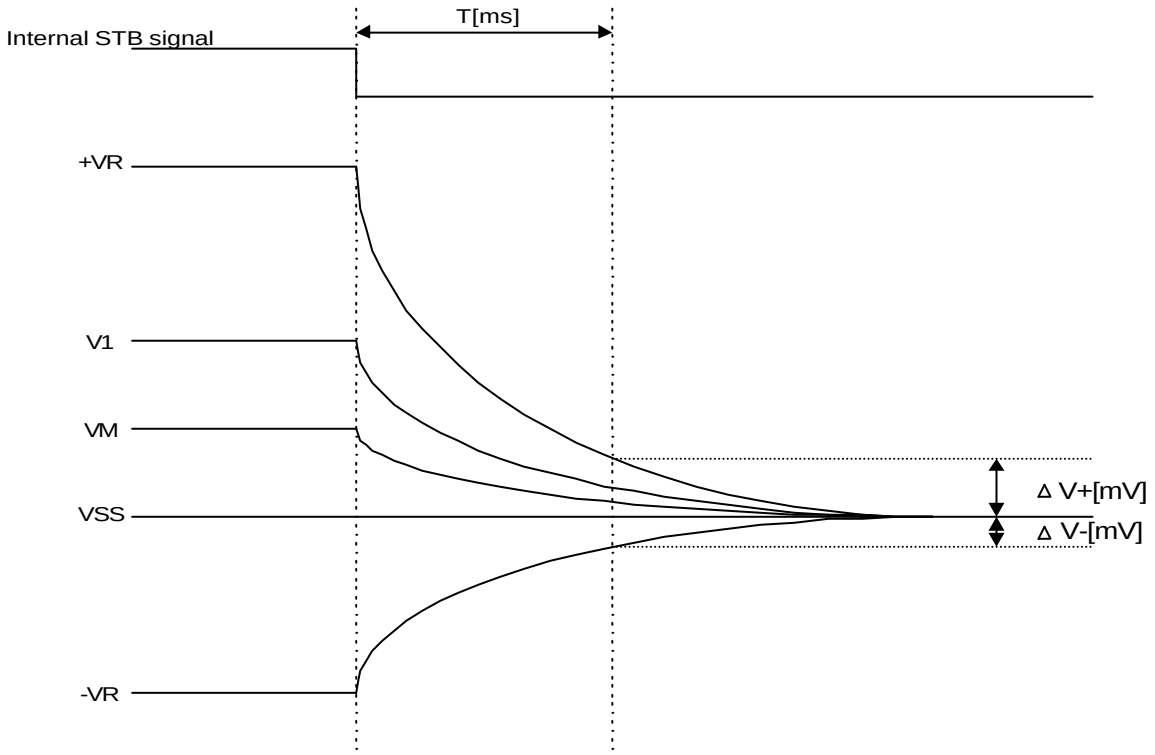


When partial display mode 1 is not used. When partial display mode 1 is used.

Figure 24. Internal oscillator application

Discharge Circuit

Driving voltage level discharge time at stand by ON.



The relation between voltage level and discharge time from when " Stand By ON" command is inputted.

LEVEL	CONDITION	T[ms]	△V+,△V-[mV]
+VR,V1,VM,-VR	+VR=10.5V, V1=3.0V, VM=1.5V, -VR=-7.5V at T=0	100	< 50
		300	< 20

INSTRUCTION DESCRIPTION

Table 15. Instruction Table

Instruction Name	D/I	/WR	/RD	DB15 ~DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.	Parameter
Non Operation	0	0	1	*	0	0	0	0	0	0	0	0	00	-
Oscillation Mode Set	0	0	1	*	0	0	0	0	0	0	1	0	02	1Byte
Driver Output Mode Set	0	0	1	*	0	0	0	1	0	0	0	0	10	1Byte
DC-DC Select	0	0	1	*	0	0	1	0	0	0	0	0	20	1Byte
DCDC Clock Division Set	0	0	1	*	0	0	1	0	0	1	0	0	24	1Byte
DCDC and AMP ON/OFF set	0	0	1	*	0	0	1	0	0	1	1	0	26	1Byte
Temperature Compensation Set	0	0	1	*	0	0	1	0	1	0	0	0	28	1Byte
Contrast Control(1)	0	0	1	*	0	0	1	0	1	0	1	0	2A	1Byte
Contrast Control(2)	0	0	1	*	0	0	1	0	1	0	1	1	2B	1Byte
Standby Mode OFF	0	0	1	*	0	0	1	0	1	1	0	0	2C	-
Standby Mode ON	0	0	1	*	0	0	1	0	1	1	0	1	2D	-
Addressing Mode Set	0	0	1	*	0	0	1	1	0	0	0	0	30	1Byte
ROW Vector Mode Set	0	0	1	*	0	0	1	1	0	0	1	0	32	1Byte
N-line Inversion Set	0	0	1	*	0	0	1	1	0	1	0	0	34	1Byte
Red palette Set	0	0	1	*	0	0	1	1	1	0	0	0	38	8Byte
Green palette Set	0	0	1	*	0	0	1	1	1	0	1	0	3A	8Byte
Blue palette Set	0	0	1	*	0	0	1	1	1	1	0	0	3C	4Byte
Entry Mode Set	0	0	1	*	0	1	0	0	0	0	0	0	40	1Byte
X-address Area Set	0	0	1	*	0	1	0	0	0	0	1	0	42	2Byte
Y-address Area Set	0	0	1	*	0	1	0	0	0	0	1	1	43	2Byte
Display OFF	0	0	1	*	0	1	0	1	0	0	0	0	50	-
Display ON	0	0	1	*	0	1	0	1	0	0	0	1	51	-
Specified Display Pattern Set	0	0	1	*	0	1	0	1	0	0	1	1	53	1Byte
Partial Display Mode Set	0	0	1	*	0	1	0	1	0	1	0	1	55	1Byte
Partial Display Start Line Set	0	0	1	*	0	1	0	1	0	1	1	0	56	1Byte
Partial Display End Line Set	0	0	1	*	0	1	0	1	0	1	1	1	57	1Byte
Area Scroll Mode Set	0	0	1	*	0	1	0	1	1	0	0	1	59	4Byte
Scroll Start Line Set	0	0	1	*	0	1	0	1	1	0	1	0	5A	1Byte
Display Format Select(Mode0)	0	0	1	*	0	1	1	0	1	1	1	0	60	-
Display Format Select(Mode1)	0	0	1	*	0	1	1	0	1	1	1	1	61	-
Set Display Data Length	X	X	X	*	1	1	1	1	1	1	0	0	FC	2Byte
Display Data Write	1	0	1	Display Data Write									-	-
Display Data Read	1	1	0	Display Data Read									-	-
Status Read	0	1	0	Status Data Read									-	-
Test Mode0	0	0	1	*	1	1	1	1	1	1	1	1	FF	-
Test Mode1	0	0	1	*	1	1	1	1	1	1	1	0	FE	-

*: Don' t care
Parameter: The number of parameter bytes that follows instruction data.

Non Operation (00H)

This instruction is Non operation.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0	0

Oscillation Mode Set (02H)

Setting internal function mode.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1	0
			0	0	0	0	0	DIV2	EXT	OSC

DIV2: Display clock selecting
DIV2 = 0: Display clock = OSC clock (Initial status)
DIV2= 1: Display clock = OSC/2 clock
EXT: External clock selecting
EXT = 0: Internal clock mode (Initial status)
EXT = 1: External clock mode
OSC: Internal oscillator ON/OFF
OSC = 0: Internal oscillator OFF(Initial status)
OSC = 1: Internal oscillator ON

Driver Output Mode Set(10H)

This instruction sets the display direction.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	0	0	0	0
			0	0	0	0	0	0	SDIR	SWP

SDIR: Segment direction
This bit is for controlling the direction of segment driver.
SDIR = 0 (Initial status)

SWP: Swap segment output SEGAi and SEGCi
This bit is for swapping the output of segment driver.
SWP = 0 (Initial status)

DC-DC Select (20H)

Selects DC-DC step-up of the common driver in normal and partial mode

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	0	0	0
			0	0	0	0	0	0	DC(2)	DC(1)

DC(1) : 1' st DC-DC booster boosting step select for V1 generation in normal mode and partial mode 0.
DC(2) : 1' st DC-DC booster boosting step select for V1 generation in partial mode 1.

DC(2) : In partial mode 1	
DB1	DC-DC step up
0	X1.0
1	X1.5

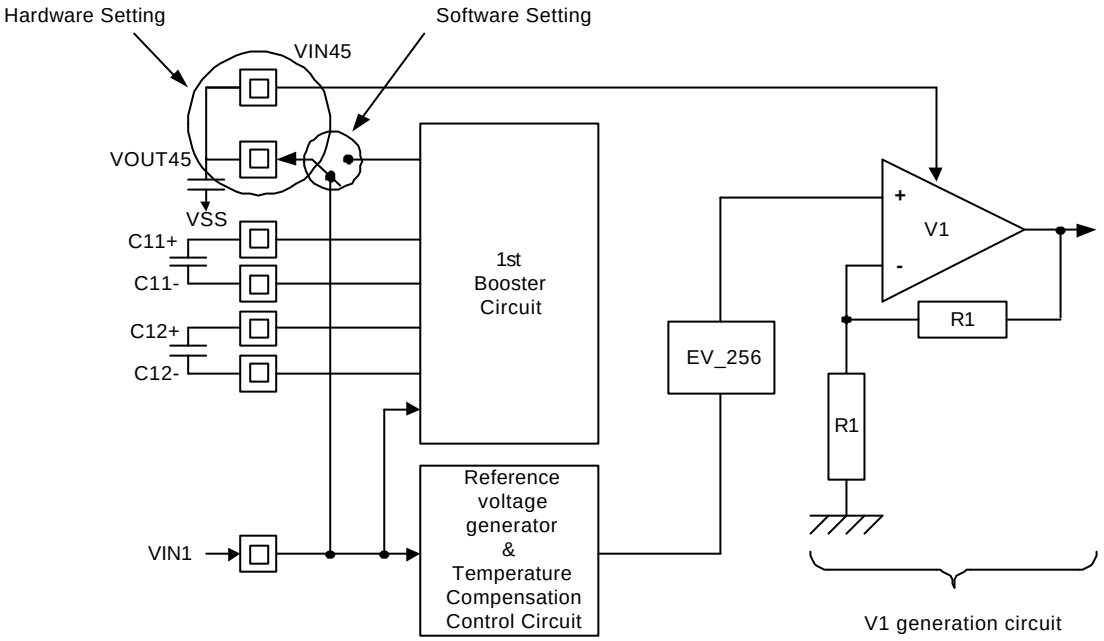
DC(1) : In normal mode, partial mode 0	
DB0	DC-DC step up
0	X1.0
1	X1.5

DC-DC Select and power supply for V1 Op-Amp.

Even if VIN45 is connected to VOUT45 or VIN1, a setup by software must be able to be performed. Power supply for V1 Op.Amp. is decided by Hardware setting and Software setting.

The example of usage is shown below.

Figure28. Example : Hardware Setting : VIN45 connected to VOUT45
Software Setting : Power supply for V1 Op.Amp. uses VIN1 (not VOUT45).



Hardware setting : VIN45 connected to (1) VIN1 (when 1' st boosting is not used)
(2) VOUT45 (when 1' st boosting is used)
Software setting : DC-DC Select(20H) - DC(1), DC(2)
Set value "00" Power supply for V1 Op.Amp. uses VIN1 directly.
Set value "01" or "10" Power supply for V1 Op.Amp. uses VOUT45.

DCDC Clock Division (24H)

This instruction sets the internal booster clock frequency.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	0	0
			0	0	DIV(2)		0	0	DIV(1)	

DIV(1) : DC-DC Charge Pump Division Ratio in Normal Mode Display and Partial Display Mode0
- DIV(1) = 10 (Initial status)

DIV(2) : Division Ratio in Partial Display Mode1
- DIV(2) = 10 (Initial status)

DB5	DB4	DIV(2)
0	0	fPCK = fOSC/2x
0	1	fPCK = fOSC/4x
1	0	fPCK = fOSC/6x
1	1	fPCK = fOSC/8x

DB1	DB0	DIV(1)
0	0	fPCK = fOSC/2x
0	1	fPCK = fOSC/4x
1	0	fPCK = fOSC/6x
1	1	fPCK = fOSC/8x

Note: fOSC = (ROUNDUP (Duty/3) + dummy) x 4 x 4 x frame frequency

DC/DC and AMP ON/OFF Set (26H)

This instruction set up the DC/DC and Op-amp in common start up setting.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	1	0
			0	0	0	0	AMP	DCDC3	DCDC2	DCDC1

AMP : Built-in OP-AMP ON/OFF.
- AMP=0 :OP-AMP OFF(Initial status)
- AMP=1 :OP-AMP ON

DCDC1: Built-in 1st Booster ON/OFF (Initial status)
- DCDC1= 0: 1st Booster OFF (Initial status)
- DCDC1= 1: 1st Booster ON

DCDC2: Built-in 1st Booster ON/OFF (Initial status)
- DCDC2= 0: 2nd Booster OFF (Initial status)
- DCDC2= 1: 2nd Booster ON

DCDC3: Built-in 1st Booster ON/OFF (Initial status)
- DCDC3= 0: 3rd Booster OFF (Initial status)
- DCDC3= 1: 3rd Booster ON

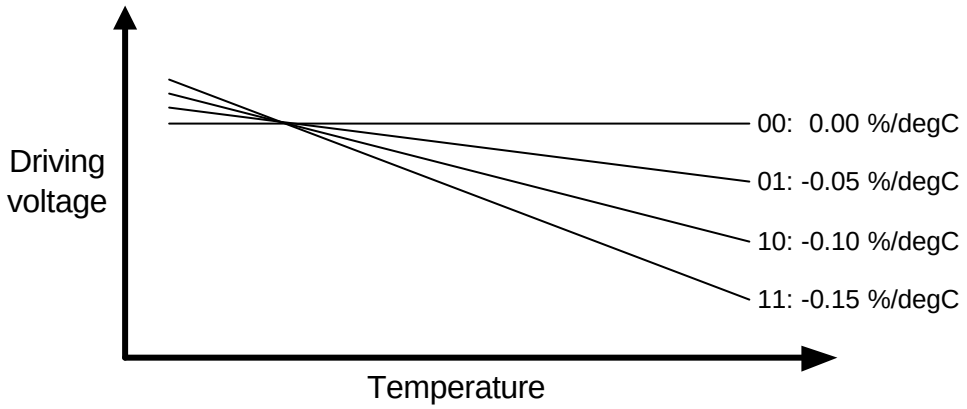
Temperature Compensation Set (28H)

This Instruction sets up the driving voltage slope for temperature compensation.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	0	0
			0	0	0	0	0	0	TCS	

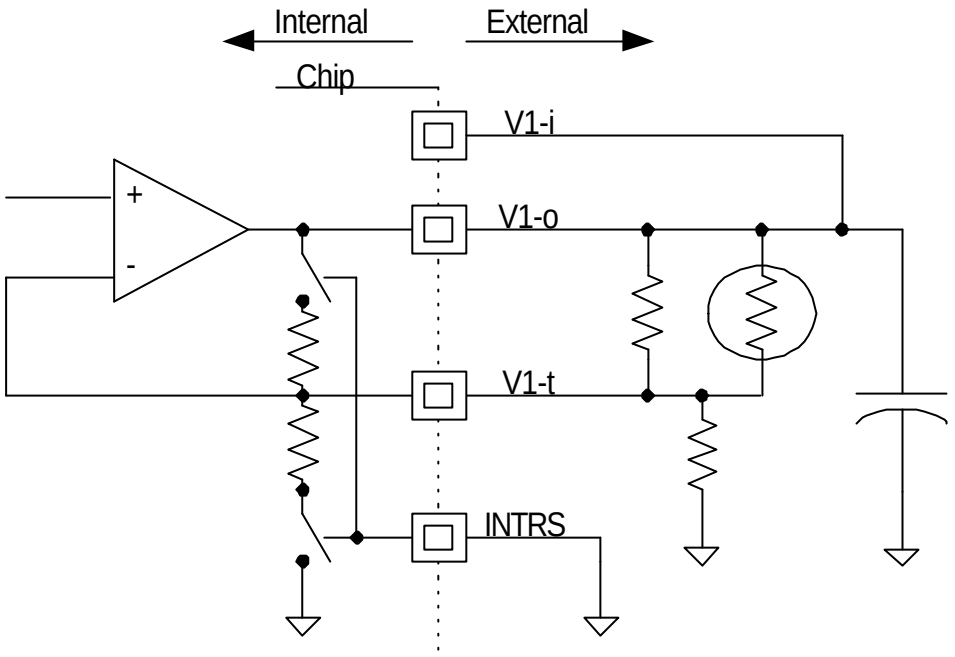
TCS: Temperature compensation slope set

- TCS = 00 : 0.00%/degC
- TCS = 01 : -0.05%/degC
- TCS = 10 : -0.10%/degC
- TCS = 11 : -0.15%degC



Temperature Compensation

If external temperature compensation is needed, circuit diagram is described as below. To use temperature compensation, two resistors and one thermistor are needed.



Contrast Control (1) (2AH)

This instruction updates the contrast control value in normal display mode and partial display mode 0.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	1	0
			Contrast control value (0 to 255)							

The relation between V1 voltage (typ.) and Contrast(1) set value (3bit step case)

Contrast(1) (HEX)	V1[V]	Contrast(1) (HEX)	V1[V]	Contrast(1) (HEX)	V1[V]	Contrast(1) (HEX)	V1[V]	Contrast(1) (HEX)	V1[V]	Contrast(1) (HEX)	V1[V]
00h	2.000	30h	2.244	60h	2.488	90h	2.731	C0h	2.975	F0h	3.219
08h	2.041	38h	2.284	68h	2.528	98h	2.772	C8h	3.016	F8h	3.259
10h	2.081	40h	2.325	70h	2.569	A0h	2.813	D0h	3.056	FFh	3.300
18h	2.122	48h	2.366	78h	2.609	A8h	2.853	D8h	3.097		
20h	2.163	50h	2.406	80h	2.650	B0h	2.894	E0h	3.138		
28h	2.203	58h	2.447	88h	2.691	B8h	2.934	E8h	3.178		

Contrast Control (2) (2BH)

This instruction updates the contrast control value in partial display mode 1.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	0	0	0	1
			Contrast control value (0 to 255)							

The relation between V1 voltage (typ.) and Contrast(2) set value (3bit step case)

Contrast(1) (HEX)	V1[V]	Contrast(1) (HEX)	V1[V]	Contrast(1) (HEX)	V1[V]	Contrast(1) (HEX)	V1[V]	Contrast(1) (HEX)	V1[V]	Contrast(1) (HEX)	V1[V]
00h	2.000	30h	2.244	60h	2.488	90h	2.731	C0h	2.975	F0h	3.219
08h	2.041	38h	2.284	68h	2.528	98h	2.772	C8h	3.016	F8h	3.259
10h	2.081	40h	2.325	70h	2.569	A0h	2.813	D0h	3.056	FFh	3.300
18h	2.122	48h	2.366	78h	2.609	A8h	2.853	D8h	3.097		
20h	2.163	50h	2.406	80h	2.650	B0h	2.894	E0h	3.138		
28h	2.203	58h	2.447	88h	2.691	B8h	2.934	E8h	3.178		

Standby Mode OFF (2CH)

This instruction releases the standby mode.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	0

The internal statuses during standby off are as following:

- All common and segment output: refer to following
- Oscillator circuit: On (EXT = 0, OSC=1),OFF (others)
- Displaying clocks (FR, PM, CL, CK): In operation

Function and Pin condition at standby OFF

Function/Pin	Condition
DC/DC booster(1' st,2' nd,3' rd)	ON(Operate)
COM outputs	+VR /VM / VSS /–VR
SEG outputs	V1 /VSS

Standby Mode ON (2DH)

This instruction enters the standby mode to reduce the power consumption to the static power consumption value (Initial status). The following instructions, standby off and display on, cause returning to the normal operation status.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	1

The internal statuses during standby on are as following:

- All common and segment output: refer to following table
- Oscillator circuit: OFF
- Displaying clocks (FR, PM, CL, CK) are held.

Function and Pin condition at standby ON

Function/Pin	Condition
DC/DC booster(1' st,2' nd,3' rd)	OFF
SEG and COM outputs	VSS

LCD driving power output condition at Standby ON.

Level	Condition
+VR	VSS
V1	VSS
VM	VSS
-VR	VSS

Addressing Mode Set (30H)

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	0	0
			0	0	GSM	DSG	SGF	SGP		SGM

GSM: Gray Scale Mode
- 0 : 4,096 Color mode(Initial status)
- 1 : 256 Color mode
  1. 8 bit mode : DB[7:0] :RRRGGGBB
  2. 16bit mode: DB[15:0] :RRRGGGBBRRRGGGBB
  3. 3bits of R and G, 2bits of B are expanded to 4 bit internally by red, green and blue palette set instruction

DSG : Duty Adjust Setting
- 0 : Dummy subgroup is one subgroup (Initial status)
- 1 : Dummy subgroup is none

SGF : SG Frame Inversion mode setting
- 0: SG Frame inversion OFF (Initial status)
- 1: SG Frame inversion ON

SGM : SG inversion mode setting
- 0: SG inversion OFF (Initial status)
- 1: SG inversion ON

SGP : SG Phase mode setting
- 00 : Same phase in all pixels
- 01 : Different phase by 1pixel-unit
- 10 : Different phase by 2pixel-unit
- 11 : Different phase by 4pixel-unit

Row Vector Mode Set (32H)

Setting ROW function.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	1	0
			0	0	0	0	INC			VEC

INC: Row Vector Increment Mode. This Parameter set up Row vector increment period

DB3	DB2	DB1	Row Vector Increment Period
0	0	0	Every subgroup
0	0	1	Every 2subgroup
0	1	0	Every 4subgroup
0	1	1	Every 8subgroup
1	0	0	Every 16subgroup
1	0	1	Every 16subgroup
1	1	0	Every 16subgroup
1	1	1	Every subframe

VEC: ROW Vector Sequence Mode
- 0: R1->R2->R3->R4 -> R1.…. (initial status)
- 1: R1->R3->R2->R4 -> R1.….

N-block inversion Set (34H)

This instruction set up N block inversion for AC driving.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	1	1	1	1
			FIM	FIP	0	N-block inversion				

FIM: Forcing Inversion Mode
FIM = 0: Forcing Inversion OFF (Initial status)
FIM = 1: Forcing Inversion ON
FIP: Forcing Inversion Period
FIP = 0: Forcing Inversion Period is one frame
FIP = 1: Forcing Inversion Period is two frames
N-block Inversion : This parameter indicates the basic period of polarity inversion.
The whole period of polarity inversion is decided by FIM, FIP and this parameter.

DB7	DB6	DB5	DB4 – DB0	Polarity Inversion Period
X	x	x	0	every frame
0	x	x	1	every 1 block
:	:	:	:	:
0	x	x	31	every 31 blocks
1	0	x	1	every 1 block and every frame
:	:	:	:	:
1	0	x	31	every 31 blocks and every frame
1	1	x	1	every 1 block and every 2 frames
:	:	:	:	:
1	1	x	31	every 31 blcks and every 2 frames

Red palette Set (38H)

Setting red gray scale data for 256 Color mode.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	0	0	0
			0	0	0	0	RAM data “000” to GS data			
			0	0	0	0	RAM data “001” to GS data			
			0	0	0	0	RAM data “010” to GS data			
			0	0	0	0	RAM data “011” to GS data			
			0	0	0	0	RAM data “100” to GS data			
			0	0	0	0	RAM data “101” to GS data			
			0	0	0	0	RAM data “110” to GS data			
			0	0	0	0	RAM data “111” to GS data			

Green palette Set (3AH)

Setting green gray scale data for 256 Color mode.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	0	1	0
			0	0	0	0	RAM data “000” to GS data			
			0	0	0	0	RAM data “001” to GS data			
			0	0	0	0	RAM data “010” to GS data			
			0	0	0	0	RAM data “011” to GS data			
			0	0	0	0	RAM data “100” to GS data			
			0	0	0	0	RAM data “101” to GS data			
			0	0	0	0	RAM data “110” to GS data			
			0	0	0	0	RAM data “111” to GS data			

Blue palette Set (3CH)

Setting blue gray scale data for 256 Color mode.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	1	0	0
			0	0	0	0	RAM data “000” to GS data			
			0	0	0	0	RAM data “001” to GS data			
			0	0	0	0	RAM data “010” to GS data			
			0	0	0	0	RAM data “011” to GS data			

Entry Mode Set (40H)

Setting internal function mode.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	0	0
			0	0	0	0	0	HL	X/Y	RMW

HL: Exchange higher and lower byte only for "Display Data Write/Read" in 256 color & 16-bit data bus .
HL = 0 : Exchange status(initial status)
HL = 1 : Not exchange status

X/Y: Memory address counter mode setting
X/Y = 0: Y address counter mode (Initial status)
X/Y = 1: X address counter mode (Don' t use in 256 color & 16bit data bus mode)

RMW: Read modify write mode ON/OFF select
RMW = 0: Read modify write OFF (Initial status)
RMW = 1: Read modify write ON. When this mode is on, X(Y) address of on-chip display RAM is increment not in reading display data but in writing display data.

X Address Area Set (42H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	0
			0	X start address set (Initial Status = 00H)						
			0	X end address set (Initial Status = 7FH)						

The current X address of the on-chip display data RAM is the X start address by setting this instruction. In X address count mode (X/Y = "H"), the X address is increased from X start address to X end address. When X address is equal to the X end address, the Y address is increased by 1 and the X address returns to X start address. The X start and X end addresses must be set as a pair and X start address must be less than X end address.

Address Area Set (43H)

This instruction and parameter set up the Y address areas of the on-chip display data RAM.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	1
			0	Y start address set (Initial Status = 00H)						
			0	Y end address set (Initial Status = 7FH)						

The current Y address of the on-chip display data RAM is the Y start address by setting this instruction. In Y address count mode (X/Y = "L"), the Y address is increased from Y start address to Y end address. When Y address is equal to the Y end address, the X address is increased by 1 and the Y address returns to Y start address. The Y start and Y end address must be set as a pair and Y start address must be less than Y end address.

Display OFF (50H)

Turn the display OFF(Initial status).
When display is off, all segment and common output are VSS level.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	0

Function and Pin condition at Display OFF

Function/Pin	Condition
DC/DC booster(1^{st},2^{nd},3^{rd})	ON(Operate)
SEG and COM outputs	VSS

Display ON (51H)

Turns the display ON.
In case of being standby mode, this instruction does not work. This instruction is executed after standby mode off.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	1

Function and Pin condition at Display ON

Function/Pin	Condition
DC/DC booster(1^{st},2^{nd},3^{rd})	ON(Operate)
COM outputs	+VR /VM /-VR
SEG outputs	V1 /VSS

Specified Display Pattern Set (53H)

This instruction sets the specified display pattern.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	1	1
			0	0	0	0	0	0	SDP	

SDP : Specified Display Pattern set
- SDP = 00 : Normal display
- SDP = 01 : Reverse display : Display data reversing mode setting without the contents of the display RAM
- SDP = 10 : Whole display pattern becomes OFF regardless of the RAM data.
- SDP = 11 : Whole display pattern becomes ON regardless of the RAM data.

Partial Display Mode Set (55H)

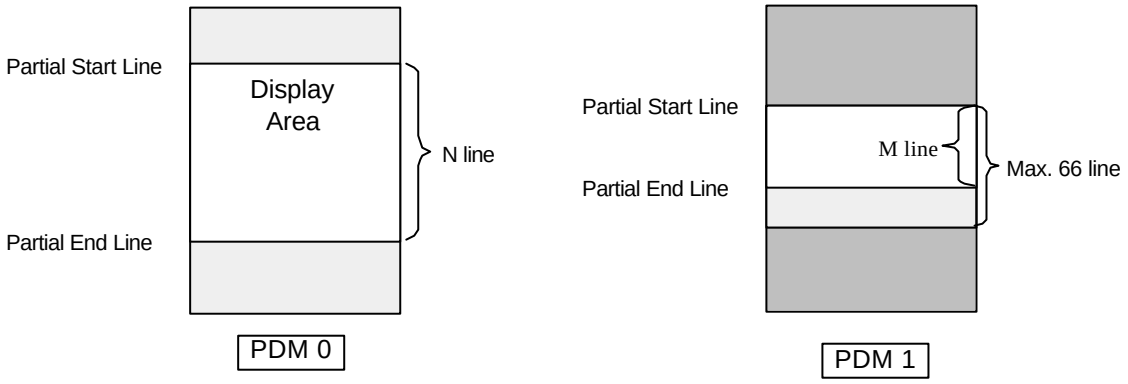
D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	0	1
			0	0	0	0	0	0	PDM	PT

PT: Partial Display ON/OFF
- PT = 0: Partial display OFF = Normal mode (Initial status)
- PT = 1: Partial display ON

PDM: Partial Display mode set
- PDM = 0: Partial mode 0 : Duty ratio is same as Normal display mode(initial status)
- PDM = 1: Partial mode 1 : Duty ratio is changed from Normal display mode(66 duty fixed)

Applied parameter in PDM0 and PDM1 are summarized as below

PDM	Contrast	Duty	Bias	DC-DC Select	OSC	PCK
0	Contrast control(1)	Normal	Bias(1)	DC-DC(1),DC(1)	OSC1-OSC2	DIV(1)
1	Contrast control(1)	1/66	Bias(2)	DC-DC(1),DC(2)	OSC3-OSC4	DIV(2)



No display Area : No COM Scanning field (COM = Vm fixed)

Except Partial Display Area : COM Timing is existing, but COM = Vm fixed

Partial Display Area : Real display field

Operation in Partial Display Mode 0 (PDM=0)

On scanning except partial display area
- -SEG output select V0 or V1 level depend on " FR" value. Refer to 44
- -All of COM output is fixed VM level.

On scanning partial display area
- -It is equal to be in normal mode

Operation in Partial Display Mode 1 (PDM=1)

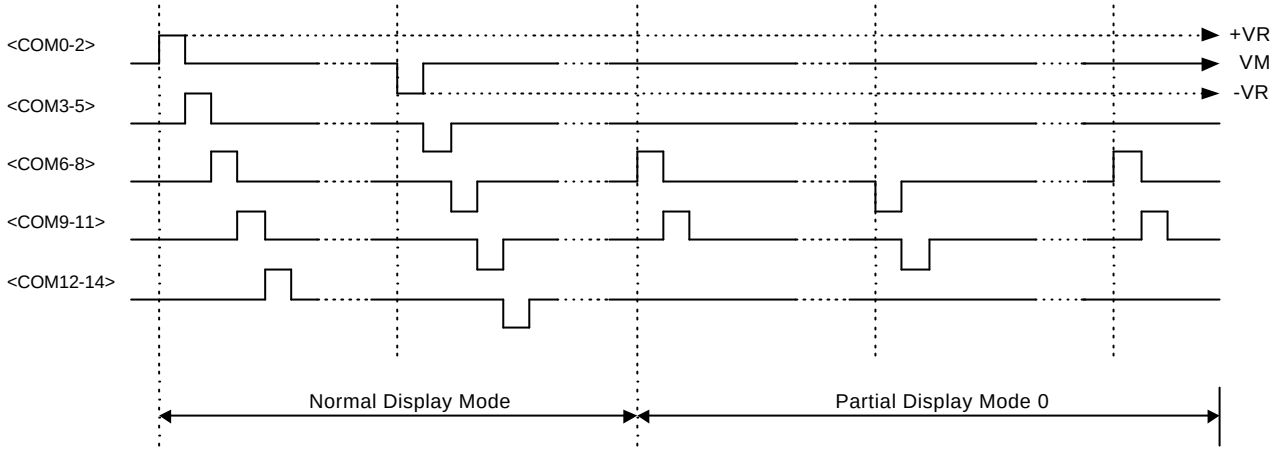
Display area is from partial start line to partial end line.
(COM driver output is fixed VM except display area, only max66 line output COM signal.

On scanning except partial display area
- -SEG output select V0 or V1 level depend on " FR" value. Refer to Page44
- -All of COM output is fixed VM level.

On scanning partial display area
- -It is equal to be in normal mode

Partial Display Mode0

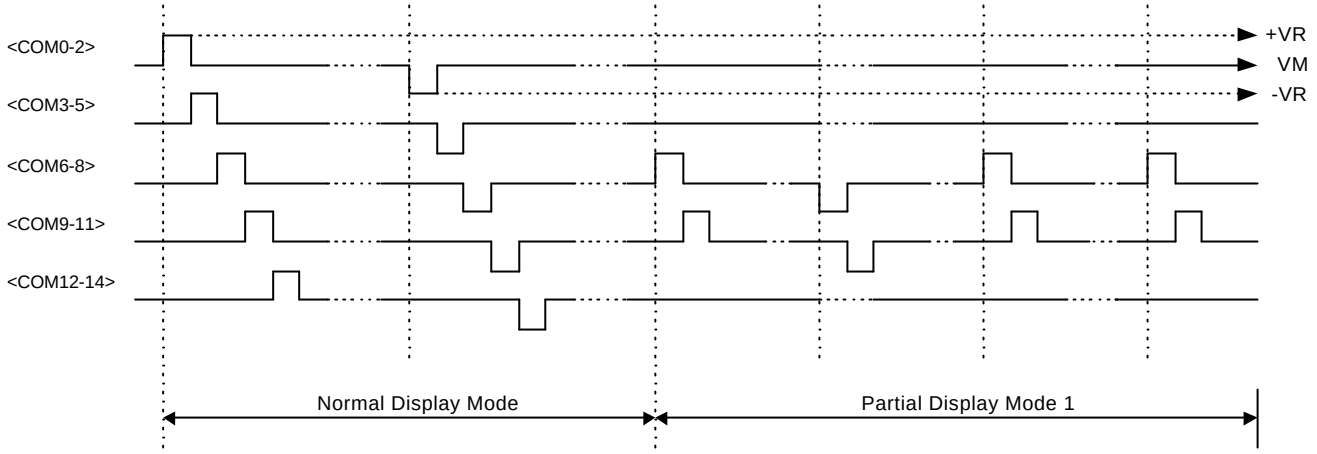
In case of COM 6 to COM11 Partial display



Item	Partial Display Area	Out of Partial Display Area
Duty	Same as normal display mode	
Contrast	Same as normal display mode (Contrast(1) setting)	
Oscillator	Same as normal display mode (OSC1 – OSC2)	
SEG Output level	Same as normal mode (V1,V0)	Depends on Internal " FR" signal See page 44
COM Output level	Same as normal mode (+VR,VM,-VR)	VM fixed

Partial display mode1

In case of COM 6 to COM11 Partial display



Item	Partial Display Area	Out of Partial Display Area	Out of Display Area
Duty	1/66duty		
Contrast	Contrast(2) setting		
Oscillator	(OSC3 – OSC4) setting value		
SEG Output level	Same as normal mode (V1,V0)	Depends on " FR" signal See page 44	-
COM Output level	Same as normal mode (+VR, VM, -VR)	VM fixed	VM fixed

Partial Display Start Line Set (56H), Partial Display End Line Set(57H)

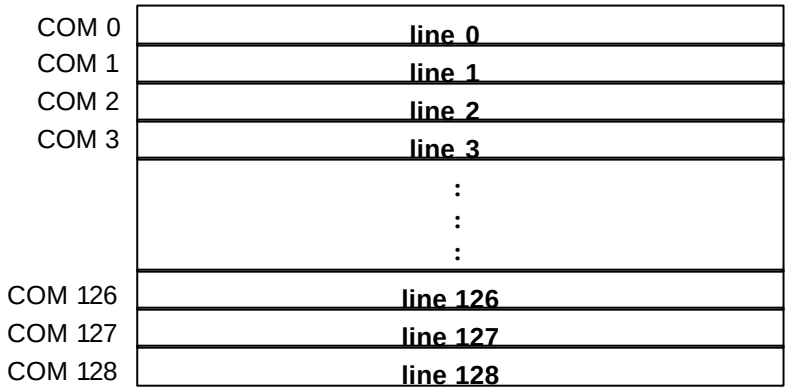
These 2 instructions set the partial display area and it is possible to display a part.

Partial Display Start Line Set (56H)

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	0
			0	Partial start line						

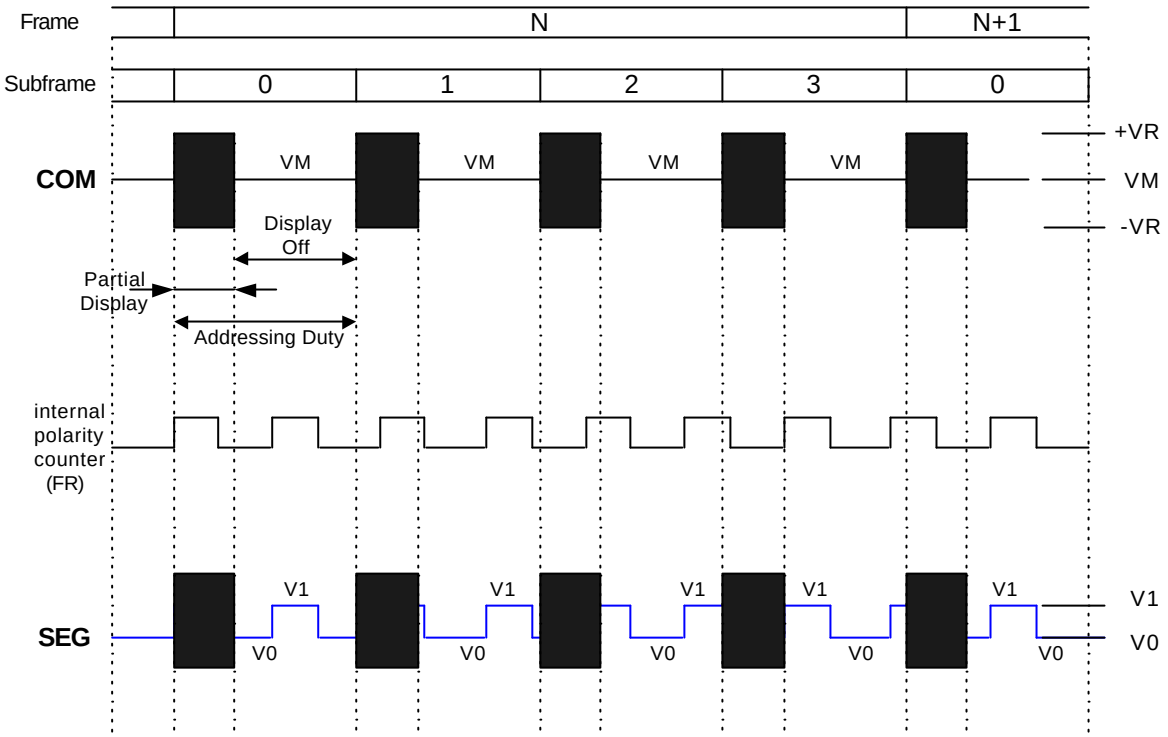
Partial Display End Line Set (57H)

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	1
			0	Partial end line						



Parameter set appoints display line number. At PDM 0, Parameter Size is able to be in a number of Display lines. But that is not able to be over max 66 line at PDM 1. Partial end line must set bigger number than Partial start line.

Example of Segment Voltage in non-display area



Area scroll Set (59H)

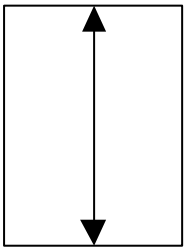
This instruction sets up area scroll field (start line, end line, Lower fixed line number), and it is possible to make screen to display as partial scroll field.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	0	1
			0	0	0	0	0	0	SCM	
			0	Scroll area start line						
			0	Scroll area end line						
			0	Lower fixed number						

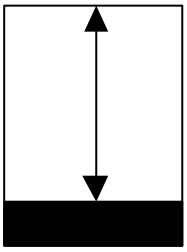
Note: In lower and center scroll mode, scroll area end line must be smaller than duty - lower fixed number.

SCM: Scroll mode setting

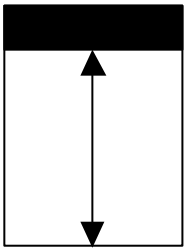
DB1	DB0	Mode
0	0	Entire display(Initial status)
0	1	Upper scroll display
1	0	Lower scroll display
1	1	Center scroll display



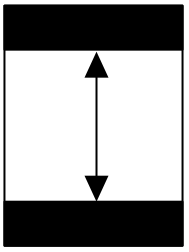
Entire Display



Upper Display



Lower Display



Center Display

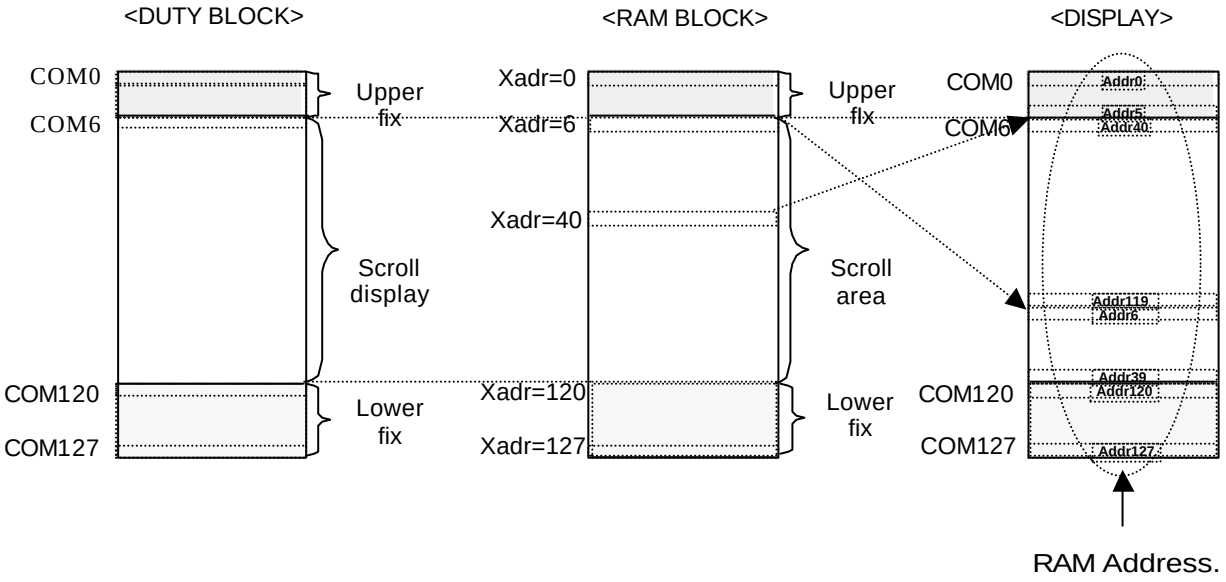
Scroll Start Line Set (5AH)

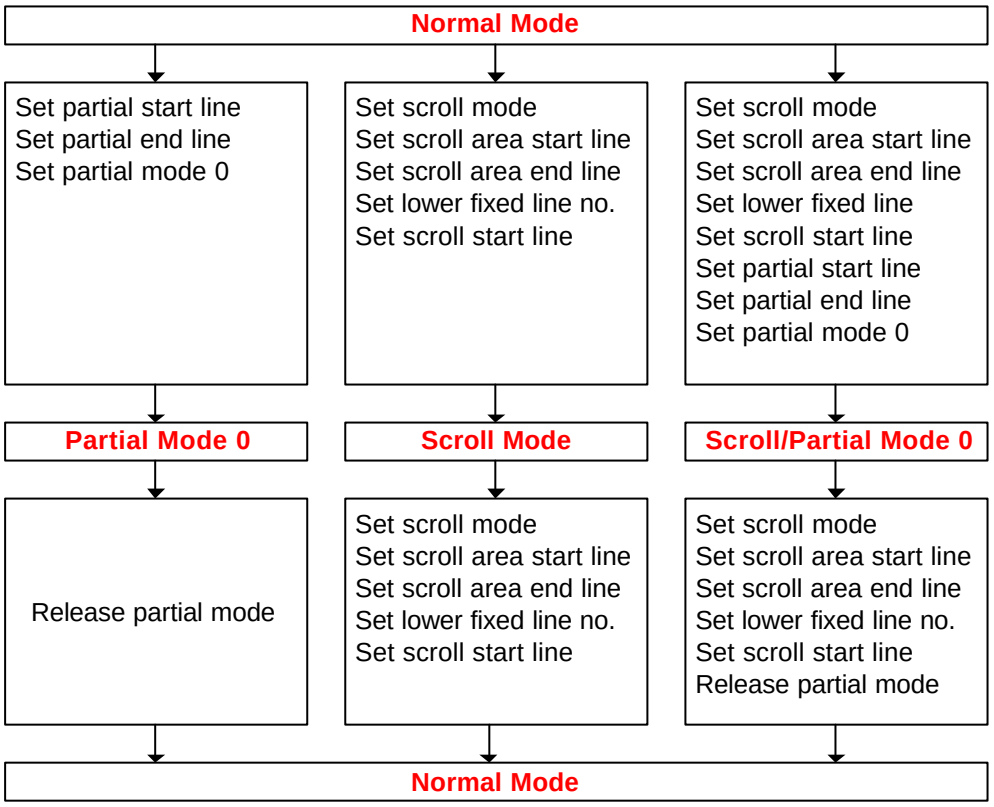
This instruction and parameter set up scroll start line. On this instruction, scroll start line becomes the first of area scroll field. Scroll operation is occurred every issue of this instruction.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	1	0
			0	Scroll start line						

<Example>

-SCM : 2' b11 (Center display mode)
-Scroll area start line : 6
-Scroll area end line : 119
-Lower fixed number : 8
-Scroll start line : 40





Data Format Select (60H/61H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	0	0	0	0	DFS

DFS: 4,096 Color Mode Data Format Select
- 0 : 4,096 Color Data Format A (Initial Status)
  - 8 bit mode :
    - DB[7:0] : XXXXRRRR (1' st write)
    - DB[7:0] : GGGGBBBB(2' nd write)
  - 16 bit mode :
    - DB[15:0] :XXXXRRRRGGGGBBBB (12 bit)
- 1 : 4,096 Color Data Format B
  - 8 bit mode :
    - DB[7:0] : RRRRGGGG(1' st write)
    - DB[7:0] : BBBBRRRR (2' nd write)
    - DB[7:0] : GGGGBBBB(3' rd write)
  - 16 bit mode :
    - DB[15:0] :RRRRGGGGBBBBXXXX (12 bit)

Display Data Write/Read

D/I	/WR	/RD	DB15 ~ DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	Display RAM write in data								
1	1	0	Display RAM read out data								

1. 4,096 Color mode

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
2nd cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1st cycle	X	X	X	X	R3	R2	R1	R0
2nd cycle	G3	G2	G1	G0	B3	B2	B1	B0
3rd cycle	X	X	X	X	R3	R2	R1	R0
4th cycle	G3	G2	G1	G0	B3	B2	B1	B0

2. 256 color mode

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st cycle	R2	R1	R0	G2	G1	G0	B1	B0	R2	R1	R0	G2	G1	G0	B1	B0

(3) 8bit access mode

	7	6	5	4	3	2	1	0
1st cycle	R2	R1	R0	G2	G1	G0	B1	B0

Status Read

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	BSY	X/Y	0	PDM	PT	STB	REV	DP

This instruction indicates the internal status of the S6B33A2.

DP: (0 : Display OFF Status, 1 : Display ON Status)
REV: (0 : Display Image Non-Reversing, 1 : Display Image Reversing)
STB: (0 : Standby Mode OFF Status, 1 : Standby Mode ON Status)
PT: (0 : Partial Display Mode OFF Status, 1 : Partial Display Mode ON Status)
PDM: (0 : Partial Display Mode 0, 1 : Partial Display Mode 1)
X/Y: (0 : Y-address Count Mode, 1 : X-address Count Mode)
BSY: (0 : No Busy, 1 : Busy)

Set Display Data Length

This Instruction is only used in 3-pin SPI MPU interface mode(PS=" L" , MPU[1]=" L"). It consists of two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second and third bytes will be number of data bytes will be write. When DI is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted.
The next byte after the display data string is handled as command data.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	1	0	0
			Number of display data upper 8bits (DDL_H)							
			Number of display data lower 8bits (DDL_L)							

Test Mode1 (FFH)

This Instruction is for testing IC. User is not permitted to access. If access ,have to reset.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	1	1	1

Test Mode2 (FEH)

This Instruction is for testing IC. User is not permitted to access. If access ,have to reset.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	1	1	0

INSTRUCTION PARAMETER

Table 16. Instruction Parameter

Instruction	Hex	Para.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Oscillation Mode Set	02H	1	0	0	0	0	0	0	EXT	OSC
			*	*	*	*	*	*	0	0
Driver Output Mode Set	10H	1	0	0	0	0	0	0	SDIR	SWP
			*	*	*	*	*	*	0	0
DC-DC Set	20H	1	0	0	0	0	0	0	DC(2)	DC(1)
			0	0	0	0	0	0	0	0
PCK Generation Mode Set	24H	1	0	0	DIV(2)		0	0	DIV(1)	
			*	*	1	0	*	*	1	0
DCDC and AMP ON/OFF Set	26H	1	0	0	0	0	AMP	DCDC3	DCDC2	DCDC1
			*	*	*	*	0	0	0	0
Temperature Compensation Set	28H	1	0	0	0	0	0	0	TCS	
			*	*	*	*	*	*	0	0
Contrast Control (1)	2AH	1	Contrast control value in normal and partial display mode0(0 to 255)							
			0	0	0	0	0	0	0	0
Contrast Control(2)	2BH	1	Contrast control value in partial display mode 1(0 to 255)							
			0	0	0	0	0	0	0	0
Addressing Mode Set	30H	1	0	0	GSM	DSG	SGF	SGP		SGM
			*	*	0	0	0	0	0	0
ROW Vector Mode Set	32H	1	0	0	0	0	INC			VEC
			*	*	*	*	0	0	0	0
N-line Inversion Set	34H	1	FIM	FIP	0	N-block Inversion				
			0	0	*	0	0	0	0	0
Red palette Set	38H	8	0	0	0	0	RAM data "000" to GS data			
			0	0	0	0	RAM data "001" to GS data			
			0	0	0	0	RAM data "010" to GS data			
			0	0	0	0	RAM data "011" to GS data			
			0	0	0	0	RAM data "100" to GS data			
			0	0	0	0	RAM data "101" to GS data			
			0	0	0	0	RAM data "110" to GS data			
			0	0	0	0	RAM data "111" to GS data			
Green palette Set	3AH	8	0	0	0	0	RAM data "000" to GS data			
			0	0	0	0	RAM data "001" to GS data			
			0	0	0	0	RAM data "010" to GS data			
			0	0	0	0	RAM data "011" to GS data			
			0	0	0	0	RAM data "100" to GS data			
			0	0	0	0	RAM data "101" to GS data			
			0	0	0	0	RAM data "110" to GS data			
			0	0	0	0	RAM data "111" to GS data			
Blue palette Set	3CH	4	0	0	0	0	RAM data "000" to GS data			
			0	0	0	0	RAM data "001" to GS data			
			0	0	0	0	RAM data "010" to GS data			
			0	0	0	0	RAM data "011" to GS data			
Entry Mode Set	40H	1	0	0	0	0	0	HL	X/Y	RMW
			*	*	*	*	*	0	0	0
X-address Area Set	42H	2	0	X Start address set						
			*	0	0	0	0	0	0	0
			0	X end address set						
			*	1	1	1	1	1	1	1
Y-address Area Set	43H	2	0	Y start address set						
			*	0	0	0	0	0	0	0
			0	Y end address set						
			*	1	1	1	1	1	1	1

Set Display Data Length	FCH	2	Number of display data upper word							
			Number of display data lower word							
Specified Display Pattern Set	53H	1	0	0	0	0	0	0	SDP	
			*	*	*	*	*	*	0	0
Partial Display Mode Set	55H	1	0	0	0	0	0	0	PDM	PT
			*	*	*	*	*	*	0	0
Partial Display Start Line Set	56H	1	0	Partial start line						
			*	0	0	0	0	0	0	0
Partial Display End Line Set	57H	1	0	Partial end line						
			*	0	0	0	0	0	0	0
Area Scroll Mode Set	59H	4	0	0	0	0	0	0	SCM	
			*	*	*	*	*	*	0	0
			0	Scroll area start line						
			*	0	0	0	0	0	0	0
			0	Scroll area end line						
			*	1	1	1	1	1	1	
			0	Lower Fixed number						
			*	0	0	0	0	0	0	0
Scroll Start Line Set	5AH	1	0	Scroll start line						
			*	0	0	0	0	0	0	0

Reset Operation

When /RST becomes "L", following procedure is occurred.

- X address: 0
- Y address: 0
- Display OFF
- Read Modify Write Mode OFF
- Function Mode Set

OSC = 0: Oscillator OFF
EXT = 0: Internal Oscillator Mode
REV = 0: Reversing mode OFF
X/Y = 0: Y-address Count Mode
HL = 0
Standby Mode ON

- PCK Generation mode Set

DIV(1) = 10: fPCK = fOSC/6x
DIV(2) = 10: fPCK = fOSC/6x

- DC-DC Select

DC(1) = 0: X1 step-up
DC(2) = 0: X1 step-up

- DC/DC and AMP ON/OFF Set

AMP =0: Built-in OP-AMP OFF
DCDC1 =0: Built-in 1st booster OFF
DCDC2 =0: Built-in 2nd booster OFF
DCDC3 =0: Built-in 3rd booster OFF

- N-block inversion

FIM =0: Forcing Inversion OFF
FIP =0: Forcing Inversion Period in one frame
N-block inversion = 00H: frame inversion

- Partial Display Mode

PT = 0: Partial Display Mode OFF
PDM = 0: Partial Mode 0

- Partial Display Area Set

Partial start line = 00H
Partial end line = 00H

-Area Scroll Set

Mode = 00H : Entire Display Scroll Mode
Area Start Line: 00H
Area End Line: 7FH
Lower Fixed Line Number: 00H

- Scroll Start Line Set

Scroll Start Line: 00H

- Addressing Mode Set

GSM =0: 4,096 color mode
DSG = 0: Mode 0
SGF = 0: SG Frame Inversion OFF
SGM = 0: SG Reverse Mode OFF
SGP=00:Same phase in all pixel

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage range	VDD	-0.3 to +4.0	V
LCD Supply Voltage range	|VCC – VEE|	20	V
Input Voltage range	Vin	- 0.3 to VDD +0.3	V
Operating Temperature range	TOPR	-30 to +70	°C
Storage Temperature range	TSTR	-55 to +150	°C

OPERATING VOLTAGE

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (1)	VDD	1.8	-	3.3	V
Supply Voltage (2)	2Vr	-	-	20	V
Supply Voltage (3)	VIN	2.4	3.0	3.6	V

DC CHARACTERISTICS (1)

(Vss = 0V, VDD = 1.8 to 3.3V, Ta = -30 to 70 °C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Operating voltage		VDD		1.8	-	3.3	V	VDD
Operating voltage		VIN1		2.4	-	3.6	V	VCI
Operating voltage		DC2IN		1.66	-	2.75	V	DC2IN
Operating voltage		VIN2		2.4	-	5.4	V	VIN2
Operating voltage		VIN45		2.4	-	5.4	V	VIN45
Operating voltage		2Vr	2Vr = |(+VR)- (-VR)|	4.0	-	20	V	+VR, -VR
Driving voltage input range		VM	External power supply mode	1.0		1.65	V	VM
		VCC		7.0		11.55	V	VCC
		VEE		-8.25		-5.0	V	VEE
Input voltage	High	VIH		0.8VDD	-	VDD	V	
	Low	VIL		VSS	-	0.2VDD		
Output voltage	High	VOH	IOH = 0.5mA	0.8VDD	-	VDD	V	
	Low	VOL	IOL = 0.5mA	VSS	-	0.2VDD		
Input leakage current		IIL	VIN = VDD or VSS	-1.0	-	+1.0	µA	
Output leakage current		IOZ	VIN = VDD or VSS	-3.0	-	+3.0	µA	
Oscillator Frequency Tolerance	Normal or Partial 0	FOSC1	R1=? (fFR=80Hz target), DSG=0, 128 display lines	50.688	56.32	61.952	kHz	OSC1 - OSC2
	Partial 1	FOSC2	R1=? (fFR=80Hz target), DSG=0, 66 display lines	26.496	29.44	32.384	kHz	OSC3 - OSC4
Oscillator Frequency Range	Normal or Partial 0	FOSC1	(*1)	35.200		70.400	kHz	OSC1 - OSC2
	Partial 1	FOSC2	(*2)	18.400		36.800	kHz	OSC3 - OSC4
Driving voltage input range		V1 VM		2.0 1.0	-	3.3 1.65	V	

(*1) Minimum oscillator frequency range is defined at fFR=50Hz and display line number=128
Maximum oscillator frequency range is defined at fFR=100Hz and display line number=128
(*2) Minimum oscillator frequency range is defined at fFR=50Hz and display line number=66
Maximum oscillator frequency range is defined at fFR=100Hz and display line number=66

DC CHARACTERISTICS (2)

(Vss = 0V, V_{DD} = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Driver output resistance	SEG	R_{ON-Seg}	V1=3.3 V, VM=1.65V, V0=0V, Ta = 25°C, Iload=100uA	-	1.5	3.0	kΩ	SEGn
	COM	R_{ON-Com}	VCC=12 V, VM=1.5V, VEE=-9.0V, Ta = 25°C, Iload=100uA	-	1.0	1.5	kΩ	COMn
Current consumption	Normal Mode	IDD1	**VDD=3V**					VDD
			VIN1=3.0V, V1=3.3V, Bias(1)=1/6, DC(1)=x1.5, Ta=25°C, Display line=128 DSG=0 (1dummy) f_{OSC1}=49.3kHz (fFR=70Hz) Low current mode, No load, No access, All white pattern	-	400	-	µA	
			VDD=1.8V					
			VIN1=3.0V, V1=3.3V, Bias(1)=1/6, DC(1)=x1.5, Ta=25°C, Display line=128 DSG=0 (1dummy) f_{OSC1}=49.3kHz (fFR=70Hz) Low current mode, No load, No access, All white pattern	-	270	-	µA	
	Partial1 Mode	IDD2	**VDD=3V**					
			VIN1=3.0V, V1=3.3V, Bias(2)=1/6, DC(2)=x1.5, Ta=25°C, Display line=66 DSG=0 (1dummy) f_{OSC1}=25.8kHz (fFR=70Hz) Low current mode, No load, No access, All white pattern	-	240	-	µA	
			VDD=1.8V					
			VIN1=3.0V, V1=3.3V, Bias(2)=1/6, DC(2)=x1.5, Ta=25°C, Display line=66 DSG=0 (1dummy) f_{OSC1}=25.8kHz (fFR=70Hz) Low current mode, No load, No access, All white pattern	-	180	-	µA	

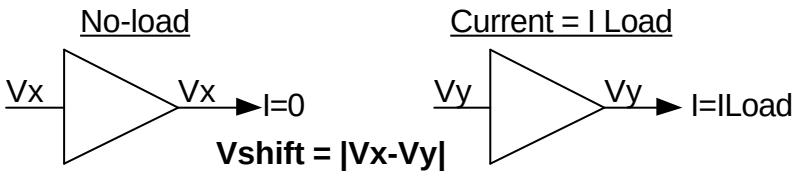
* : " IDD1 and IDD2" are determined from lowest power consumption for dc-dc converter.

DC CHARACTERISTICS (3)

(Vss = 0V, V_{DD} = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Voltage shift range(*1)	Δ (+VR)	Low current mode Isource = 80uA High current mode Isource = 150 or 250uA	-	-	100	mV	+VR
	Δ (V1)	Low current mode Isource = 250uA High current mode Isource = 500 or 1000uA	-	-	20	mV	V1
	Δ (VM)	Low current mode Isource,sink = 250uA High current mode Isource,sink = 500 or 1000uA	-	-	20	mV	VM
	Δ (-VR)	Low current mode Isink = 80uA High current mode Isink = 150 or 250uA	-	-	100	mV	-VR

(*1) Voltage shift means output voltage deference between output current = Iload and no-load.
Refer to the following figure. (in case of source current mode)



Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Tolerance of Bias ratio	Δ (+VR)_0 Δ (-VR)_0(*1)	No load	-100	-	+100	mV	+VR -VR

(*1) Tolerance of bias ratio definition
Δ (+VR)_0 = ((+VR) - VM) – VM *6
Δ (-VR)_0 = (VM - (-VR)) – VM *6

DC CHARACTERISTICS (4)

(Vss = 0V, V_{DD} = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item	Symbol	Condition		Min	Typ	Max	Unit	Remarks
Temperature compensation	ΔVt	VDD=VIN1=V1=3.0V, -20 to 70 °C		-0.02	-	+0.02	%/°C	V1
Tolerance of Contrast step of V1	ΔVstep			2.539	5.078	7.617	mV	V1
Voltage range	ΔV1 ΔVM	Contrast set = FFh	V1	3.25	3.3	3.35	V	V1
			VM	1.60	1.65	1.70	V	VM
		Contrast set = 00h	V1	1.95	2.00	2.05	V	V1
			VM	0.95	1.00	1.05	V	VM

Item			Condition		Max	Unit	Ref
			Load current	Voltage range			
Offset Voltage	||+VR-VM| -|VM -(-VR)||		I Load = +100uA (+VR) I Load = -100uA (-VR)	+VR=7.0~11.55 V V1=2.0~3.3V VM=1.0~1.65V -VR=-8.25~-5 V	100	mV	Fig.1
	||V1-VM| -|VM-V0||	A	I Load = +100uA (V1, VM)		50	mV	Fig.2
		B	I Load = +100uA (+VR) I Load = -100uA (-VR)				

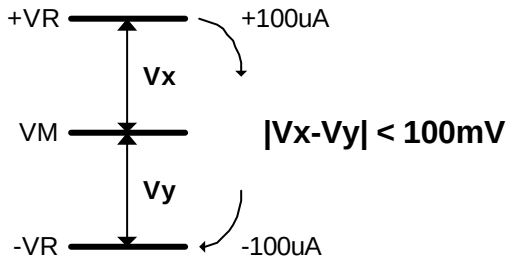


Fig. 1: Offset voltage definition (+VR,VM,-VR)

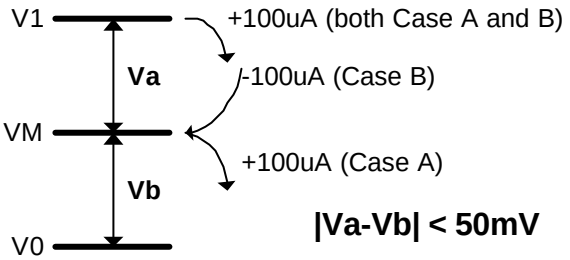


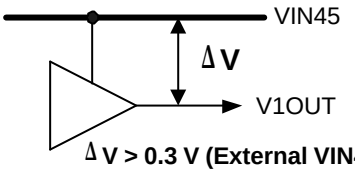
Fig. 2: Offset voltage definition (V1,VM,V0)

DC CHARACTERISTICS (5)

(Vss = 0V, V_{DD} = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item		Range	
		Min	Max (DC(1) and DC(2) = X1.5)
Voltage Level	V1OUT	2.0 V	3.3 V(*1)
	VMOUT	1.0 V	1.65 V(*2)
	DC2OUT	1.67 V	2.75 V(*3)

(*1) This definition is shown as below



ΔV > 0.3 V (External VIN45)

ΔV > 0.5 V (VIN45 = VOUT45)

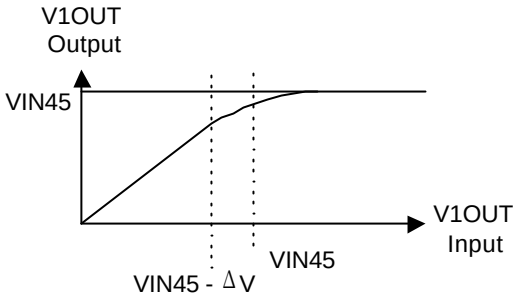
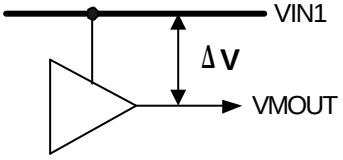


Fig. 1

If V1OUT input voltage is set over VIN45, V1OUT output voltage must be clipped near VIN45. In this case, V1OUT output level must not be unstable. Refer to Fig.1

(*2) This definition is shown as below



ΔV > 0.3 V

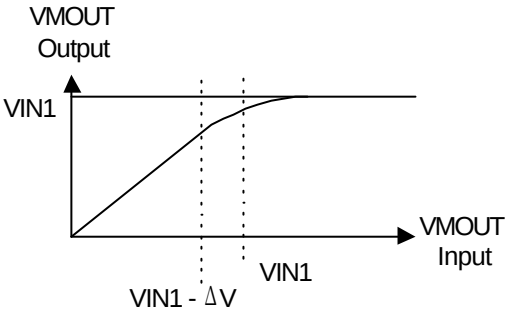
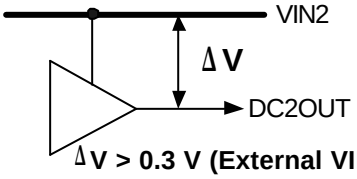


Fig. 2

If VMOUT input voltage is set over VIN1, VMOUT output voltage must be clipped near VIN1. In this case, VMOUT output level must not be unstable. Refer to Fig.2

(*3) This definition is shown as below



ΔV > 0.3 V (External VIN2)

ΔV > 0.5 V (VIN2 = VOUT45)

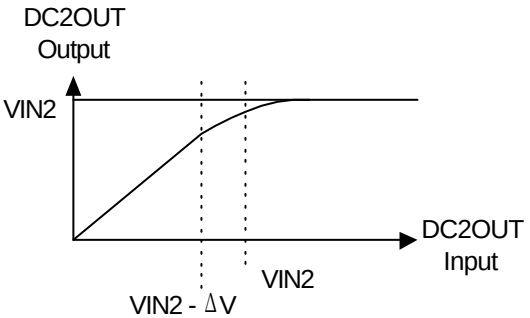
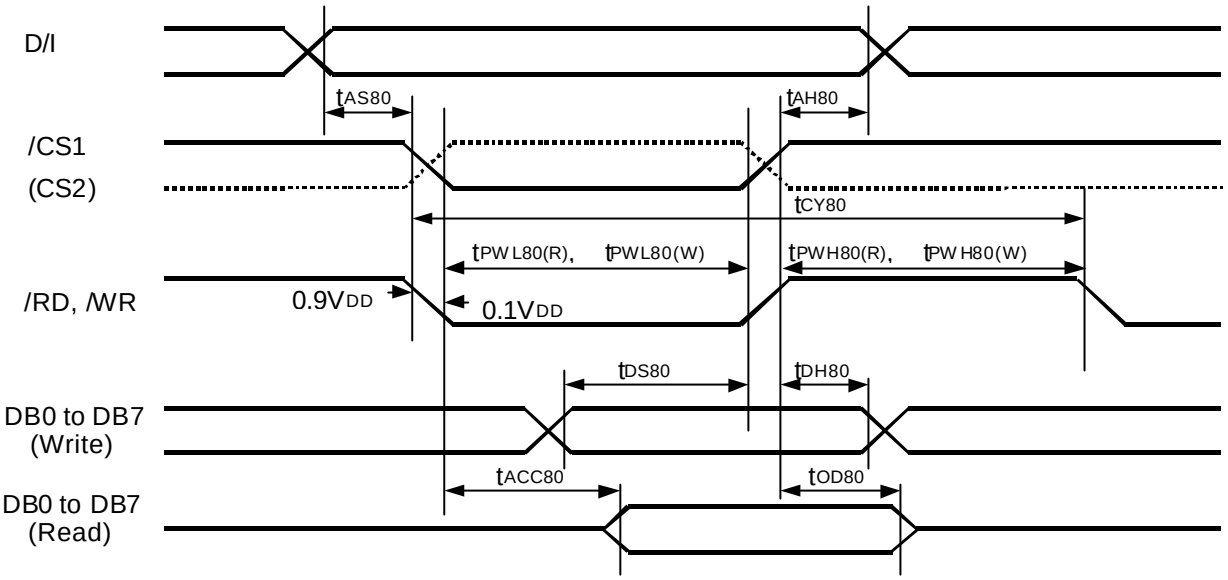


Fig.3

If DC2OUT input voltage is set over VIN2, DC2OUT output voltage must be clipped near VIN2. In this case, VMOUT output level must not be unstable. Refer to Fig.3

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)



** $t_{PWL80(W)}$ and $t_{PWL80(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and /WR(/RD) is low.

Figure 27. Parallel Interface (8080-series MPU) Timing Diagram

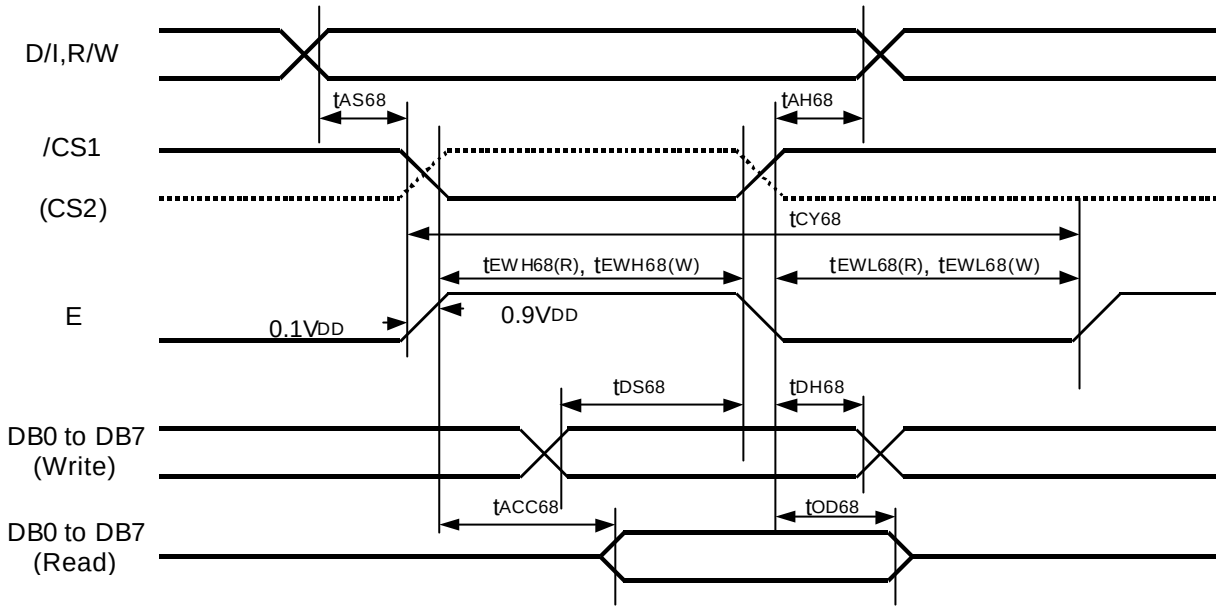
Table 17. AC Characteristics (8080-series Parallel Mode)

(VDD = 1.8 to 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	D/I	t_{AS80} t_{AH80}	1.8V/3.3V	0	- -	ns
			1.8V/3.3V	0		
System cycle time		t_{CY80}	1.8V	470	-	ns
			3.3V	180		
Pulse width low for write Pulse width High for write	/WR (/WR)	t_{PWLW} t_{PWHW}	1.8V	160	- -	ns
			3.3V	70		
Pulse width low for read Pulse width high for read	/RD (/RD)	t_{PWLR} t_{PWHR}	1.8V	160	- -	ns
			3.3V	70		
Data setup time Data hold time	DB0 to DB15	t_{DS80} t_{DH80}	1.8V/3.3V	70/35	- -	ns
			1.8V/3.3V	15/10		
Read access time Output disable time		t_{ACC80} t_{OD80}	1.8V/3.3V	170/90	-	ns
			C_L = 100 pF	-		

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 10 ns or less.
(tr + tf) < (t_{CY80} - t_{PWLW} - t_{PWHW}) for write, (tr + tf) < (t_{CY80} - t_{PWLR} - t_{PWHR}) for read

Read / Write Characteristics (6800-series Microprocessor)



** $t_{EWH68(W)}$ and $t_{EWH68(R)}$ is specified in the overlapped period when /CS1 is low (CS2 is high) and E is high.

Figure 28. Parallel Interface (6800-series MPU) Timing Diagram

Table 18. AC Characteristics (6800-series Parallel Mode)

(V_{DD} = 1.8 to 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	D/I R/W	t_{AS68} t_{AH68}	1.8V/3.3V	0	- -	ns
			1.8V/3.3V	0		
System cycle time		t_{CY68}	1.8V	470	- -	ns
			3.3V	180		
Enable width high for write Enable width low for write	/RD (E)	t_{EWHW} t_{EWLW}	1.8V	160	- -	ns
			3.3V	70		
Enable width high for read Enable width low for read	/RD (E)	t_{EWHR} t_{EWLR}	1.8V	160	- -	ns
			3.3V	70		
Data setup time Data hold time	DB0 to DB15	t_{DS68} t_{DH68}	1.8V/3.3V	70/35	- -	ns
			1.8V/3.3V	15/10		
Read access time Output disable time		T_{ACC68} t_{OD68}	1.8V/3.3V	170/90	- -	ns
			C_L = 100 pF	-		

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 10 ns or less.
(tr + tf) < (t_{CY68} - t_{EWHW} - t_{EWLW}) for write, (tr + tf) < (t_{CY68} - t_{EWHR} - t_{EWLR}) for read

Serial Data Interface Timing

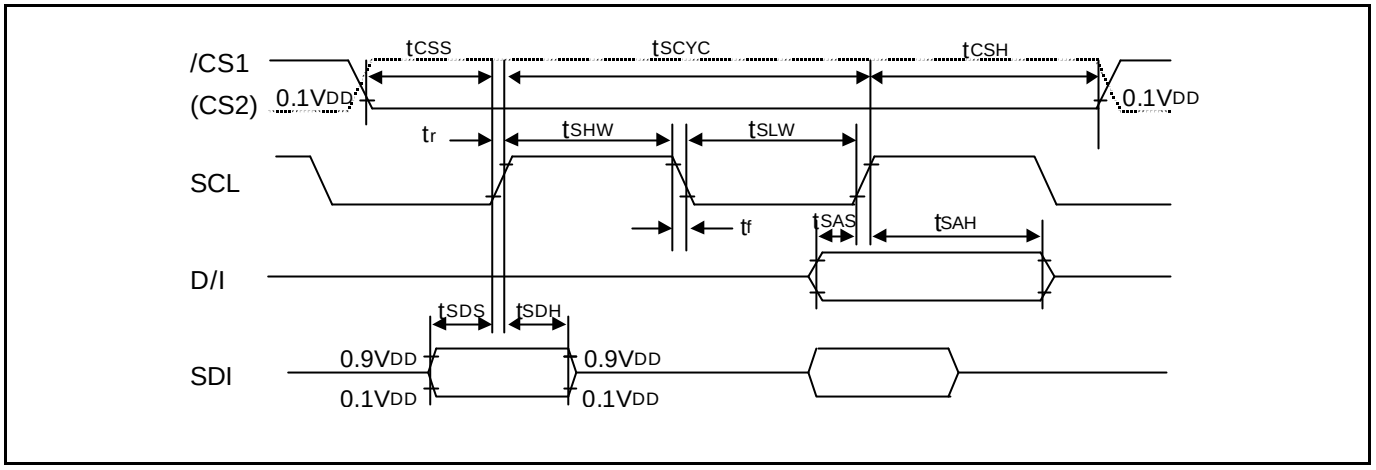


Table 19. Serial Data Interface Timing

(V_{DD} = 1.8 to 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
SCL Cycle Time	SCL	t_{CSC}		50		us
SCL High Pulse Width	SCL	t_{SHW}		20		ns
SCL Low Pulse Width	SCL	t_{SLW}		20		ns
SDI Setup time	SDI	t_{SDS}		20		ns
SDI Hold time	SDI	t_{SDH}		20		ns
D/I Setup time	D/I	t_{SAS}		20		ns
D/I Hold time	D/I	t_{SAH}		20		ns
Chip Select Setup time	/CS1 (CS2)	t_{CSS}		20		ns
Chip Select Hold time	/CS1 (CS2)	t_{CHS}		20		ns

Reset Input Timing

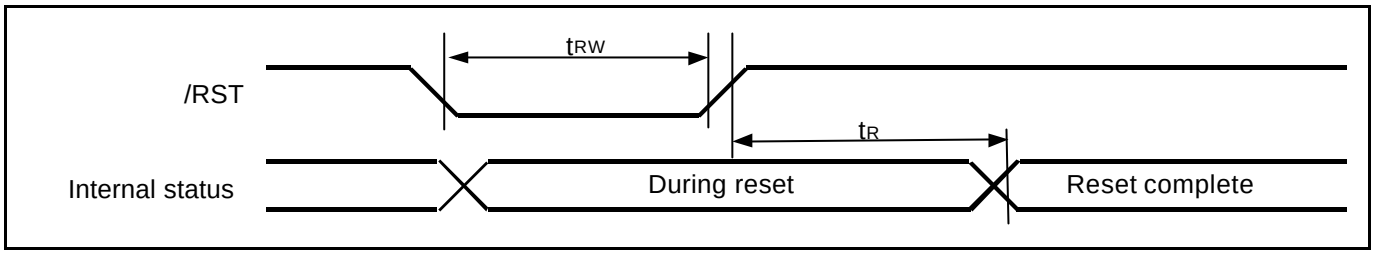


Figure 29. Reset Input Timing Diagram

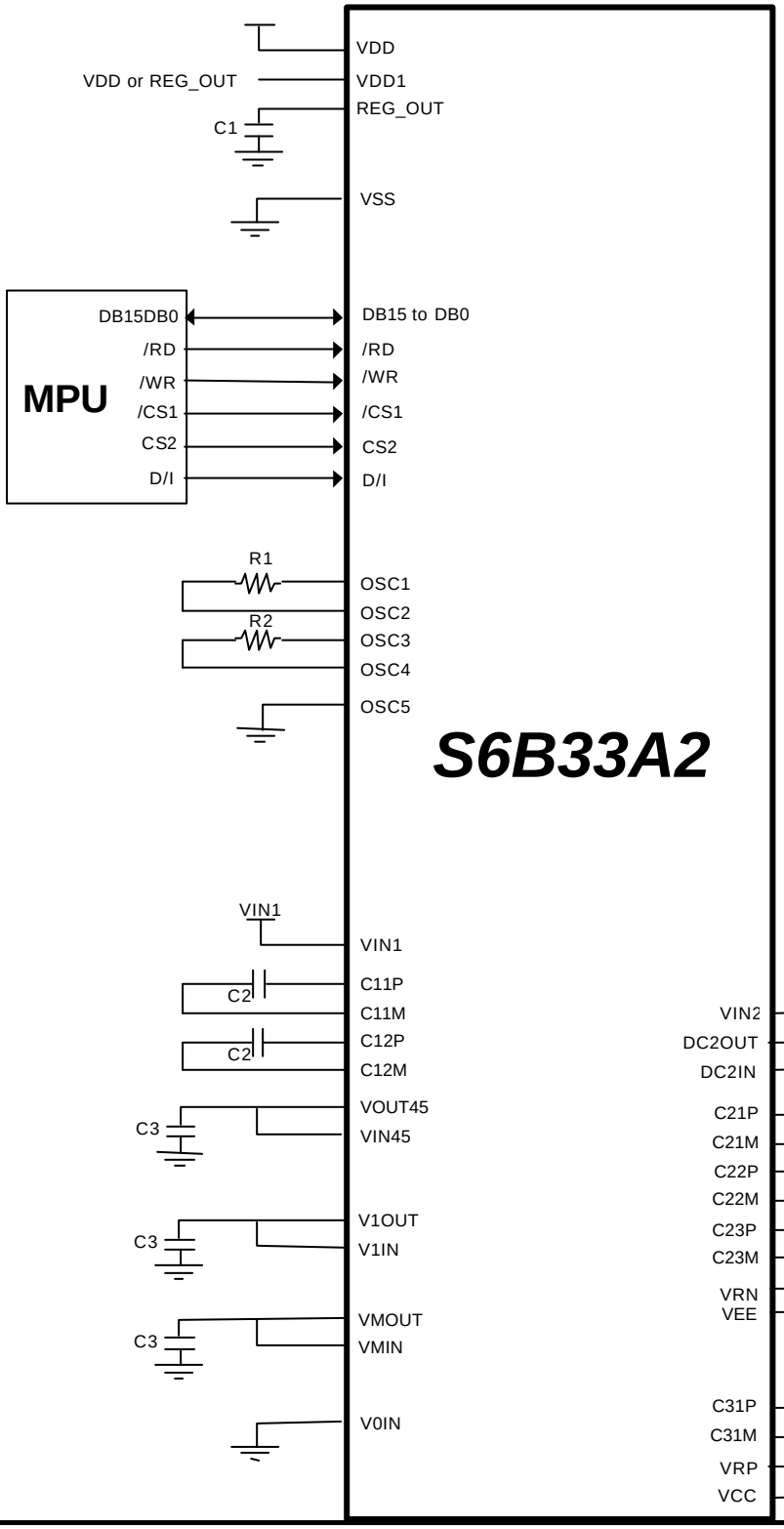
Table 20. AC Characteristics (Reset mode)

(V_{DD} = 1.8 to 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	/RST	t_{RW}		1000	-	ns
Reset time	-	t_R		-	1000	ns

SYSTEM APPLICATION DIAGRAM

Internal Power Mode



External Components

Name	Device
R1,R2	Resistors
C1,C2,C3	Capacitors
D1	Schottky barrier diode

Values of external Capacitors and D1

Item	Capacitance
C1	1.0 to 4.7µF
C2	1.0 to 2.2µF
C3	1.0 to 2.2µF
D1	Vforward = Max. 0.3V at 1mA Vreverse = Min. 15V

Maximum rating voltage of capacitors

Item	Maximum rating voltage
REG_OUT to VSS	3V
VOUT45 to VSS	8V
C11P to C11M	6V
C12P to C12M	6V
VMOUT to VSS	3V
DC2OUT to VSS	5V
V1OUT to VSS	6V
C21P to C21M	5V
C22P to C22M	10V
C23P to C23M	13V
VSS to VRN	13V
C31P to C31M	17V
VRP to VSS	18V

External Power Mode