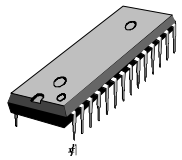
I²C BUS CONTROLLED R/G/B VIDEO AMPLIFIER

32-DIP-600A



The S1D2503X01-D0B0 is a very high frequency video amplifier system with I²C bus control used in monitors with high resolution up to 1600 × 1200.

It contains 3 matched R/G/B video amplifiers with OSD interface and provides flexible interfacing to I²C bus controlled adjustment systems.

FUNCTIONS

- I²C bus controlled 200MHz RGB video pre-amplifier for monitors
- The S1D2503X01-D0B0 is a very high frequency video amplifier system with OSD interface controlled by I²C bus.
- All controls and adjustments are digitally performed thanks to I²C bus.
  : Contrast, brightness and DC output level of R/G/B signals common to the 3-channel and drive adjustment (sub contrast), cut-off control (AC or DC coupling by CT bit) is separated for each channel.
- The S1D2503X01-D0B0 is included video & OSD half tone function.
- The white blance adjustment is effective on brightness, video & OSD signals.
- The S1D2503X01-D0B0 works for application using AC or DC coupled CRT driver.
- In addition to beam current limitation (ABL), OSD intensity interface and brightness uniformity (BU) interface are possible with external pins.

ORDERING INFORMATION

Device	Package	Operating Temperature
S1D2503X01-D0B0	32-DIP-600A	-25 °C — +80°C

FEATURES

- 3-channel matched R/G/B Video Amplifier
- I²C BUS control items
  - Contrast control
  - Brightness control
  - SUB contrast control for each channel
  - OSD contrast control
  - Cut-off control for each channel
  - Brightness control for cut-off
  - Switch registers for SBLK, half tone, cut-off INT/EXT, BPS (Blank Pulse Input Polarity Selection) and CPS (Clamp Pulse Input Polarity Selection).
- Built in clamp gate with anti OSD sagging
- Built in OSD Interface, OSD BLK
- Built in OSD Intensity Interface
- Built in ABL (Automatic Beam Limitation)
- Built in video input clamp, BRT clamp
- Built in video & OSD half tone function on OSD picture (OSD raster 8 colors and 3 raster selection by HR/G/B)
- Built in smooth video contrast control with external capacitor.
- 3-channel R/G/B video amplifier 200MHz @f-3dB
- TTL OSD inputs, 80MHz bandwidth
- Contrast control range: 38dB
- SUB contrast control range: 11dB
- OSD contrast control range: 38dB
- Capable of 7Vp-p output swing
- High speed OSD BLK

BLOCK DIAGRAM

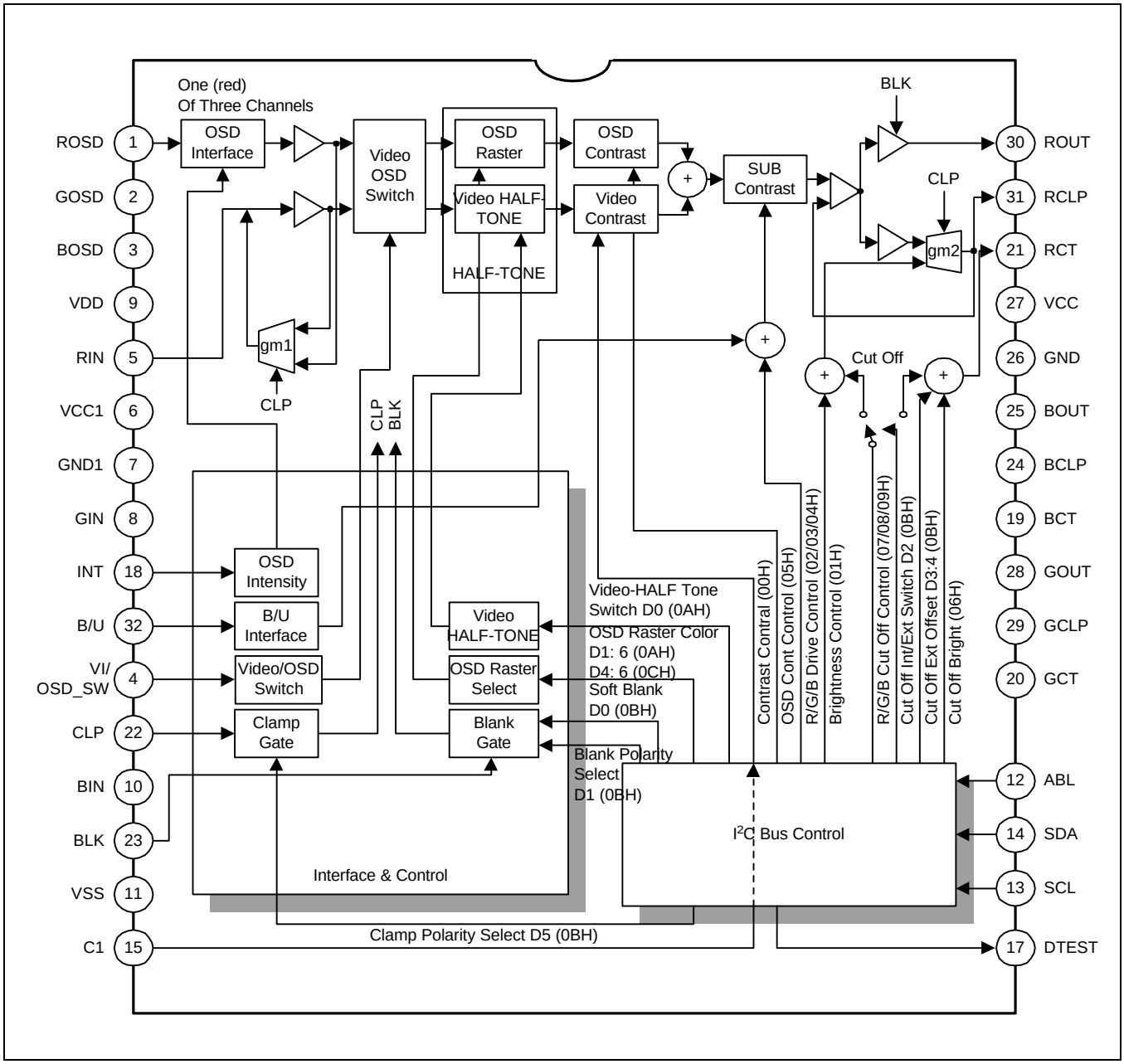


Figure 1. Block Diagram

PIN CONFIGURATION

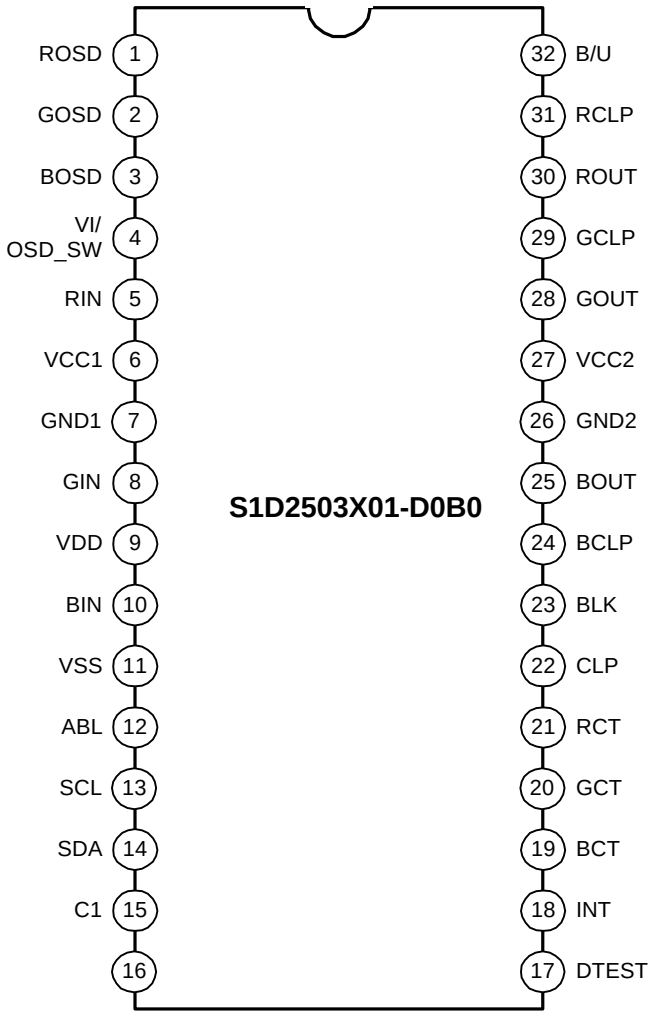


Figure 2. Pin Configuration

Table 1. Pin Configuration (continued)

Pin No	Symbol	I/O	Configuration
1	ROSD	I	Red OSD input
2	GOSD	I	Green OSD input
3	BOSD	I	Blue OSD input
4	VI/OSD_SW	I	Video or OSD switch
5	RIN	I	Red video input
6	VCC1	-	VCC (normal)
7	GND1	-	Ground1 (normal)
8	GIN	I	Green video input
9	VDD	-	VDD (logic)
10	BIN	I	Blue video input
11	VSS	-	Ground (logic)
12	ABL	I	Automatic beam limit
13	SCL	I/O	Serial clock
14	SDA	I/O	Serial data
15	C1	-	Contrast cap
16	-	-	-
17	DTEST	-	-
18	INT	-	OSD intensity
19	BCT	I	Blue cut off control
20	GCT	I	Green cut off control
21	RCT	I	Red cut off control
22	CLP	I	Clamp gate signal input
23	BLK	I	Blank gate signal input
24	BCLP	-	Blue clamp cap
25	BOUT	O	Blue video output
26	GND2	-	Ground2 (drive part)
27	VCC2	-	VCC (drive part)
28	GOUT	O	Green video output
29	GCLP	-	Green clamp cap
30	ROUT	O	Red video output
31	RCLP	-	Red clamp cap
32	B/U	I	Brightness uniformity

PIN DESCRIPTION

Table 2. Pin Description

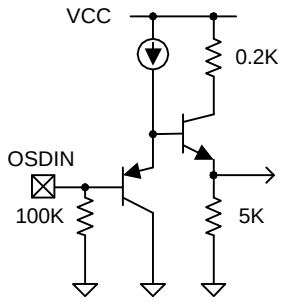
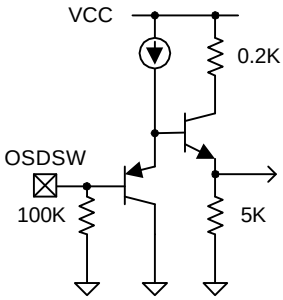
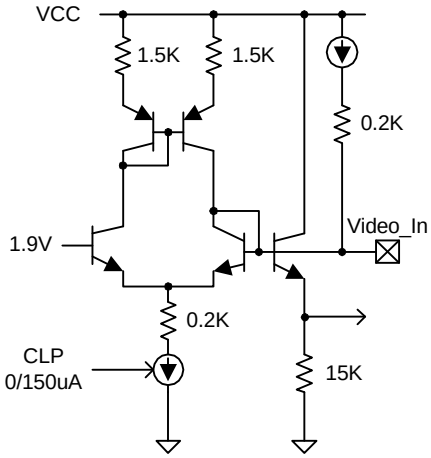
Pin No	Pin Name	Schematic	Description
1 2 3	Red OSD input (ROSD) Green OSD input (GOSD) Blue OSD input (BOSD)		OSD input signals are in TTL level and will be connected to ground when switching to video input
4	Video/OSD switch (VI/OSD_SW)		Video/OSD signal is switched by pin4 DC level PIN4 = "High", OSD input PIN4 = "Low", video input **Pin4 / Output** High / OSD Low / Video
5 8 10	Red video input (RIN) Green video input (GIN) Blue video input (BIN)		MAX input video signal is 0.7Vpp
6	VCC1	-	Normal power supply (12V)
7	GND1	-	Normal ground
9	VDD	-	Logic power supply (5V)
11	VSS	-	Logic ground

Table 2. Pin Description (Continued)

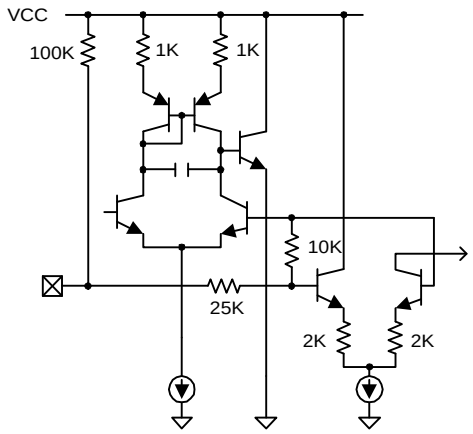
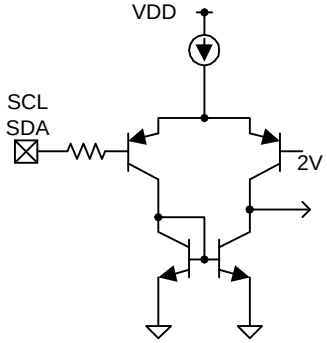
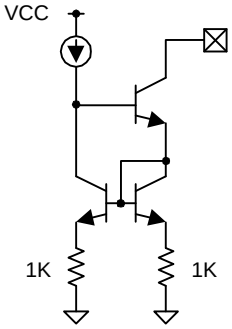
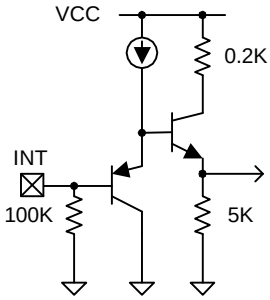
Pin No	Pin Name	Schematic	Description
12	ABL		Auto beam limitation input (control range: 0.5 — 4.5V)
13 14	Serial clock input (SCL) Serial data input (SDA)		SCL, SDA for I²C bus control
15	Contrast cap1	-	External contrast cap pin
17	DAC test pin		DAC current (0 - 500uA)

Table 2. Pin Description (Continued)

<table>
<tr><th>Pin No</th><th>Pin Name</th><th>Schematic</th><th>Description</th></tr>
<tr><td>18</td><td>OSD intensity input (INT)</td><td> 
</td><td>Active high</td></tr>
<tr><td>19

20

21</td><td>Blue cut-off control (BCT)

Green cut-off control (GCT)

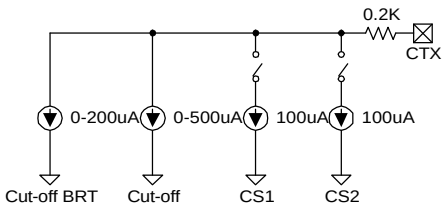
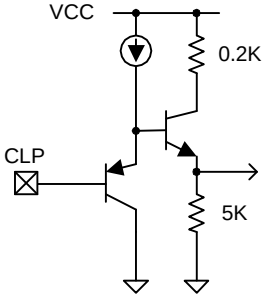
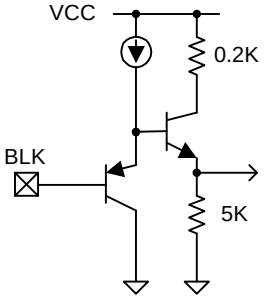
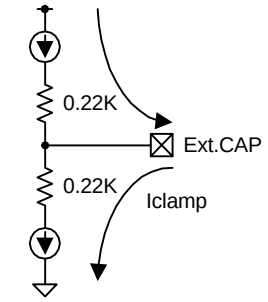
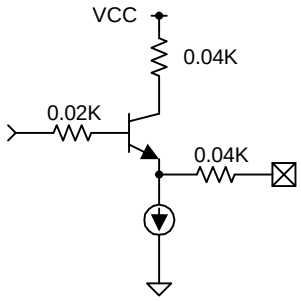
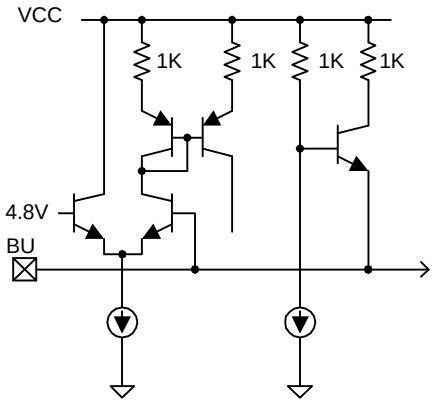
Red cut-off control (RCT)</td><td> 
</td><td>Cut-off control output</td></tr>
<tr><td>22</td><td>Clamp gate input (CLP)</td><td> 
</td><td>Video amp active when clamp gate signal is in low TTL level.
<table><tr><th>CPS Bit</th><th>CLP Signal</th></tr><tr><td>0</td><td>Low</td></tr><tr><td>1</td><td>High</td></tr></table>
Clamp gate min. pulse width
: 0.2us, at fh: 50kHz
  </td></tr>
<tr><td>23</td><td>Blank gate input (BLK)</td><td> 
</td><td>Video amp blanks video signal when blank gate signal is in low TTL level.
<table><tr><th>BPS Bit</th><th>BLK Signal</th></tr><tr><td>0</td><td>Low</td></tr><tr><td>1</td><td>High</td></tr></table></td></tr>
</table>

Table 2. Pin Description (Continued)

Pin No	Pin Name	Schematic	Description
31 29 24	Red clamp cap (RCLP) Green clamp cap (GCLP) Blue clamp cap (BCLP)		Brightness control activated by charging and discharging of the external cap. (0.1μF) (During clamp gate)
30 28 25	Red video output (ROUT) Green video output (GOUT) Blue video output (BOUT)		Video signal output
26	GND2	-	Drive ground
27	VCC2	-	Drive power supply (12V)
32	Brightness uniformity (BU)		BU interface input

ABSOLUTE MAXIMUM RATING (TA = 25 °C) (see 1)

Table 3. Absolute Maximum Rating

No	Item	Symbol	Value			Unit
			Min	Typ	Max	
1	Maximum supply voltage	V_{CC}1/2	-	-	13.2	V
2	Operating temperature (see 2)	Topr	-25	-	80	°C
3	Storage temperature	Tstg	-65	-	150	°C
4	Operating supply voltage	Vccop	11.4	12.0	12.6	V (see 3)
5	Power dissipation	P_D	-	-	1.38	W
6	Logic part power supply	V_{DD}	-	-	5.5	V

THERMAL & ESD PARAMETER

Table 4. Thermal & ESD Parameter

No	Item	Symbol	Value			Unit
			Min	Typ	Max	
1	Thermal resistance (junction-ambient)	θja	-	50	-	°C/W
2	Junction temperature	Tj	-	149	-	°C
3	Human body mode (C = 100p, R = 1.5k)	HBM	±2	-	-	KV
4	Machine model (C = 200p, R = 0)	MM	±300	-	-	V
5	Charge device model	CDM	±800	-	-	V

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

Ta = 25 °C, V_{CC1} = V_{CC2} = 12V; V_{DD} = 5V; Pin1, 2, 3, 4 = 0V; Pin22 4V; Pin18, 32 = 0V; POR; unless otherwise stated

Table 5. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{CC} (see 4)		80	110	140	mA
Maximum supply current	ICCmax	$V_{CC1, 2}$ = 15V	100	140	180	mA
Video input bias voltage	Vbias		1.6	1.9	2.2	V
Clamp gate low input voltage	V22L	P_{22} = 4V → 0V	1.0	1.5	2.0	V
Clamp gate high input voltage	V22H	P_{22} = 0V → 4V	1.0	1.5	2.0	V
Clamp gate low input current	I22L		-8	-4	-	uA
Clamp gate high input current	I22H	P_{22} = 12V	-	3	6	uA
Clamp cap charge current	Iclamp+	$P_{24, 29, 31}$ = 4V	0.4	0.8	1.2	mA
Clamp cap discharge current	Iclamp-	$P_{24, 29, 31}$ = 8V	-1.2	-0.8	-0.4	mA
Blank gate low input voltage	V23L	P_{23} = 4V → 0V	1.0	1.5	2.0	V
Blank gate high input voltage	V23H	P_{23} = 0V → 4V	1.0	1.5	2.0	V
Blank gate low input current	I23L	P_{23} = 0V	-8	-4	-	uA
Blank gate high input current	I23H	P_{23} = 12V	-	3	6	uA
BRT output voltage (POR)	VOpor	P_{22} = S8 (pulse width 0.2us/38kHz)	0.9	1.4	1.9	uA
Black level voltage channel difference	ΔVO_{BL} (see 5)		-0.3	-	0.3	V
Clamp cap high voltage	V_CLP	$V_{CC1, 2}$ = 15V	8	10	12	V
Video output high voltage	VOH	P_{22} = 4V	6.2	7.5	9	V
Video blank output voltage	VOB		-	0.1	0.2	V
SCL high input current	I13H		-	0.01	1	uA
SDA high input current	I14H		-	0.01	1	uA
SCL/SDA low level input voltage	VbusL	OB: O/H, SCL/SDT signal high = 3.5V, low = 1.5V	-	-	1.5	V
SCL/SDA high level input voltage	VbusH		3.5	-	-	V
SCL/SDA input pin ref. voltage	VbusR	$P_{13, 14}$ = open status	1.5	2.0	2.5	V
Video input resistance	VIDEOin		10	100	-	kΩ
Spot killer voltage	Vspot	$V_{CC1, 2}$ = 12 → 9V	9.2	10.4	11.2	V
POR ext. cut-off output current	IctXpo		150	250	350	uA
Cut-off min. output voltage difference	ΔVcutmin	ΔVcutmin = Vout [07, 08, 09: 00H] - Vout [POR]	-0.6	-0.4	-0.2	V
Cut-off max. output voltage difference	ΔVcutmax	ΔVcutmax = Vout [07, 08, 09: FFH] - Vout [POR]	0.2	0.4	0.6	V

Table 5. DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Ext. cut-off output current range	ΔIctx	OB: 04H, $P_{19, 20, 21}$ = 5V, ΔIctx = P20's I [07, 08, 09: FFH] - P20's I [07, 08, 09: 00H]	330	480	630	uA
Cut-off BRT output current range	ΔIctbrt	OB: 04H, $P_{19, 20, 21}$ = 5V, ΔIctbrt = P20's I [06:FFH] - P20's I [06:00H]	130	200	330	uA
Ext. cut-off offset output current1	Ics1	OB: 04H, $P_{19, 20, 21}$ = 5V, 06 - 09: 00H, CS1 bit = 1	60	90	120	uA
Ext. cut-off offset output current2	Ics2	OB: 04H, $P_{19, 20, 21}$ = 5V, 06 - 09: 00H, CS2 bit = 1	60	90	120	uA
Video soft blank output voltage	VOsoft	OB: 01H	-	0.1	0.2	V
Wrong slave address det.	WSADDR	OB: 01H, when wrong slave address is inputted you must measure voltage.	0.9	1.4	1.9	V
Blank polarity selector voltage	VBPS	OB: 02H	-	0.1	0.2	V
Clamp polarity selector voltage	VCPS	OB: 20H	0.9	1.4	1.9	V
Video brightness low output voltage	VOBL	01: 00H	-	0.1	0.2	V
Video output worst low output	VLOW		-0.2	-	0.2	V
Video brightness high output voltage	VOBH	01: FFH	2.2	2.8	3.4	V
BU input bias voltage	VBU	01: 80H	4	4.8	5.6	V

AC ELECTRICAL CHARACTERISTICS

Ta = 25 °C, V_{CC1} = V_{CC2} = 12V; V_{DD} = 5V; Pin1, 2, 3, 4 = 0V; Pin5, 8, 10 = S1; Pin23 = 4V; Pin22 = S8; Pin18, 32 = 0V; POR.
Vin = 0.56Vpp manually adjust video output pins 25, 28 and 30 to 4V DC for the AC test (see 11) unless otherwise stated (see 12)

Table 6. AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video bandwidth (see 7,8)	f -3dB	$P_{5, 8, 10}$ = S2, 00, 02, 03, 04 = FFH When P_{22} = 0V, you must measure clamp cap pin voltage. Then P_{22} = 4V, P_8 = 2.2V, clamp cap pin = above measurement voltage.	200	250	-	MHz
Video amp gain	AVmax	P_{22} = S8 (low: 0.5V, high: 3V) 00, 02, 03, 04 = FFH	15.5	17.5	19.5	dB
Max. gain channel difference	ΔAVmax (see 6,7)	AVmax = 20log (Vout / Vin) ΔAVmax =20log (Voutch1 / Vontch2)	-1	-	1	dB
Low gain channel difference	ΔAVlow (see 6,7)	P_{22} = S8 (low: 0.5V, high: 3V), 00 = 40H, 02, 03, 04 = FFH ΔAVlow = 20log (Voutch1 / Voutch2)	-1	-	1	dB
Sub drive ctrl max-center	AVDmax	AVDmax = 20log (Vout [02, 03, 04: 80H]/ Vout [02, 03, 04: FFH])	-5	-4	-3	dB
Sub drive ctrl min-center	AVDmin	AVDmin = 20log (Vout [02, 03, 04: 00H]/ Vout [02, 03, 04: 80H])	-11	-8	-5	dB
Contrast ctrl max-center	AVCmax	AVCmax = 20log (Vout [02, 03, 04: 80H]/ Vout [02, 03, 04: FFH])	-7.5	-6	-4.5	dB
Contrast ctrl min-center	AVCmin	AVCmin = 20log (Vout [00:00H] / Vout [00, 02, 03, 04: 80H])	-	-	-35	dB
ABL control range	ΔABL	00, 02, 03, 04 = FFH, ΔABL = 20log (Vlow [P12 = 0.5V] / Vmax [P12 = 5V])	-14.5	-11.5	-8.5	dB
BU modulation ratio1	BU1	P_{32} = S9	6	12	18	%
BU modulation ratio2	BU2		18	24	30	%
Video amp THD	THD	$P_{5, 8, 10}$ = S5, P22 = 4V, $P_{24, 29, 31}$ = Var.	-	1	5	%
Video rising time (see 7)	tr	$P_{5, 8, 10}$ = S6, $P_{24, 29, 31}$ = Var.	-	1.4	1.8	nS
Video falling time (see 7)	tf		-	1.4	1.8	nS
Blank output rising time (see 7)	trBlank	P_{22} = 0V, P_{23} = S7	-	3	10	nS
Blank output falling time (see 7)	tfBlank		-	5	12	nS
Blank rising prop. delay	trBlankPr		-	25	35	nS
Blank falling prop. delay	tfBlankPr		-	15	25	nS
Video output channel crosstalk 10kHz	CT_10K (see 9)	P_5 = S3, P_{22} = 4V, 00, 02, 03, 04: FFH	-	-65	-45	dB
Video output channel crosstalk 10MHz	CT_10M (see 7,9)	When P_{22} = 0V, you must measure clamp cap pin voltage. Then P_{22} = 4V, video input pin = 2.2V DC bias, clamp cap pin = above measurement voltage CT-10K = 20log (Voutch2 / Voutch2 [AVmax Vout])	-	-50	-35	dB

OSD ELECTRICAL CHARACTERISTICS

Ta = 25 °C, $V_{CC1} = V_{CC2} = 12V$; $V_{DD} = 5V$;

Pin1, 2, 3, 4 = 4V; Pin23 = 4V; Pin12, 18, 22, 32 = 0V; POR; unless otherwise stated

Table 7. OSD Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OSD low input voltage	$V_{OSD}L$	P_4 = S7, $P_{1, 2, 3}$ = 4V → 0V	2.0	2.5	3.0	V
OSD high input voltage	$V_{OSD}H$	P_4 = S7, $P_{1, 2, 3}$ = 0V → 4V	2.0	2.5	3.0	V
OSD select low input voltage	VosdsL	P_4 = S7 (S7's level 5Vpp → 0Vpp)	2.0	2.5	3.0	V
OSD select high input voltage	VosdsH	P_4 = S7 (S7's level 0Vpp → 5Vpp)	2.0	2.5	3.0	V
OSD output voltage	Vosd	$P_{1, 2, 3}$ = 3V, P_4 = S7, 05: FFH	2.6	3.6	4.6	V_{PP}
OSD gain channel difference	ΔVosd	$P_{1, 2, 3}$ = 3V, P_4 = S7, 05: FF, ΔVosd = Vosdch1 - Vosdch2	-300	-	300	mVpp
OSD attenuation	Vosdatt	$P_{1, 2, 3}$ = 3V, P_4 + S7, Vosdatt = Vosd [05:80H] / Vosd [05:FFH] × 100	30	50	70	%
OSD low gain channel difference	ΔVosdL	$P_{1, 2, 3}$ = 3V, P_4 + S7, ΔVosdL = Vosdch1 [05:80H] - Vosdch2 [05:80H]	-300	-	300	mVpp
Video/OSD switch time	tr (OSD-s)	P_4 = S7, P_{22} = S8	-	4	10	nS
OSD/video switch time	tf (OSD-s)		-	4	10	nS
Video/OSD prop. delay	tr-prop (OSD-s)		-	5	15	nS
OSD/video prop. delay	tf-prop (OSD-s)		-	10	20	nS
OSD rising time	trOSD	$P_{1, 2, 3}$ = S7, $P_{4, 22}$ = S8	-	4	8	nS
OSD falling time	tfOSD		-	4	8	nS
OSD rising prop. delay	tr-prop		-	5	15	nS
OSD falling prop. delay	tf-prop		-	5	15	nS
Video/OSD 10MHz crosstalk	CTVi/OSD-10M	$P_{1, 2, 3}$ = none, $P_{5, 8, 10}$ = S4, P_{22} = S8, 00, 02, 03, 04, 05: FFH) CTVs/OSD-10M = 20log (Vout [P_4 = S8] / Vout [P_4 = 0V])	-	-50	-35	dB
R OSD HT attenuation (blue)	VHTblueR	$P_{1, 2, 3}$ = 4V, P_4 = S7, P_{22} = S8, 05: FFH VHTblue = Vout [04:41H] / Vout [04:00H] × 100	80	100	120	%
G OSD HT attenuation (blue)	VHTblueG		80	100	120	%
B OSD HT attenuation (blue)	VHTblueB		30	50	70	%
R OSD HT attenuation (white)	VHTwhiteR	$P_{1, 2, 3}$ = 4V, P_4 = S7, P_{22} = S8, 05: FFH VHTwhite = Vout [04:48H] / Vout [04:00H] × 100	30	50	70	%
G OSD HT attenuation (white)	VHTwhiteG		30	50	70	%
B OSD HT attenuation (white)	VHTwhiteB		30	50	70	%
OSD intensity attenuation	Vintatt	P_4 = S7, P_{22} = S8, 05: FFH, OA: 00H Vintatt = Vout [P_{18} = 0V] / Vout [P_{18} = 3V] × 100	30	50	70	%
OSD contrast low output	V_{OCL}	P_4 = S7, P_{22} = S8, 05: 00H, $V_{CC1, 2}$: 15V V1 = 4V, $P_{2, 3}$ = 0V, P_4 = S7, P_{22} = S8, 00, 02, 03, 04, 05: FFH	-	-	0.2	Vpp
OSD output channel crosstalk	V_{OSDCT}		-0.3	-	0.3	Vpp

I²C BUS RECOMMENDED OPERATING CONDITIONS

Table 8. I²C BUS Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input high level voltage	VinH	3.0	-	-	V
Input low level voltage	VinL	-	-	1.5	V
SCL clock frequency	f_{SCL}	-	-	200	kHz
Hold time before a new transmission can start	t_{BUF}	1.3	-	-	uS
Hold time for start condition	t_{HDS}	0.6	-	-	uS
Set-up time for stop conditions	t_{SUP}	0.6	-	-	uS
The low period of SCL	t_{LOW}	1.3	-	-	uS
The high period of SCL	t_{HIGH}	0.6	-	-	uS
Hold time data	t_{HDAT}	0.3	-	-	uS
Set-up time data	t_{SUPDAT}	0.25	-	-	uS
Rise time of SCL	t_R	-	-	1.0	uS
Fall time of SCL	t_F	-	-	3.0	uS

I²C BUS TIMING REQUIREMENT

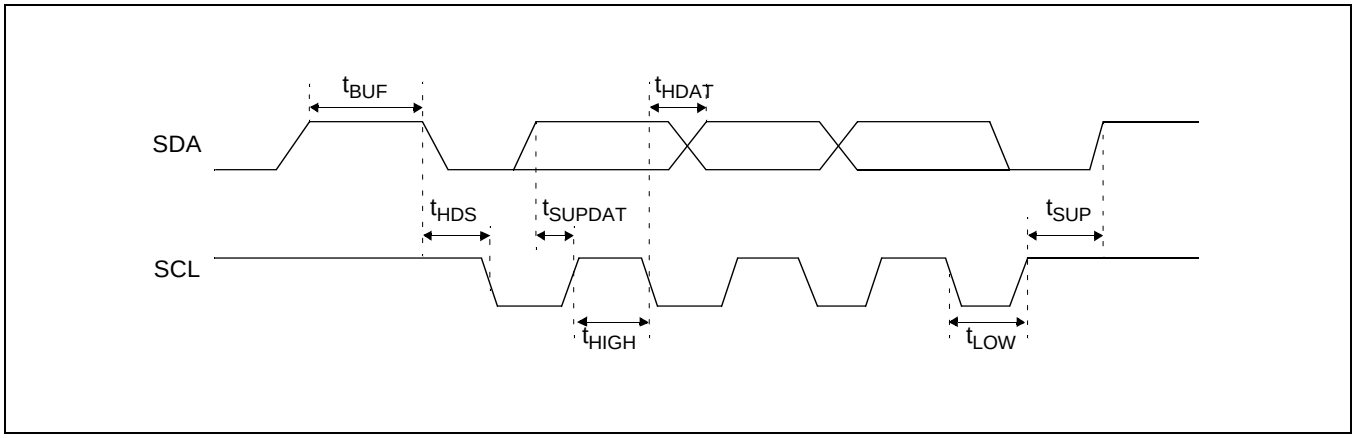


Figure 3. I²C BUS Timing Requirement

NOTES:

1. Absolute maximum rating indicates the limit beyond which damage to the device may occur.
2. Operating ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the electrical characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
3. VCC supply pins 6, and 27 must be externally wired together to prevent internal damage during VCC power on/off cycles.
4. The supply current specified is the quiescent current for VCC1/VCC2 and VDD with RL = ∞, The supply current for VCC2 (pin 27) also depends on the output load.
5. Output voltage is dependent on load resistor. Test circuit uses RL = 390Ω
6. Measure gain difference between any two amplifiers Vin = 560mVpp.
7. When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video amplifier 10MHz isolation test also requires this printed circuit board. The reason for a double sided full ground plane PCB is that large measurement variations occur in single sided PCBs.
8. Adjust input frequency from 10MHz (AV max reference level) to the-3dB frequency (f -3dB).
9. Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at fin = 10MHz for Iso_10MHz.
10. A minimum pulse width of 200 ns is guaranteed for a horizontal line of 15kHz. This limit is guaranteed by design. if a lower line rate is used a longer clamp pulse may be required.
11. During the AC test the 4V DC level is the center voltage of the AC output signal. For example. If the output is 4Vpp the signal will swing between 2V DC and 6V DC.
12. These parameters are not tested on each product which is controlled by an internal qualification procedure.

TEST SIGNAL FORMAT

Table 1. Test Signal Format

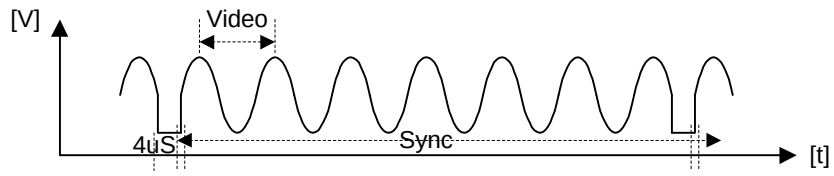
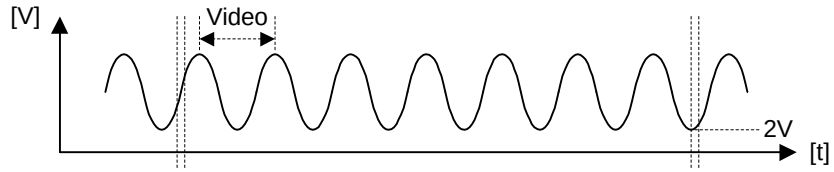
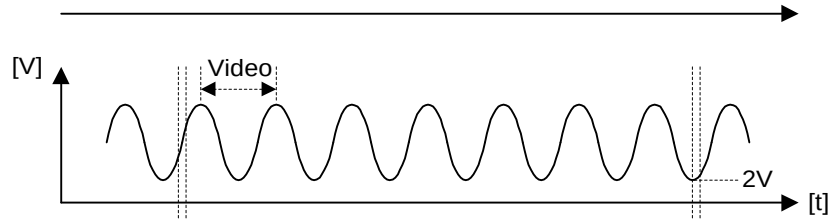
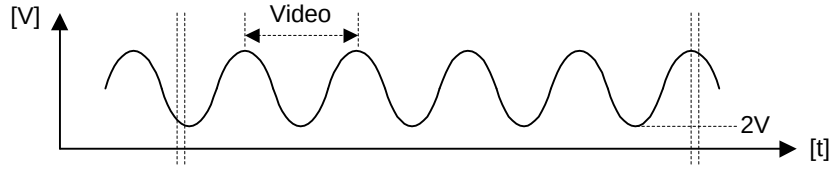
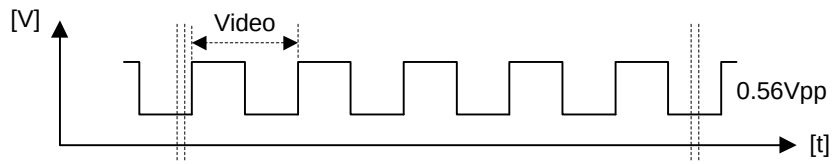
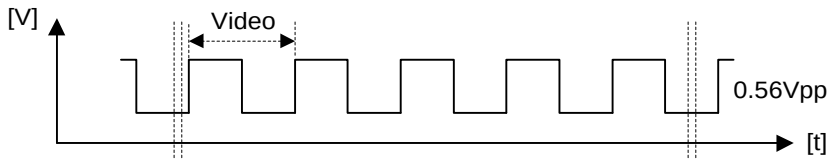
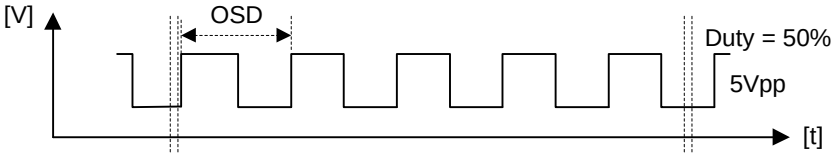
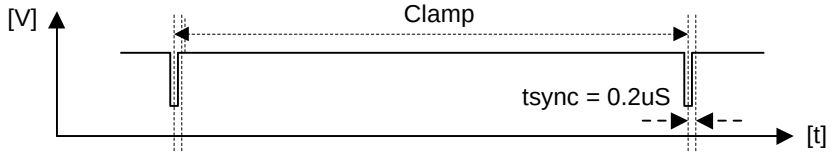
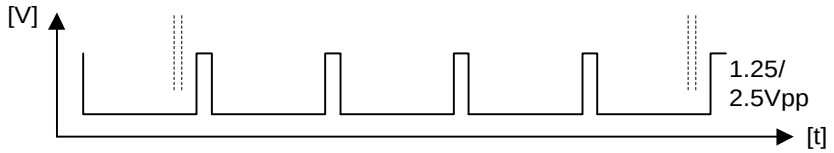
Signal Name	Input Signal Formal	Signal Description
S1		Video gain measurement Video = 1MHz/0.056Vpp (Half-Tone: 5MHz) Sync = 50kHz
S2		Video bandwidth measurement Video = 1 - 200MHz/ 0.56Vpp
S3		Cresstalk (10kHz) measurement Video = 10kHz/0.56Vpp
S4		Cresstalk (10MHz) measurement Video = 10MHz/0.56Vpp
S5		THD measurement Video = 19kHz/0.56Vpp

Table 1. Input Signal Formal (Continued)

Signal Name	Input Signal Formal	Signal Description
S6		Video Tr/Tf measurement Video = 200kHz/0.7Vpp (Duty = 50%)
S7		OSD gain, OSD Tr/Tf, propagation delay measurement OSD S/W input OSD = 200kHz/5Vpp (Duty = 50%)
S8		Clamp gate input Clamp = 50kHz (5Vpp) (Half-Tone: 200kHz) tsync = 0.2uS
S9		BU input (200kHz) - BU1 = 1.25Vpp - BU2 = 2.5Vpp

- S1, S6, S7, S9 signal's low level must be synchronized with the S8 signal's sync. term.
- The input signal level uses the IC pin as reference

FUNCTIONAL DESCRIPTION

OSD INTENSITY INPUT (ACTIVE: HIGH)

This input pin is used to indicate the OSD color intensity.

Thus, 16 color selection is achievable by combining this intensity pin with R/G/B OSD input.

OSD INPUTS

The S1D2503X01-D0B0 includes all the circuitry necessary to mix OSD signals into the R/G/B video signal.

You need 4 pins for function. (R/G/B OSD, OSD blanking)

DATA TRANSFER

All bytes are sent MSB (Most Significant Bit) bit first and the write data transfer is closed by a stop.

The MCU can write data into the S1D2503X01-D0B0 registers. To do that, after a start, the MCU must send:

- The I²C address slave byte with a low level for R/W bit (bit1)
- The byte of the internal register address where the MCU wants to write data (sub address)
- The data
- Stop

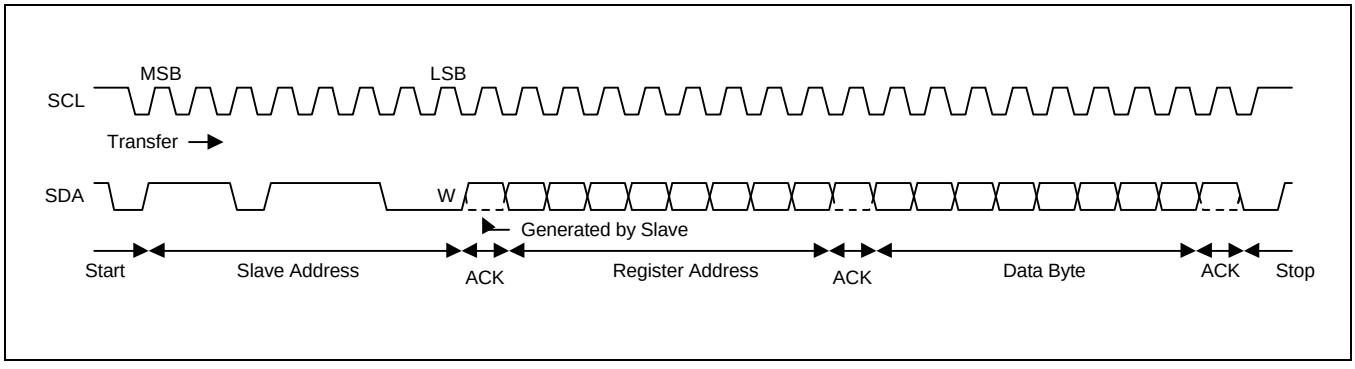
Serial Interface

The 2-wires serial interface is an I²C bus interface.

The slave address of the S1D2503X01-D0B0 is DC (hexadecimal)

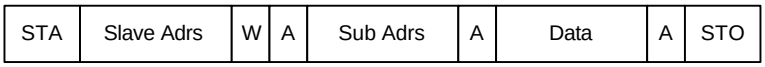
Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1
1	1	0	1	1	1	0	0 (W)

I²C Bus Write Operation: A complete data transfer

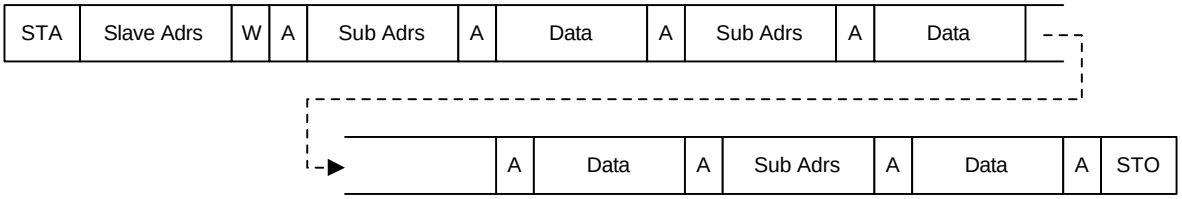


Data Transfer Format

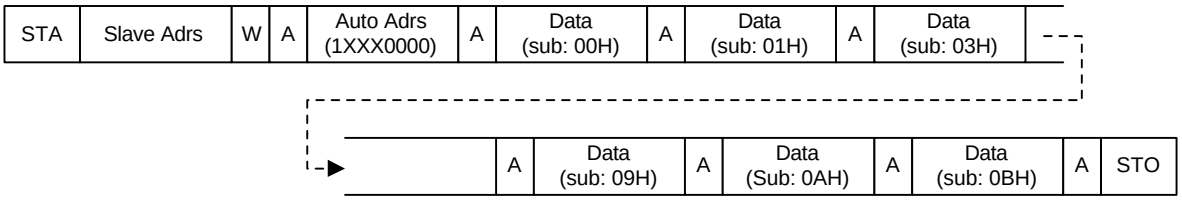
- 1Byte Data Transfer



- Multi Data Transfer



- Automatic Increment
  The automatic increment feature of the sub address enables a quick slave receiver initialization within one transmission, by the I²C bus controller



SUB ADDRESS ALLOCATION MAP (SLAVE ADDRESS: DCH)

Sub Address (Hex)	Function								DAC Bits	Int. Value (Hex)
	D7	D6	D5	D4	D3	D2	D1	D0		
00H	Contrast control								8 bits	80H
01H	Brightness control (3-ch)								8 bits	80H
02H	SUB contrast control (R)								8 bits	80H
03H	SUB contrast control (G)								8 bits	80H
04H	SUB contrast control (B)								8 bits	80H
05H	OSD contrast control								8 bits	80H
06H	Cut-off brightness control								8 bits	80H
07H	Cut-off control (R)								8 bits	80H
08H	Cut-off control (G)								8 bits	80H
09H	Cut-off control (B)								8 bits	80H
0AH	-	HB2	HG2	HR2	HB1	HG1	HR1	HT	-	00H
0BH	-	-	CPS	CS2	CS1	CT	BPS	SBLK	-	00H
0CH	-	HB3	HG3	HR3	T4	T3	T2	T1	-	0FH

- SBLK: Soft blanking switch (1: on, 0: off)
- CPS: Clamping input polarity selection (1: pos., 0: neg.)
- BPS: Blanking input polarity selection (1: pos., 0: neg.)
- HT: Video & OSD half tone (1: on, 0: off)
- HR/HG/HB: OSD raster color switch for video half tone (HT = 1)

OSD Raster1			OSD Raster2			OSD Raster3			Half Tone
HR1	HG1	HB1	HR2	HG2	HB2	HR3	HG3	HB3	
0	0	0	0	0	0	0	0	0	Black (initial)
0	0	1	0	0	1	0	0	1	Blue
0	1	0	0	1	0	0	1	0	Green
0	1	1	0	1	1	0	1	1	Cyan
1	0	0	1	0	0	1	0	0	Red
1	0	1	1	0	1	1	0	1	Magenta
1	1	0	1	1	0	1	1	0	Yellow
1	1	1	1	1	1	1	1	1	White

- CT: Cut-off control INT/EXT (0: INT/1: EXT)
- CS1/2: Extended cut-off brightness control data bits (CS1 = 100uA/CS2 = 100uA)

REGISTER DESCRIPTION

Contrast (OSD contrast adjustment) (8-bits)

The contrast adjustment is made by controlling simultaneously the gain of three internal variable gain amplifiers through the I²C bus interface.
The contrast adjustment allows you to cover a typical range of 38dB.

Brightness Adjustment (8-bits)

The brightness adjustment controls to add the same black level (pedestal) to the 3-channel/R/G/B signals after contrast amplifier by I²C bus.

Cut-Off Brightness Adjustments (8-bits)

The cut-off brightness adjustment is made by simultaneously controlling the external cut-off current.

SUB Contrast Adjustment (8-bits ´ 3)

The SUB contrast adjustment allows to cover a typical range of 12dB.

Cut-Off Adjustments (8-bits ´ 3)

These adjustments are used to adjust the white balance, and the gain of each channel is controlled by I²C bus.

Contrast Register (SUB ADRS: 00H) (Vin = 0.56Vpp, bright: 40H, sub: FFH)

Hex	Bits								Contrast (Vpp)	Gain (dB)	Int. Value (Hex)
	B7	B6	B5	B4	B3	B2	B1	B0			
00	0	0	0	0	0	0	0	0	0	-30.0	
80	1	0	0	0	0	0	0	0	1.12	11.5	O
FF	1	1	1	1	1	1	1	1	4.2	17.5	
Increment/bit									0.0164		

Brightness Register (3-ch) (sub adrs: 01H) (cont: 40H, sub: FFH)

Hex	Bits								Brightness (V)	Int. Value (Hex)
	B7	B6	B5	B4	B3	B2	B1	B0		
00	0	0	0	0	0	0	0	0	0	
80	1	0	0	0	0	0	0	0	1.4	O
FF	1	1	1	1	1	1	1	1	2.8	
Increment/bit									0.0109	

SUB Contrast Register (3-ch) (sub a]drs: 02/03/04H) (Vin = 0.56Vpp, bright: 40H, cont: FFH)

Hex	Bits								Sub Contrast (Vpp)	Gain (dB)	Int. Value (Hex)
	B7	B6	B5	B4	B3	B2	B1	B0			
00	0	0	0	0	0	0	0	0	1.33	7.5	
80	1	0	0	0	0	0	0	0	2.65	13.5	O
FF	1	1	1	1	1	1	1	1	4.2	17.5	
Increment/bit									0.0123		

OSD Contrast Register (sub adrs: 05H) (VOSD = TTL, bright: 40H, sub: FFH)

Hex	Bits								OSD Contrast (Vpp)	Gain (dB)	Int. Value (Hex)
	B7	B6	B5	B4	B3	B2	B1	B0			
00	0	0	0	0	0	0	0	0	0	-	
80	1	0	0	0	0	0	0	0	2.0	-	O
FF	1	1	1	1	1	1	1	1	4.0	-	
Increment/bit									0.0156		

Cut-Off Brightness Register (3-ch) (sub adrs: 06H)

Hex	Bits								Cut-Off Brightness (uA)	Int. Value (Hex)
	B7	B6	B5	B4	B3	B2	B1	B0		
00	0	0	0	0	0	0	0	0	0	
80	1	0	0	0	0	0	0	0	100	O
FF	1	1	1	1	1	1	1	1	200	
Increment/bit									0.781	

Cut-Off Register (3-ch) (sub adrs: 07/08/09H) (cont = 80H, subcont: FFH)

- INT: CT = 0

Hex	Bits								Cut-Off INT (V)	Int. Value (Hex)
	B7	B6	B5	B4	B3	B2	B1	B0		
00	0	0	0	0	0	0	0	0	-0.4	
80	1	0	0	0	0	0	0	0	0	O
FF	1	1	1	1	1	1	1	1	0.4	
Increment/bit									0.0031	

- EXT: CT = 1

Hex	Bits								Cut-Off EXT (uA)	Int. Value (Hex)
	B7	B6	B5	B4	B3	B2	B1	B0		
00	0	0	0	0	0	0	0	0	0	
80	1	0	0	0	0	0	0	0	250	O
FF	1	1	1	1	1	1	1	1	480	
Increment/bit									1.875	

RECOMMENDATION

12V Power Routing

Because S1D2503X01-D0B0 is a wideband AMP of above 200MHz, 12V power significantly affects the video characteristics. The effects from the inductance and capacitance are different for each board, and , therefore, some tuning is required to obtain the optimum performance. The output power, VCC2, must be separated from VCC1 using a bead or a coil, which is parallel-connected to the damping resistor. In the case of using a coil , the appropriate coil value is between 20uH - 200uH. Parallel-connected a variable resistor to the coil and control its resistance to obtain the optimum video waveform.

(Bead use: Refer to Application Circuit)

(Moreover, bead can be replaced using a coil and variable resistor to obtain the optimum video waveform.)

VCC1 12V Power

Use a 104 capacitor and large capacitor for the power filter capacitor.

12V Output Stage Power VCC2

Do not use the power filter capacitor or use a capacitor smaller than 22pF, because it is an important factor of video oscillation.

Output Stage GND2

Care must be taken during routing because it ,as an AMP output stage GND, is an important factor of video oscillation. R/G/B clamp cap and R/G/B load resistor must be placed as close as possible to the GND2 pin. GND2 must be arranged so that it has the minimum GND loop.

R/G/B Clamp Capacitor

Use the 104 capacitor for normal R/G/B clamps.

During the clamp signal's input period, the clamp stage compares the video output's pedestal level and the level adjusted by sub address 01. If an error is detected, current is charged/discharged to the clamp capacitor, so that the video output pedestal level is set to the adjusted level.

The current charged/discharged to the clamp cap is about 750uA. The capacitor value is very important.

If the R/G/B clamp cap's charge current is different for each channel, the screen can first appear to be red or blue, then later become normal when you turn the power on. In that case, it is best to change the clamp cap value to adjust the charge/discharge time.

DC Coupling Capacitor

Select the video input DC coupling cap with sagging in mind.

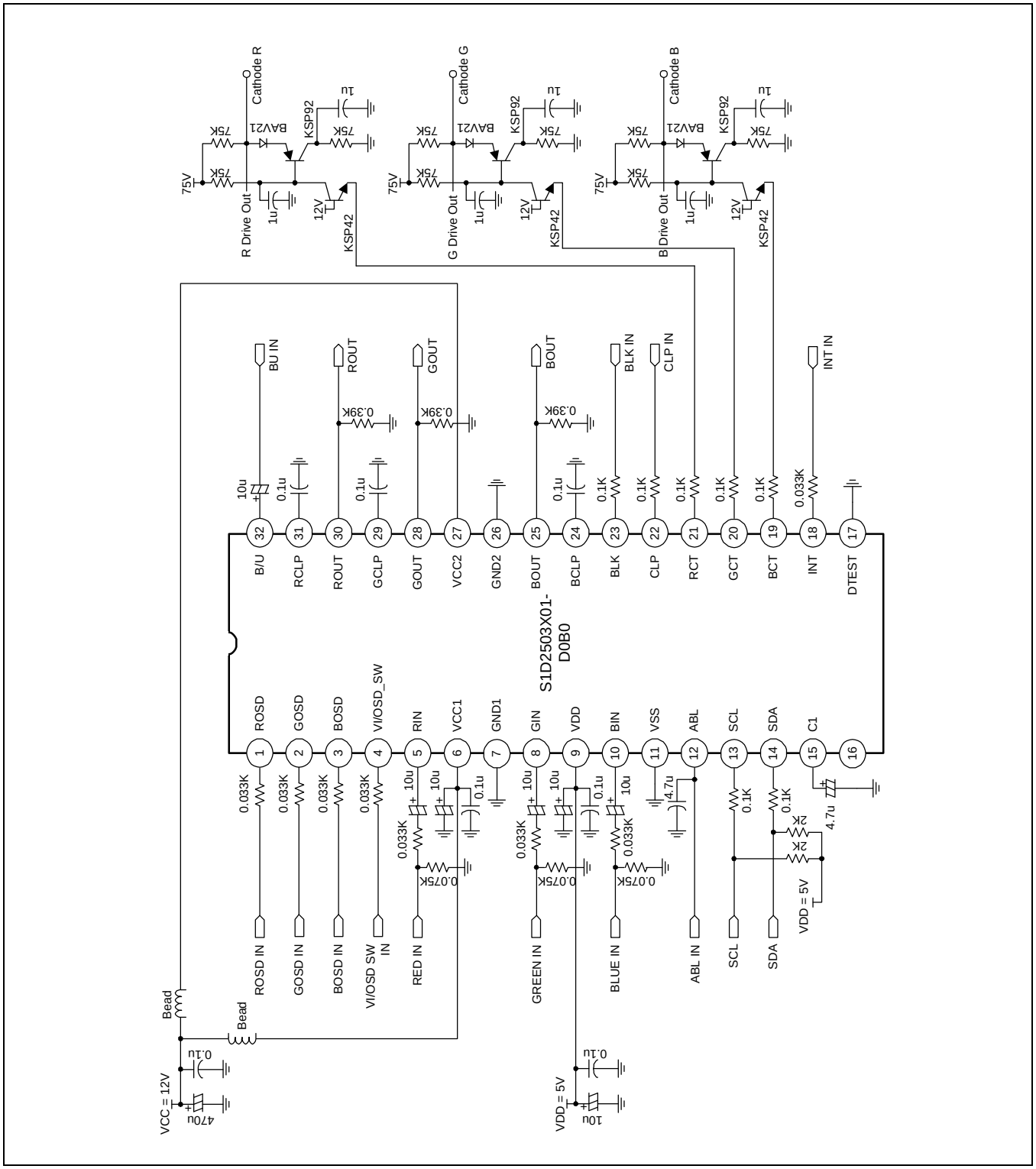
Select from between 10uF and 0.1uF.

Brightness Uniformity(modulation means suppressing the ratio to the video output level)

The brightness uniformity feature using the Pre AMP directly influences the video signal, so it can influence the focus as well. Therefore, it is best to minimize the modulation degree as much as possible. Try not to go above10%.

When not using the IC's B/U feature, connect it to a capacitor of about 0.1uF and short it to GND.

APPLICATION BOARD CIRCUIT



TYPICAL APPLICATION CIRCUIT