

6A, 1200V Hyperfast Dual Diode

The RHRP6120CC is a hyperfast dual diode with soft recovery characteristics ($t_{RR} < 55\text{ns}$). It has half the recovery time of ultrafast diodes and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

Formerly developmental type TA49058.

PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP6120CC	TO-220AB	RHR6120C

NOTE: When ordering, use the entire part number.

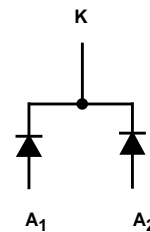
Features

- Hyperfast with Soft Recovery<55ns
- Operating Temperature +175°C
- Reverse Voltage1200V
- Avalanche Energy Rated
- Planar Construction

Applications

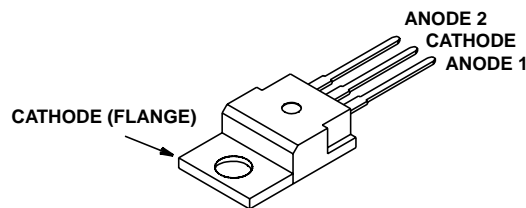
- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Symbol



Packaging

JEDEC TO-220AB



RHRP6120CC

Absolute Maximum Ratings (Per Leg) $T_C = +25^{\circ}\text{C}$, Unless Otherwise Specified

	RHRP6120CC	UNITS
Peak Repetitive Reverse Voltage..... V_{RRM}	1200	V
Working Peak Reverse Voltage..... V_{RWM}	1200	V
DC Blocking Voltage..... V_R	1200	V
Average Rectified Forward Current..... $I_{F(AV)}$ $T_C = 130^{\circ}\text{C}$	6	A
Repetitive Peak Surge Current..... I_{FSM} Square Wave, 20kHz	12	A
Nonrepetitive Peak Surge Current..... I_{FSM} Halfwave, 1 Phase, 60Hz	60	A
Maximum Power Dissipation..... P_D	50	W
Avalanche Energy (See Figures 10 and 11)..... E_{AVL}	10	mJ
Operating and Storage Temperature..... T_{STG}, T_J	-65 to +175	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications (Per Leg) $T_C = +25^{\circ}\text{C}$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_F	$I_F = 6\text{A}, T_C = +25^{\circ}\text{C}$	-	-	3.2	V
	$I_F = 6\text{A}, T_C = +150^{\circ}\text{C}$	-	-	2.6	V
I_R	$V_R = 1200\text{V}, T_C = +25^{\circ}\text{C}$	-	-	100	μA
	$V_R = 1200\text{V}, T_C = +150^{\circ}\text{C}$	-	-	500	μA
t_{RR}	$I_F = 1\text{A}, dI_F/dt = 200\text{A}/\mu\text{s}$	-	-	55	ns
	$I_F = 6\text{A}, dI_F/dt = 200\text{A}/\mu\text{s}$	-	-	65	ns
t_A	$I_F = 6\text{A}, dI_F/dt = 200\text{A}/\mu\text{s}$	-	33	-	ns
t_B	$I_F = 6\text{A}, dI_F/dt = 200\text{A}/\mu\text{s}$	-	22	-	ns
Q_{RR}	$I_F = 6\text{A}, dI_F/dt = 200\text{A}/\mu\text{s}$	-	210	-	nC
C_J	$V_R = 10\text{V}, I_F = 0\text{A}$	-	22	-	pF
$R_{\theta JC}$		-	-	3	$^{\circ}\text{C}/\text{W}$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300 μs , D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 9), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 9).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 9).

Q_{RR} = Reverse recovery charge.

C_J = Junction Capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled Avalanche Energy (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

Typical Performance Curves

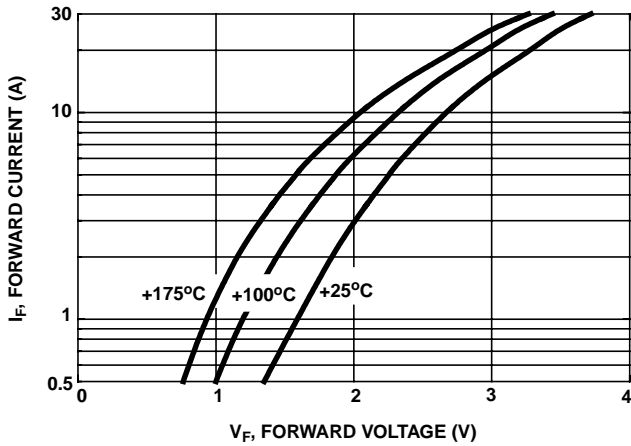


FIGURE 1. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

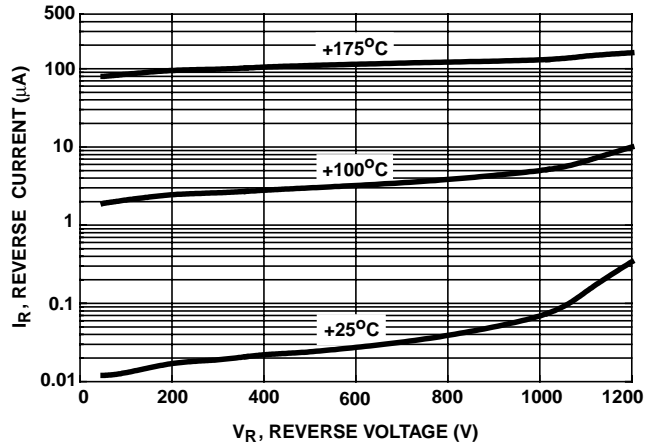


FIGURE 2. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

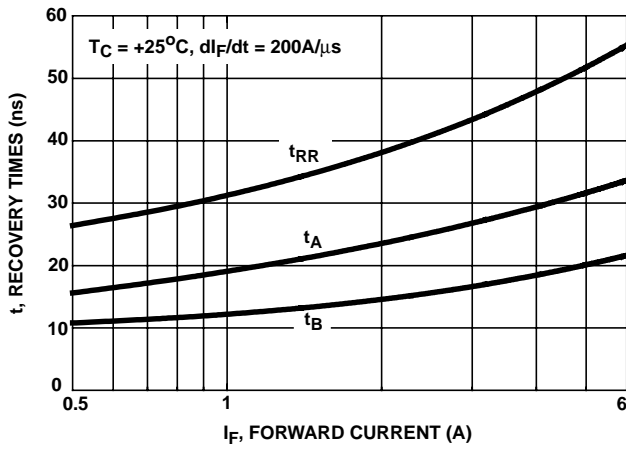


FIGURE 3. TYPICAL t_{RR} , t_A AND t_B CURVES vs FORWARD CURRENT AT 25°C

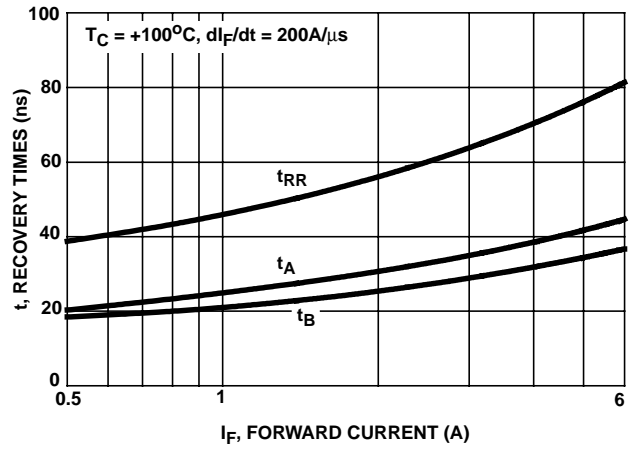


FIGURE 4. TYPICAL t_{RR} , t_A AND t_B CURVES vs FORWARD CURRENT AT 100°C

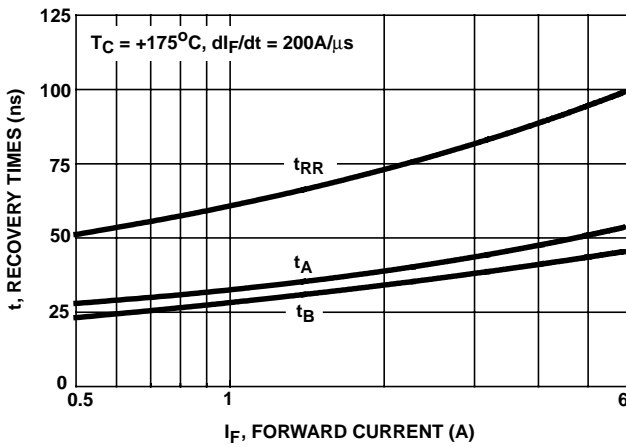


FIGURE 5. TYPICAL t_{RR} , t_A AND t_B CURVES vs FORWARD CURRENT AT 175°C

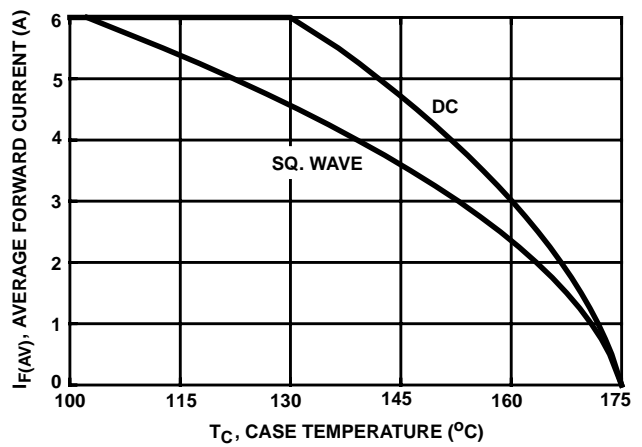


FIGURE 6. CURRENT DERATING CURVE

Typical Performance Curves (Continued)

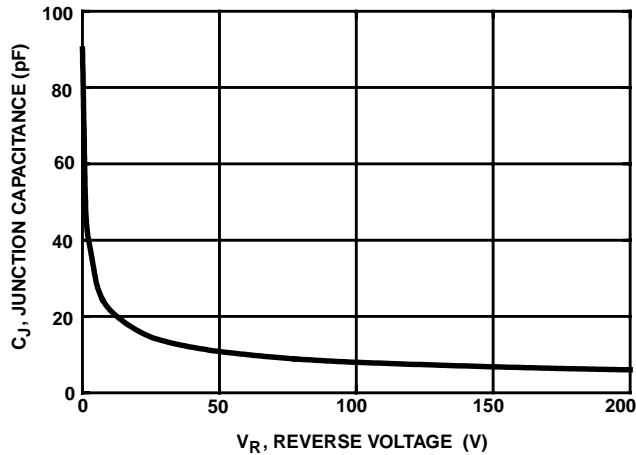


FIGURE 7. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuits and Waveforms

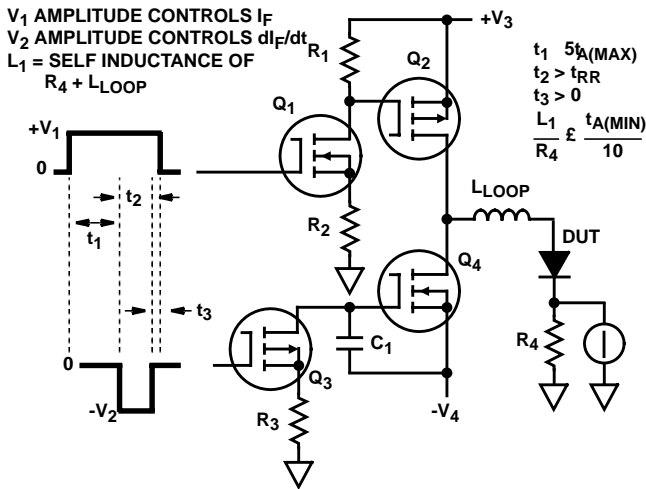


FIGURE 8. t_{RR} TEST CIRCUIT

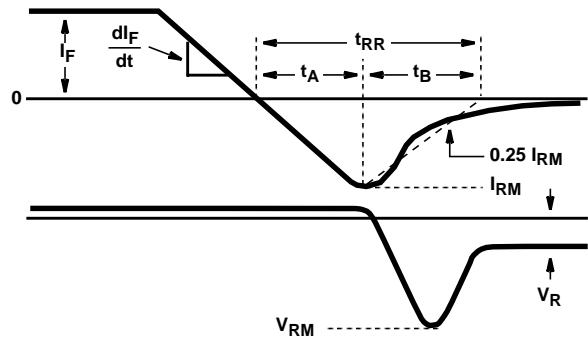


FIGURE 9. t_{RR} WAVEFORMS AND DEFINITIONS

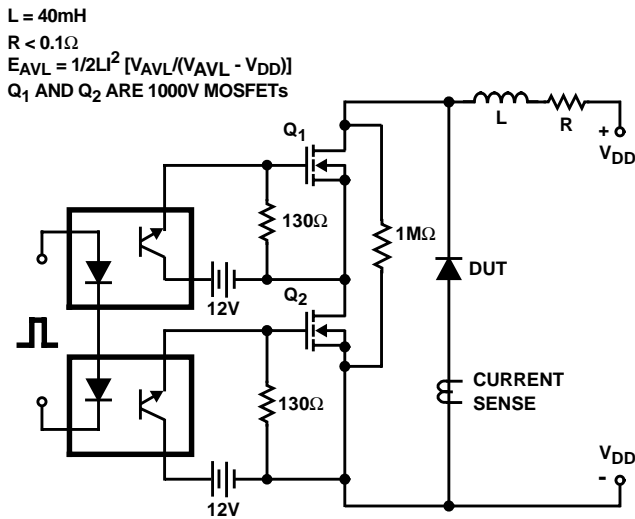


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

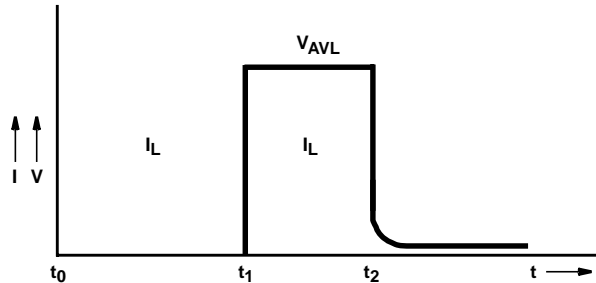
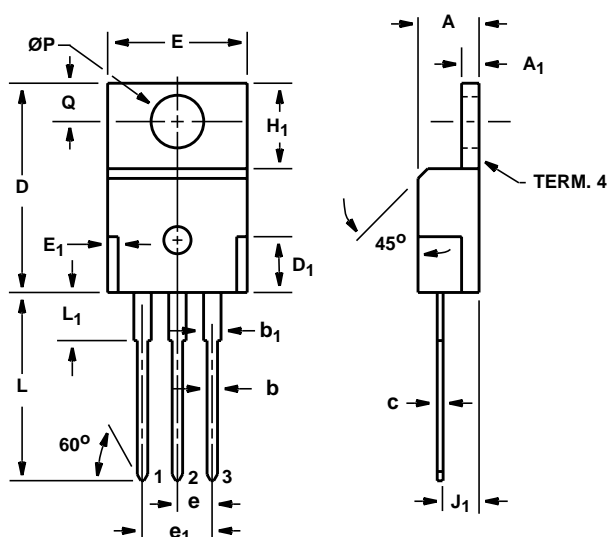


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



LEAD 1. ANODE 1
 LEAD 2. CATHODE
 LEAD 3. ANODE 2
 TERM. 4. CATHODE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D ₁	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E ₁	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L₁.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site www.intersil.com

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
 P. O. Box 883, Mail Stop 53-204
 Melbourne, FL 32902
 TEL: (321) 724-7000
 FAX: (321) 724-7240

EUROPE

Intersil SA
 Mercure Center
 100, Rue de la Fusee
 1130 Brussels, Belgium
 TEL: (32) 2.724.2111
 FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
 7F-6, No. 101 Fu Hsing North Road
 Taipei, Taiwan
 Republic of China
 TEL: (886) 2 2716 9310
 FAX: (886) 2 2715 3029