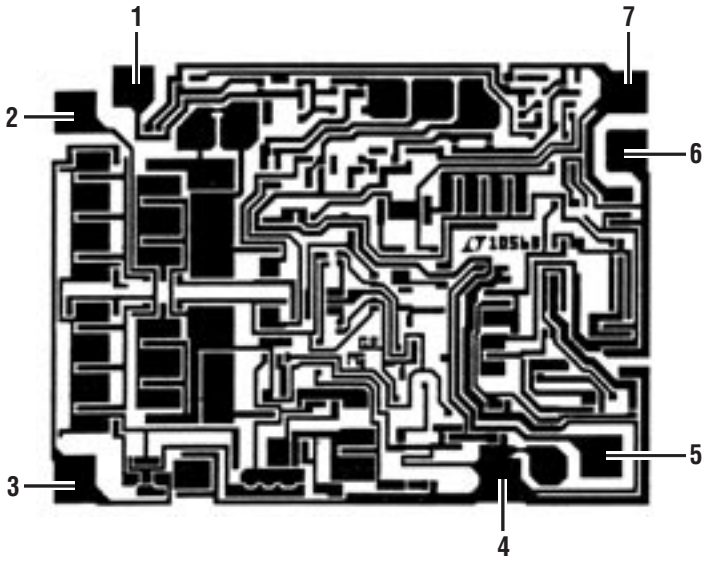
RH1056
Precision, High Speed, JFET Input Operational Amplifier



59mils × 78mils,
Backlap: 12mils
Backside (substrate) is an alloyed gold layer.

DIE CROSS REFERENCE (Notes 1 and 2)

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
RH1056A RH1056A	RH1056 DICE RH1056 DWF*

Please refer to LTC standard product data sheet for other applicable product information.
***DWF = DICE in wafer form.**

PAD FUNCTION

1. BALANCE
2. – IN
3. + IN
4. V^-
5. BALANCE
6. OUT
7. V^+

DICE ELECTRICAL TEST LIMITS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 3)		0.5	mV
I_{OS}	Input Offset Current	(Note 4)		50	pA
I_B	Input Bias Current	(Note 4)		200	pA
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V, R_L = 2k	120		V/mV

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DICE ELECTRICAL TEST LIMITS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OUT}	Output Voltage Swing	R_L = 2k, V_S = ±15V	±12		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V, V_S = ±15V	86		dB
PSRR	Power Supply Rejection Ratio	VS = ±10V to ±18V	88		dB
SR	Slew Rate	(Note 5)	10		V/μs
I_S	Supply Current			6	mA

Note 1: Dice are probe tested at 25°C to the limits shown. Final specs, after assembly cannot be guaranteed at the die level due to yield loss and assembly shifts. For absolute maximum ratrings, typical specifications, performance curves and finished product specifications, please refer to the standard product data sheet.

Note 2: For dice tested to tighter limits than those listed above and/or, lot qualification based on sample lot assembly and testing, please contact LTC Marketing.

Note 3: V_S = ±15V, T_A = 25°C, V_{CM} = 0_V, unless otherwise noted.

Note 4: This is not a reflection of actual I_{OS} and I_B. Typical values are 5pA and 20pA respectively at final test. JFETs sensitivity to light at wafer sort requires a loose limit.

Note 5: Tested at a gain of "5".

Rad Hard die require special handling as compared to standard IC chips.

Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much "softer" than silicon nitride.

LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die around from the chip tray, use a Teflon-tipped vacuum wand. This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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