



# High Speed CMOS 16-Bit Register with Clock Enable in QVSOP™

QS74FCT2X377T

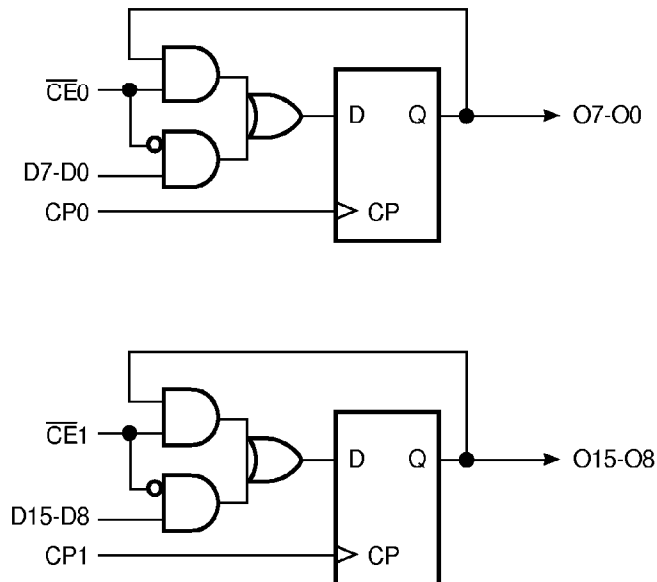
## FEATURES/BENEFITS

- Function compatible to the 74F377, 74FCT377 and 74ABT377
- CMOS power levels: <15 mW static
- Undershoot clamp diodes on all inputs
- Fastest CMOS logic family available
- JEDEC-FCT spec compatible
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Available in 40-pin 0.4 mm pitch QVSOP (Q2)
- A and C speed grades with 5.2 ns  $t_{PD}$  for C
- $I_{OL} = 48$  mA Com.

## DESCRIPTION

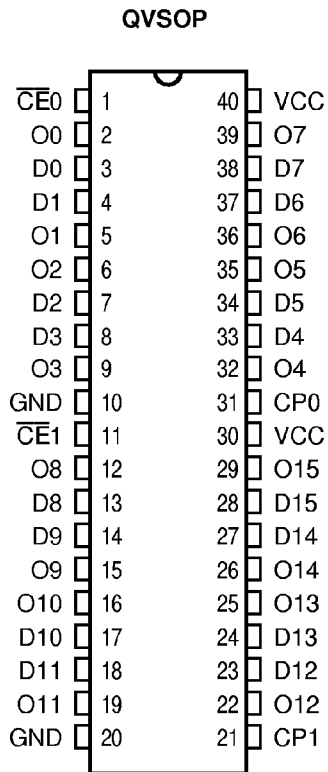
The QS74FCT2X377 is a high-speed 16-bit CMOS TTL-compatible register. It includes a buffered clock, a buffered output drive, and a synchronous clock enable. Data is stored in the register on the rising edge of the clock if the clock enable input is active. The high-output current  $I_{OL}$  and  $I_{OH}$  drive high capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when  $V_{CC}$  is removed from the device.

## FUNCTIONAL BLOCK DIAGRAM



**QS74FCT2X377T PRELIMINARY**

**PIN CONFIGURATION (Top View)**



**PIN DESCRIPTION**

Name	I/O	Description
Di	I	Data Inputs
Oi	O	Data Outputs
CPi	I	Clock Input
$\overline{CE}i$	I	Clock Enable

**FUNCTION TABLE**

$\overline{CE}i$	Inputs CPi	Di	Internal Q Value	Outputs Oi	Function
H	X	X	NC	NC	Hold Value
L	↑	L	L	L	Load Input Data
L	↑	H	H	H	

Note:

$\overline{CE}0$ , CP0 control bits 7-0

$\overline{CE}1$ , CP1 control bits 15-8