PULSUS   PS9604

Stereo, 24-Bit, 192kHz PCM-to-PWM Converter for Full Digital Power Amplifier

Features

- **Sampling Frequency: 32kHz to 192kHz**
- **8X Oversampling at 96kHz**
- **4X Oversampling at 192kHz**
- **Input Audio Data Word: 20-, 24-Bit**
- **130 dB Dynamic Range**
- **120 dB SNR (typical)**
- **Variable Modulation Index: 0.5 to 0.875**
- **PWM Switching Frequency: 256~384kHz**
- **Variable PWM Mapping Method: Both Class AD, BD amplifications are supported**
- **Automatic Sample Rate Detection**
- **System Clock:**
  2048fs at 48kHz, 1024fs at 96kHz,
  512fs at 192kHz
- **Single 3.3 V Power Supply**
- **28-Lead SOIC Package**

Description

The PS9604 is a high performance, stereo, 24-bit, 192kHz PCM-to-PWM converter IC.

The PS9604 uses a state-of-the-art digital signal-processing algorithm to convert input PCM signal to PWM format without sacrificing the quality of audio signal.

The PS9604 can be used with various 8X oversampling digital filters, for example, DF1704, SM5847, and PMD200. It can be set up to use different modulation indices and PWM mapping methods.

The PS9604's excellent SNR and ultra-low distortion makes it suitable for a size-sensitive consumer power amplifier application where high performance is required, such as high-quality AV receiver, digital TV, and hi-fi amplifiers. A high-end quality full-digital amplifier can be built using the PS9604, with minimal cost.

Application Block Diagram
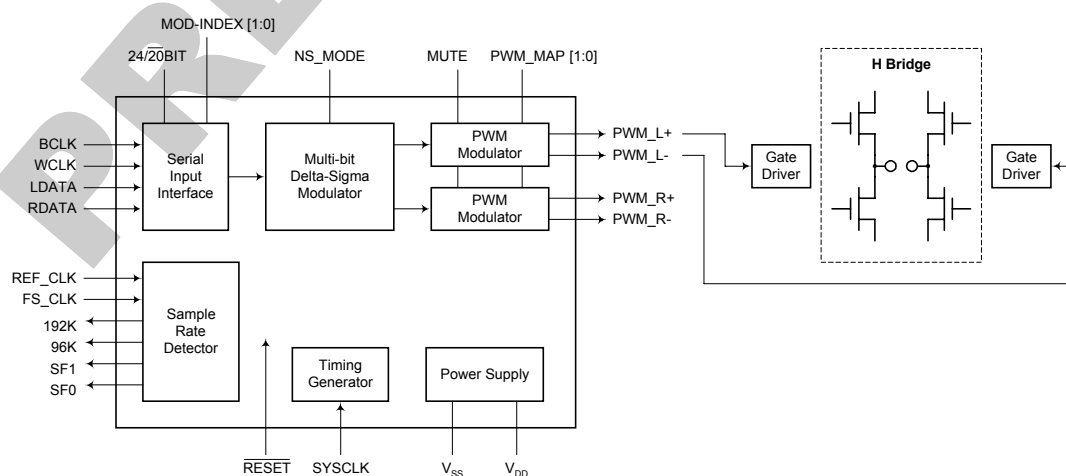
Specifications

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Power Supply Voltage (V_{DD} to V_{SS})	$V_{SS} - 0.3$	4.0	V
Input Current, (Any pin except Supply)	-	±10	mA
Output Current (/Pin)	-	±30	mA
Input Voltage (Any pin except 5V tolerant)	$V_{SS} - 0.3$	$V_{DD} + 0.5$	V
Input Voltage (5V tolerant Input)	$V_{SS} - 0.3$	+7.5	V
Storage Temperature	-65	+150	$^\circ$C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
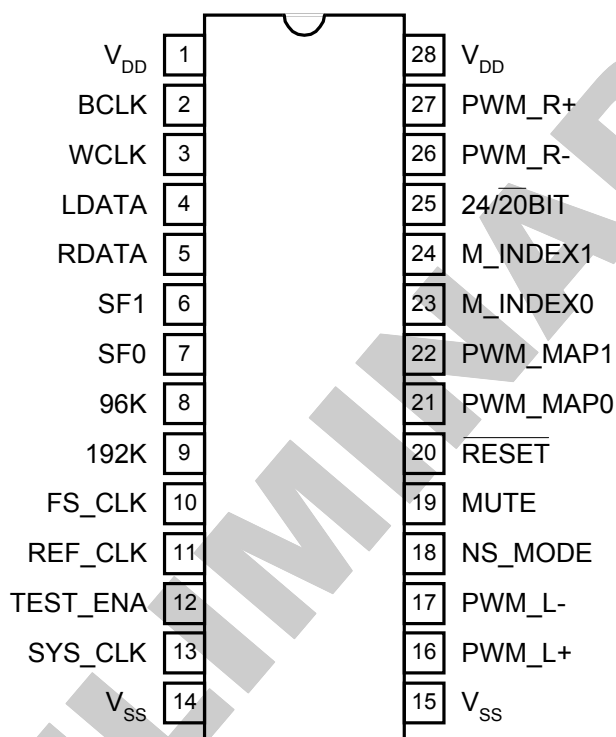
RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Power Supply Voltage (V_{DD} to V_{SS})	3.0	3.3	3.6	V
Input Voltage (Any pin except 5V tolerant)	V_{SS}	-	V_{DD}	V
Input Voltage (5V tolerant Input)	V_{SS}		5.5	V
Ambient Operating Temperature	-40		+85	$^\circ$C

ELECTRICAL CHARACTERISTICS

Parameter	Min	Typ	Max	Units
Input Leakage Current	-1	-	1	μA
High-Level Input Voltage (except RESET)	2.0	-	-	V
Low-Level Input Voltage (except RESET)	-	-	0.8	V
High-Level Input Voltage (RESET)	1.1	-	2.4	V
Low-Level Input Voltage (RESET)	0.6	-	1.8	V
High-Level Output Voltage (I_O = 2mA)	$V_{DD} - 0.4$	-	-	V
Low-Level Output Voltage (I_O = 2mA)	-	-	0.4	V
Pull-up Resistance	20	50	100	kΩ
Pull-down Resistance	20	50	100	kΩ
Input Capacitance (f = 1MHz, V_{DD} = 0V)	-	-	10	pF
Output Capacitance (f = 1MHz, V_{DD} = 0V)	-	-	10	pF

Pin Assignment

V_{DD}	1	28	V_{DD}
BCLK	2	27	PWM_R+
WCLK	3	26	PWM_R-
LDATA	4	25	24/20BIT
RDATA	5	24	M_INDEX1
SF1	6	23	M_INDEX0
SF0	7	22	PWM_MAP1
96K	8	21	PWM_MAP0
192K	9	20	RESET
FS_CLK	10	19	MUTE
REF_CLK	11	18	NS_MODE
TEST_ENA	12	17	PWM_L-
SYS_CLK	13	16	PWM_L+
V_{SS}	14	15	V_{SS}

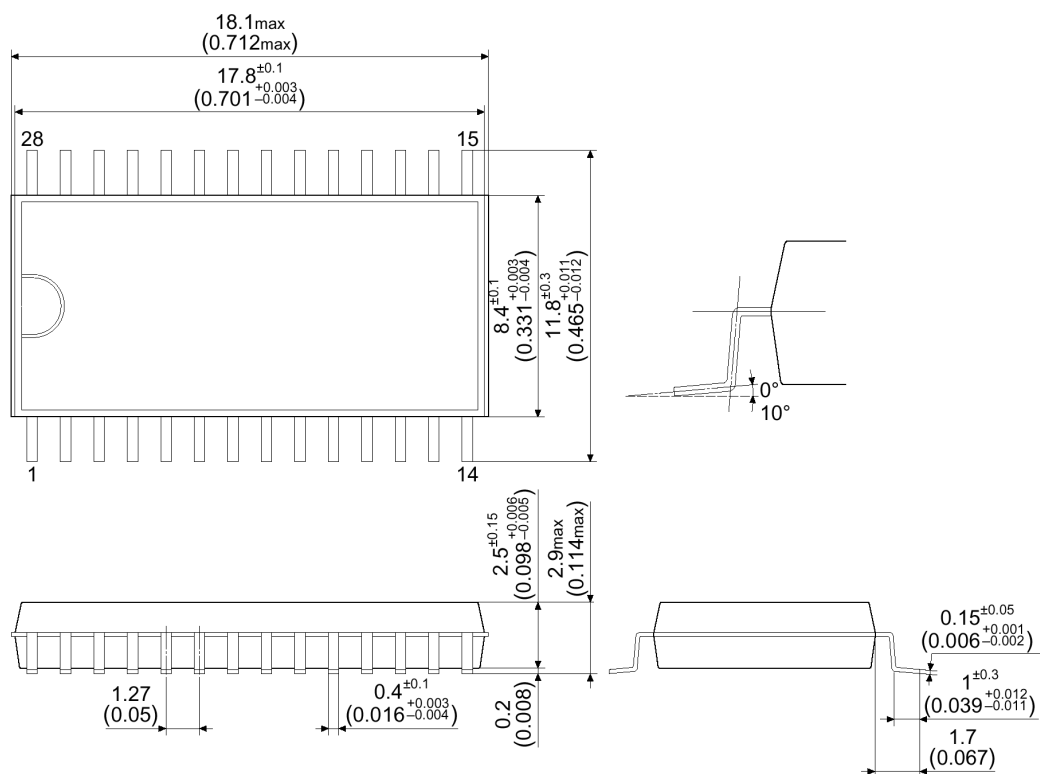PS9604 (28Lead SOIC, Top View)

Pin Descriptions

PIN No.	PIN NAME	I/O	DESCRIPTION
1	V_{DD}	-	Digital Power, +3.3V
2	BCLK	IN	Bit clock input for serial audio data. BCLK shifts data input on the rising clock edge. Need not run continuously; may be gated or used in a burst fashion. *This input is 5V tolerant.*
3	WCLK	IN	Word clock input for serial audio data. WCLK latch the shifted data input on the falling clock edge. *This input is 5V tolerant.*
4	LDATA	IN	Left channel serial data input. *This input is 5V tolerant.*
5	RDATA	IN	Right channel serial data input. Both LDATA and RDATA are assumed to be MSB-first 2's-compliment. If data is absent or held to a constant value (all 0's or constant values for 8192 words at 44.1/48kHz sampling rate), or any of the input clocks are removed, an internal MUTE is activated. *This input is 5V tolerant.*
6	SF1	OUT	Sampling rate indication output.
7	SF0	OUT	(SF1, SF0) = (0,0) : 44.1kHz (0,1) : other sampling rate (1,0) : 48kHz (1,1) : 32kHz
8	96K	OUT	88.2/96kHz sampling rate indication output. This pin goes High when the sampling rate is 88.2/96kHz.
9	192K	OUT	176.4/192kHz sampling rate indication output. This pin goes High when the sampling rate is 176.4/192kHz.
10	FS_CLK	IN	Sampling rate clock input. *This input is 5V tolerant. Internal pull-down resistor.*
11	REF_CLK	IN	Reference clock input. 12.288MHz Reference clock is required to detect sampling rate. *This input is 5V tolerant. Internal pull-down resistor.*
12	TEST_ENA	-	Chip test mode enabling input. This pin should be tied to GND for normal operation.
13	SYS_CLK	IN	Master system clock input. Connect to an external clock source. 2048Fs at 32/44.1/48kHz sampling rate, 1024Fs at 88.2/96kHz sampling rate, 512Fs at 176.4/192kHz sampling rate. *This input is 5V tolerant.*
14	V_{SS}	-	Digital Ground
15	V_{SS}	-	Digital Ground
16	PWM_L+	OUT	Left channel Positive PWM output.
17	PWM_L-	OUT	Left channel Negative PWM output.

18	NS_MODE	IN	Noise shaping mode selection. This pin selests between Noise shaping MODE0 (Low) and Noise shaping MODE1 (High). An internal 50kΩ pull-up to V_{DD} will hold NS_MODE high, so no connection is required if Noise shaping MODE1 is required. *Internal pull-up resistor. Input must be driven by levels of V_{SS} to V_{DD}.*
19	MUTE	IN	Mute control. Active High input. Assert 'High' to mute both stereo outputs. Deassert 'Low' for normal operation. *This input is 5V tolerant. Internal pull-down resistor.*
20	RESET	IN	Reset input. Active Low Schmitt-Trigger input. The Schmitt-Trigger input allows a slowly-rising input to reset the chip reliably. The RESET signal must be asserted 'Low' during power up. Deassert 'High' for operation. *This input is 5V tolerant.*
21	PWM_MAP0	IN	PWM mapping method selection. (PWM_MAP1, PWM_MAP0) = (0,0) : 400kHz, AD (0,1) : 800kHz, AD
22	PWM_MAP1	IN	(1,0) : 400kHz, BD (1,1) : 400kHz, AD *Internal pull-up resistor. Input must be driven by levels of V_{SS} to V_{DD}.*
23	M_INDEX0	IN	Modulation Index selection. (M_INDEX1, M_INDEX0) = (0,0) : 50.0% (0,1) : 62.5%
24	M_INDEX1	IN	(1,0) : 75.0% (1,1) : 87.5% *Internal pull-up resistor. Input must be driven by levels of V_{SS} to V_{DD}.*
25	24/20BIT	IN	Input data word size selection. This pin selects between 24 bits input word size (High) and 20 bits input word size (Low). An internal 50kΩ pull-up to V_{DD} will hold 24/20BIT high, so no connection is required if input word size is 24 bits. *Internal pull-up resistor. Input must be driven by levels of V_{SS} to V_{DD}.*
26	PWM_R-	OUT	Right channel Negative PWM output.
27	PWM_R+	OUT	Right channel Positive PWM output.
28	V_{DD}	-	Digital Power, +3.3V

Package Dimensions

Plastic SOP2-28 pin (450mil)

Unit:mm(inch)