PLL650-03

Low EMI Network LAN Clock

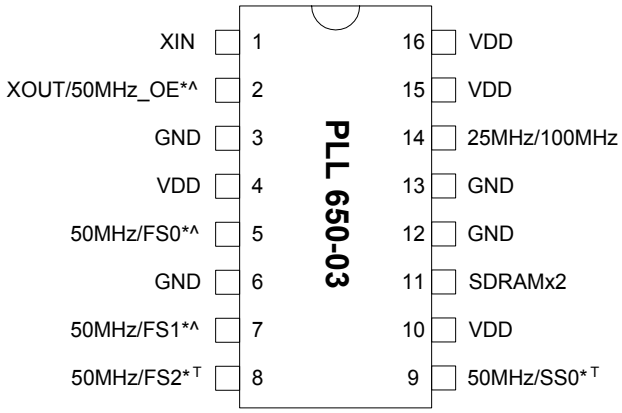
FEATURES

- Full CMOS output swing with 40-mA output drive capability. 25-mA output drive at TTL level.
- Advanced, low power, sub-micron CMOS processes.
- 25MHz fundamental crystal or clock input.
- 4 outputs fixed at 50MHz with output disable, 1 output selectable at 25MHz or 100MHz with output disable
- SDRAM selectable frequencies of 66.6, 75, 83.3, 100MHz (Double Drive Strength).
- Spread spectrum technology selectable for EMI reduction from ±0.5%, ±0.75% center for SDRAM and CPU.
- Zero PPM synthesis error in all clocks.
- Ideal for Network switches.
- 3.3V operation.
- Available in 16-Pin 150mil SOIC.

DESCRIPTION

The PLL 650-03 is a low cost, low jitter, and high performance clock synthesizer. With PhaseLink's proprietary analog Phase Locked Loop techniques, the chip accepts 25.0 MHz crystal, and produces multiple output clocks for networking chips, PCI devices, SDRAM, and ASICs.

PIN CONFIGURATION



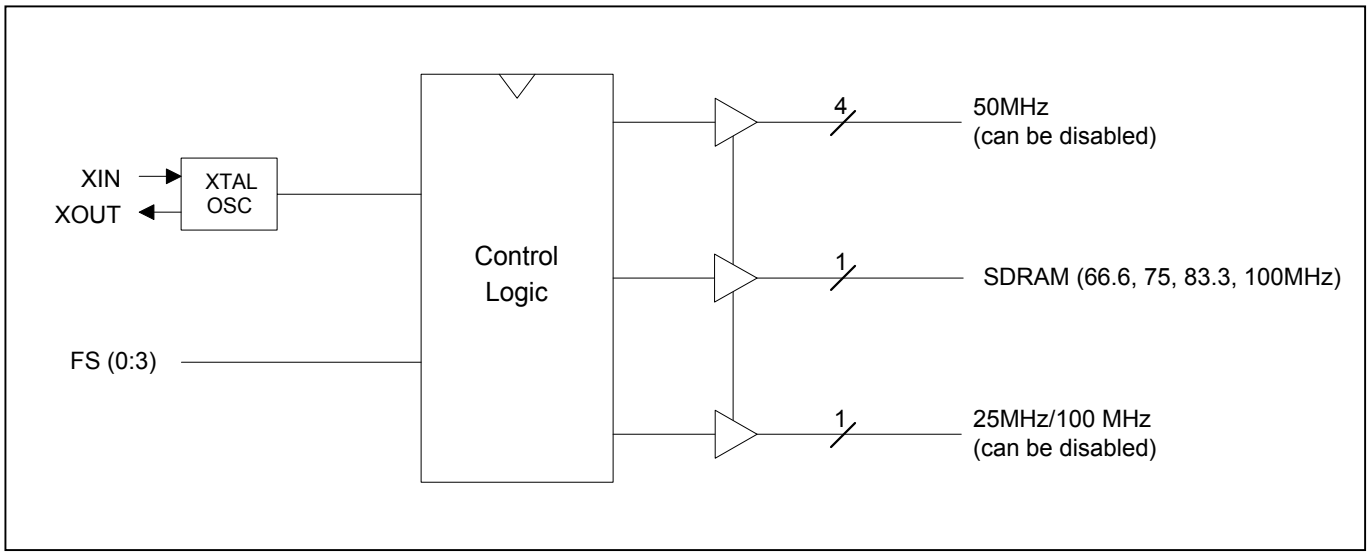
Note: SDRAMx2: Double Drive strength. T: Tri-Level input ^: Internal pull-up resistor *: Bi-directional pin (input value is latched upon power-up).

FREQUENCY TABLE

FS0	FS1	SDRAM	FS2	Pin 14
0	0	100MHz^{SST}	0	25MHz
0	1	83.3MHz^{SST}	M	Disable
1	0	75MHz^{SST}	1	100MHz^{SST}
1	1	66.6MHz^{SST}		

SST: SST modulation applied

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Type	Description
XIN	1	I	25MHz fundamental crystal input (20pF C_L parallel resonant). C_L have been integrated into the chip. No external C_L capacitor is required.
XOUT/50MHz_OE	2	B	Crystal connection pin. At power-up, this pin latches 50MHz_OE (output enable selector for all 50MHz outputs. Disabled when 50MHz_OE is logical zero. Has 120kΩ internal pull up resistor.
50MHz/FS(0:2)	5,7,8	B	50MHz outputs. These pins latch FS(0:2) value at power-up. Pins 5 and 7 have 60kΩ internal pull up resistors.
50MHz/SS0	9	B	50MHz output. This pin latches SS0 value at power-up (tri-level pin). SS0 value is used to control the spread spectrum function.
SDRAMx2	11	O	SDRAM outputs with double drive strength determined by FS(0:1) value.
25MHz/100MHz	14	O	25MHz (reference) or 100MHz output. Can be disabled with FS2 = M.
VDD	4,10,15,16	P	3.3V power supply.
GND	3,6,12,13	P	Ground.

SPREAD SPECTRUM SELECTION TABLE

SS0	SST
0	±0.75% Center
M	OFF
1	±0.5% Center

FUNCTIONAL DESCRIPTION

Selectable spread spectrum and output frequencies

The PLL650-03 provides selectable spread spectrum modulation and selectable output frequencies. Selection is made by connecting specific pins to a logical “zero” or “one”, or by leaving them not connected (tri-level inputs or internal pull-up) according to the frequency and spread spectrum selection tables shown on pages 1 and 2 respectively.

In order to reduce pin usage, the PLL650-03 uses tri-level input pins. These pins allow 3 levels for input selection: namely, 0 (Connect to GND), 1 (Connect to VDD), M (Do not connect). Thus, unlike the two-level selection pins, the tri-level input pins are in the “M” (mid) state when not connected. In order to connect a tri-level pin to a logical “zero”, the pin must be connected to GND. Likewise, in order to connect to a logical “one” the pin must be connected to VDD.

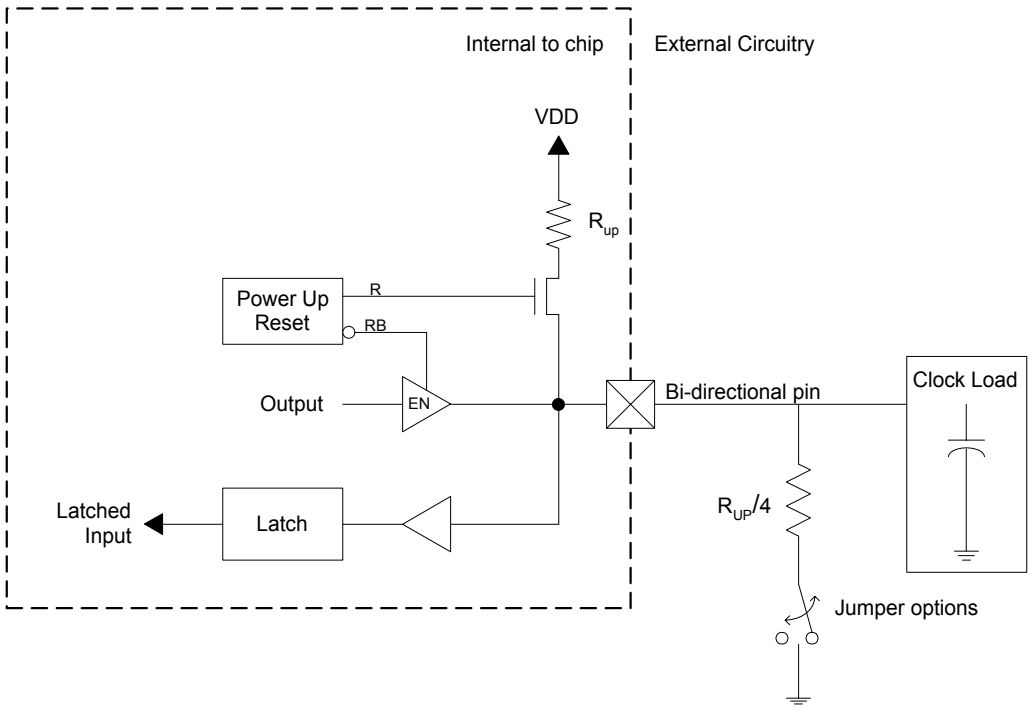
Pin 2 (XOUT/50MHz_OE) is a bi-directional pin used to disable the 50MHz outputs. Pin 5 (FS0) and pin 7 (FS1) are bi-directional pins used to select the SDRAM output frequency upon power-up. Pin 8 (FS2) and pin 9 (SS0) are bi-directional pins used to select the output frequency of pin 14, as shown in the frequency table on page 1, and to control the Spread Spectrum modulation for EMI reduction. After the input signals have been latched, pins 5, 7, 8, 9, and 11 serve as 50 MHz frequency outputs.

Connecting a bi-directional pin

A bi-directional pin serves as input upon power-up, and as output as soon as the inputs have been latched. The value of the input is latched-in upon power-up. Depending on the pin (see pin description), the input can be tri-level or a standard two-level. Unlike unidirectional pins, bi-directional pins cannot be connected directly to GND or VDD in order to set the input to "0" or "1", since the pin also needs to serve as output. In the case of two level input pins, an internal pull-up resistor is present. This allows a default value to be set when no external pull down resistor is connected between the pin and GND (by definition, a tri-level input has a the default value of "M" (mid) if it is not connected). In order to connect a bi-directional pin to a non-default value, the input must be connected to GND or VDD through an external pull-down/pull-up resistor. ***Note:*** *when the output load presents a low impedance in comparison to the internal pull-up resistor, the internal pull-up resistor may not be sufficient to pull the input up to a logical "one", and an external pull-up resistor may be required.*

For bi-directional inputs, the external loading resistor between the pin and GND has to be sufficiently small (compared to the internal pull-up resistor) so that the pin voltage be pulled below 0.8V (logical "zero"). In order to avoid loading effects when the pin serves as output, the value of the external pull-down resistor should however be kept as large as possible. In general, it is recommended to use an external resistor of around one sixth to one quarter of the internal pull-up resistor (see Application Diagram). ***Note:*** *when the output is used to drive a load presenting an small resistance between the output pin and VDD, this resistance is in essence connected in parallel to the internal pull-up resistor. In such a case, the external pull-down resistor may have to be dimensioned smaller to guarantee that the pin voltage will be low enough achieve the desired logical "zero". This is particularly true when driving 74FXX TTL components.*

APPLICATION DIAGRAM



NOTE: Rup=120kΩ for 50MHz_OE (Pin2); Rup=60kΩ for FS(0:1). R starts from 1 to 0 while RB starts from 0 to 1.

Electrical Specifications

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. AC Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency		10	25	27	MHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns
Duty Cycle*	At V_{DD} /2	45	50	55	%
Max. Absolute Jitter	Short term		±150		ps
Max. Jitter, cycle to cycle				80	ps

* : in case SDRAM output is selected to be 83.3MHz, the duty cycle of output pin 22 will be 40%-60% if its output frequency is selected to be 100MHz (FS2=1). In all other situations, pin 22 will also have a 50%-50% typical duty cycle.

3. DC Specifications

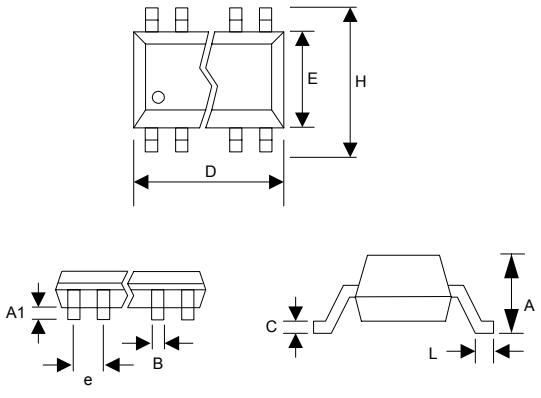
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	V_{DD}		2.97		3.63	V
Input High Voltage	V_{IH}			V_{DD} /2		V
Input Low Voltage	V_{IL}			V_{DD} /2	V_{DD} /2 - 1	V
Input High Voltage	V_{IH}	For all Tri-level input	V_{DD} -0.5			V
Input Low Voltage	V_{IL}	For all Tri-level input			0.5	V
Input High Voltage	V_{IH}	For all normal input	2			V
Input Low Voltage	V_{IL}	For all normal input			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25mA			0.4	V
Output High Voltage At CMOS Level	V_{OH}	I_{OH} = -8mA	V_{DD} -0.4			V
Operating Supply Current	I_{DD}	No Load		35		mA
Short-circuit Current	I_S			±50		mA
Nominal output current*	I_{out}	CMOS output level	35	40		mA
Nominal output current*	I_{out}	TTL output level	20	25		mA
Internal pull-up resistor	R_{up}	Pins 5,7		60		kΩ
Internal pull-up resistor	R_{up}	Pin 2		120		kΩ

*: SDRAM output strengths are doubled (i.e. min. CMOS level is 70mA, typ. CMOS level is 80mA)

PACKAGE INFORMATION

16 PIN Narrow SOIC (mm)

	SOIC	
Symbol	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
H	5.80	6.20
L	0.40	1.27
e	1.27 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL650-03 S C

PART NUMBER

TEMPERATURE
C=COMMERCIAL
I=INDUSTRAL

PACKAGE TYPE
S=SOIC

Order Number	Marking	Package Option
PLL650-03SC-R	P650-03SC	SOIC - Tape and Reel
PLL650-03SC	P650-03SC	SOIC - Tube