PI0512WS
512-Pixel 50-*m*m-Pitch Wide Aperture Spectroscopic Photodiode Array
Engineering Data Sheet

Description

Peripheral Imaging Corporation's WS series is family of self-scanning photodiode solid-state linear imaging arrays. These photodiode sensors employ PIC's proprietary CMOS Image Sensing Technology to integrate the sensors into single monolithic chip. These sensors are optimally designed for applications in spectroscopy. Accordingly, these sensors contain a linear array of photodiodes with an optimized geometrical aspect ratio (50-*m*m aperture pitch x 2500-*m*m aperture width) for helping to maintain mechanical stability in spectroscopic instruments and for providing their light-capturing ability. The family of sensor consists of active photodiode arrays of different number of pixels, 256 and 512.
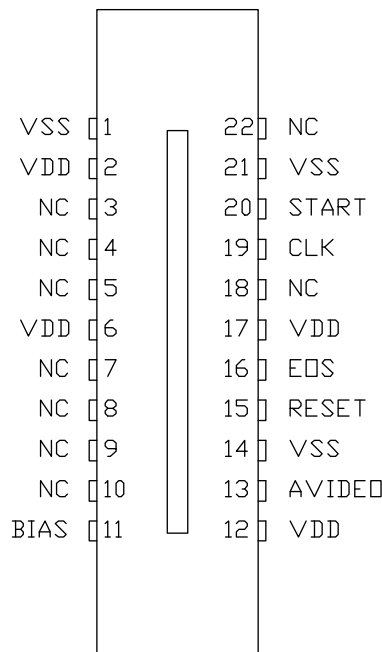
```
VSS  [1       22]  NC
VDD  [2       21]  VSS
NC   [3       20]  START
NC   [4       19]  CLK
NC   [5       18]  NC
VDD  [6       17]  VDD
NC   [7       16]  EOS
NC   [8       15]  RESET
NC   [9       14]  VSS
NC   [10      13]  AVIDEO
BIAS [11      12]  VDD
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Figure 1. Pinout configuration.

The WS series devices are mounted in 22-pin ceramic side-brazed dual-in-line packages that will insert in a standard DIP socket. A diagram of the package and its pinout configuration is seen in Figure 1.

Features

- High saturation capacitance (60pF) for wide dynamic range.
- Wide spectral response (180-1000) for UV and IR response.
- PN junction photodiodes highly resistive to UV damage.
- Low dark current.
- Integration time from 0.52 ms to 0.6 seconds at room temperature.
- Longer integration time extended to hours by cooling.
- High linearity.
- Low power dissipation.
- Geometrical structure to enhance stability and registration.
- Standard 22-lead dual-in-line integrated-circuit package.

Sensor Characteristics

The Peripheral Imaging Corporation's self-scanned photodiodes are on 50-μm center-to-center spacing. Hence, their line density 20 diodes/mm and accordingly the overall die lengths of the different arrays vary with the number of photodiodes. For example, the 256-pixel array is 12.8-mm long and the 512 pixel array is 25.6-mm long. In addition, each array has four additional dummy, non-imaging photodiodes with two on each side. The height of the sensors is 2500 µm. Accordingly, these slit-like apertures make these sensors desirable for coupling to monochromators and spectrographs.
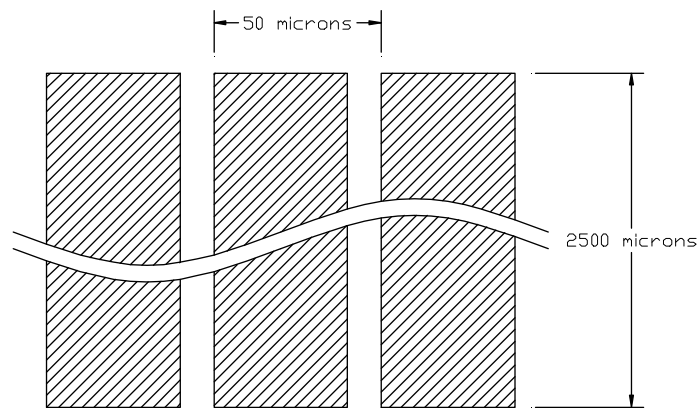

Figure 2. Geometry and layout of photodiode pixels.

During normal operation, the impinging photons in or near the PN photodiode junction generate free charges that are collected and stored on the junction's depletion capacitance. Since on average a certain fraction of charge is generated and collected for each impinging photon, the number of collected charges will proportionally increase with light exposures. Figure 3 shows the stored signal charge as function of light exposure at a wavelength of 575 nm. The exposure is the product of the light intensity in nW/cm^2 and integration time in seconds. The charge accumulates linearly until reaching the saturation charge where the corresponding exposure is the saturation exposure.
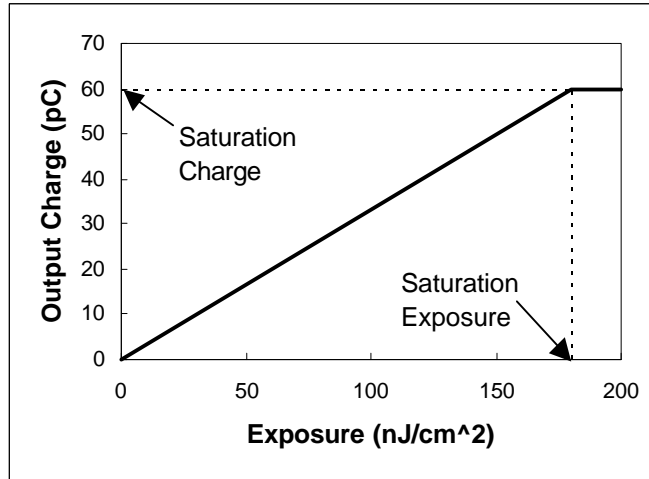

Figure 3. Stored signal charge as function of exposure at a wavelength of 575 nm.

The responsivity is defined as ratio of saturation charge divided by saturation exposure. The measured typical responsivity of a photodiode is 3.3×10^{-4} $C/J/cm^2$ at 575 nm. Figure 4 shows the predicted responsivity of the photodiodes as a function of wavelength.
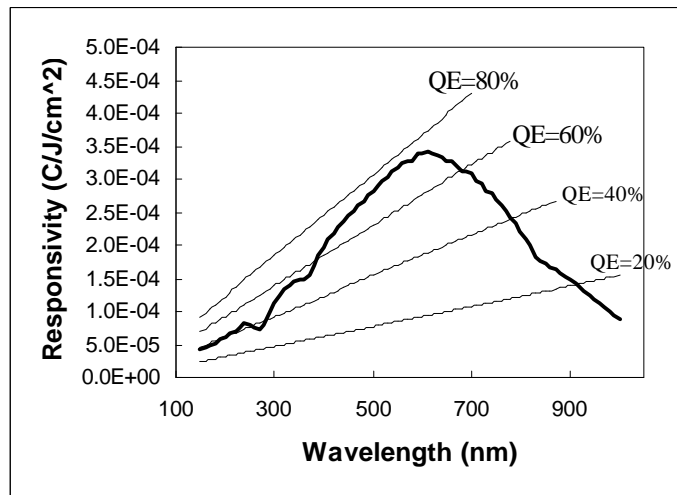

Figure 4. Predicted spectral response.

Note: Quantum Efficiency (QE) can be calculated by dividing the responsivity by the area of the sensor's element and multiplying the resulting ratio by the energy per photon in electron volts (eV).

The dark current is typically about 1 pA at 25^{o}C and will vary as function of temperature. The dark current will contribute dark-signal charges and these charges will increase as direct function of integration time and superimpose on the image signal charges.

Self-Scanning Circuit

Figure 5 shows a simplified electrically equivalent circuit diagram of the photodiode array. Every photodiode in the array is connected to a common output video line by a MOS switch. Impinging photons generate charge that is collected on each imaging photodiode when the switch is open. As the shift register sequentially closes each MOS switch, the stored charge, which is proportional in amount to the light exposure, from each corresponding photodiode is readout onto the video line. The output charge on the video line from each photodiode pixel is typically sensed by an external charge-integrating amplifier. The shift register is activated with the entry of the start pulse. This pulse propagates through each shift register stage and activates the MOS switches sequentially. When the pulse reaches the last shift register stage, the fourth and last dummy pixel is readout and end-of-scan (EOS) output is held high for one clock cycle.
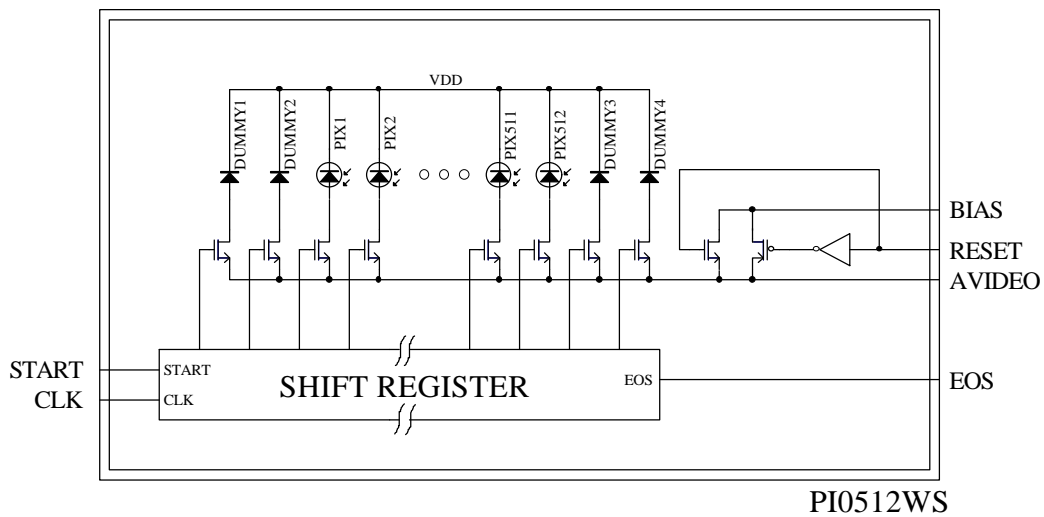

Figure 5. Simplified circuit diagram of PI0512WS photodiode array.

I/O Pins

Although the PI0512WS package has 22 pins as shown in Figure 1, there are only 6 functionally active I/O pins in addition to the supply and bias pins as shown in Figure 5. Table 1 defines the I/O acronyms, provides their full names and describes their functions. In essence, only two clocks, CLK and START, are required for controlling the timing of the sensor's video readout if the internal reset circuitry is not used. However, if the internal reset circuitry is used, a third clock signal, RESET, is required. The remaining I/O descriptions are for the video signal output, the end-of-scan signal, and the bias and supply voltage. These I/Os are listed with their acronym designators and functional descriptions in the following Table 1.

Table 1. Symbols and functions and I/O pins.

Symbol	Function and Description
VSS	Ground.
VDD	+5.0 Volts.
START	Start Pulse: Input to start the line scan.
CLK	Clock Pulse: Input to clock the shift register.
EOS	End Of Scan: Output from the shift register to indicate the completion of one line scan.
AVIDEO	Active Video Line: Charge output from the photodiodes pixels.
RESET	Reset Control Gate: Pulsing this input will reset the video line to the reset bias.
BIAS	Reset Bias Supply: Input bias reference resetting the video line.

Clock and Voltage Requirements

Clocks requirements are relatively simple. As it was indicated in Figure 5 and Table 1, there are only three input signals that require clocked inputs. They are CLK, the clock for the shift register, START, the shift register start pulse, and RESET, the reset control gate. However, in certain applications where the internal reset circuitry is unused, RESET can be tied to ground.
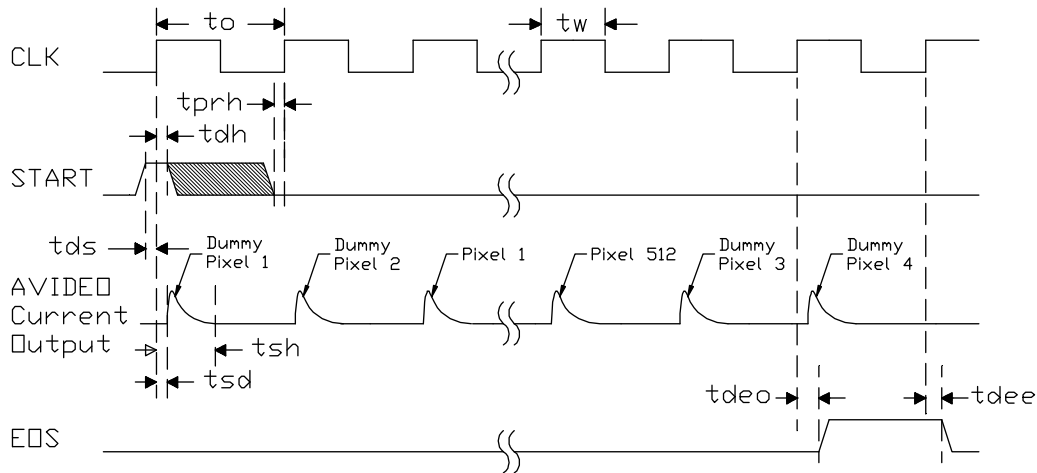

Figure 6. Timing diagram.

Table 2 . Symbol definitions and timing specifications for timing diagram.

Item	Symbol	Min	Typical	Max	Units
Clock cycle time	to	5			μs
Clock pulse width	tw	1			μs
Clock duty cycle		20	50	80	%
Prohibit crossing time of Start Pulse	tprh	0			ns
Data setup time	tds	50			ns
Data hold time	tdh	100			ns
End Of Scan delay	tdeo			300	ns
End Of Scan off	tdee			300	ns
Signal delay time	tsd	50			ns
Signal settling time	tsh			500	ns

The timing specifications and the symbol definition for Figure 6 are listed in Table 2. The control clock amplitudes for I/Os are compatible with the 5-Volt CMOS devices.

Recommended Operating Conditions at Room Temperature

Table 3 lists the recommended operational conditions.

Table 3. Recommended operating conditions at room temperature.

Parameters	Symbol	Min.	Typical	Max.	Units
Power supply	VDD	4.5	5.0	5.0	Volts
Input clock pulses high level [1]	Vih	VDD – 0.8	VDD	VDD	Volts
Input clock pulse low level [1]	Vil	0.0	0.0	0.8	Volts
Video output bias levels (dark)	Vbias	0.0	0.5	2.5	Volts
Clock frequency [2]	Fclk		100	1000	kHz
Clock pulse duty cycle		20	50	80	%
Integration time [3]	Tint	0.52		600	ms

Notes:
(1) Applies to all control-clock inputs.
(2) The minimum clock frequency must be consistent with the integration time as indicated in note (3).
(3) Integration time is specified at room temperature such that the maximum dark current charge build up in each pixel is less than 10% of the typical saturation charge. Accordingly, it can be as short as 0.52 ms or as long as 0.6 seconds at room temperature Longer integration times are possible by cooling the device.

Package Dimensions
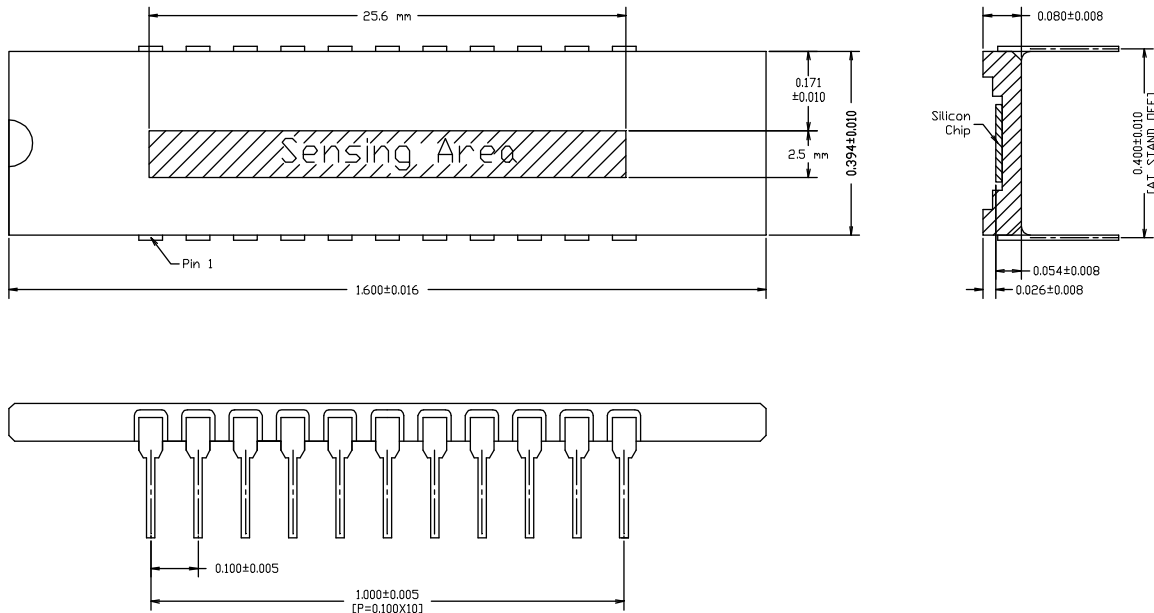
Note: Dimensions are in inches except where millimeters (mm) are indicated.

Electro-Optical Characteristics (25^{o}C)

Table 4 lists the electro-optical characteristics of PI0512WS sensor chip at 25^{o}C.

Table 4. Electro-optical characteristics.

Parameters	Symbol	Min	Typical	Max	Units
Center-to-center spacing			50		mm
Aperture width			2500		mm
Pixel area	A		1.25×10^{-3}		cm^2
Fill factor [1]	FF		76		%
Quantum efficiency [1,2]	QE		75		%
Responsivity [1,2]	R		3.3×10^{-4}		C/J/cm^2
Nonuniformity of response [3]			2	5	+/-%
Saturation exposure [2]	Esat		180		nJ/cm^2
Saturation charge	Qsat	55	60		pC
Average dark current [4]			1	3	pA
Spectral response peak	λ		600		nm
Spectral response range [5]			180 – 1000		nm

Notes:
(1) Fill factor, quantum efficiency, and responsivity are related by the equation R = $(q_e\lambda/hc)^.$QE$^.$FF$^.$A, where q_e is the charge of an electron and hc/λ is the energy of a photon at a given wavelength.
(2) At wavelength of 575 nm (yellow-green) and with no window.
(3) Measured at 50% Vsat with incandescent tungsten lamp filtered with a Schott KG-1 heat-absorbing glass.
(4) Max dark leakage $\leq$ 1.5 x average dark leakage measured with an integration period of 500 ms at 25^{o}C.
(5) From 250-1000 nm, responsivity $\geq$ 20% of its peak value.