



PH3120L

N-channel TrenchMOS™ logic level FET

Rev. 02 — 20 January 2005

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low thermal resistance
- Logic level gate drive
- SO8 equivalent area footprint
- Very low on-state resistance

1.3 Applications

- DC-to-DC converters
- Portable appliances
- Switched-mode power supplies
- Notebook computers

1.4 Quick reference data

- $V_{DS} \leq 20 \text{ V}$
- $I_D \leq 100 \text{ A}$
- $P_{tot} \leq 62.5 \text{ W}$
- $R_{DSon} \leq 2.65 \text{ m}\Omega$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source	 Top view SOT669 (LFPAK)	
4	gate		
mb	mounting base; connected to drain		

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3. Ordering information

Table 2: Ordering information

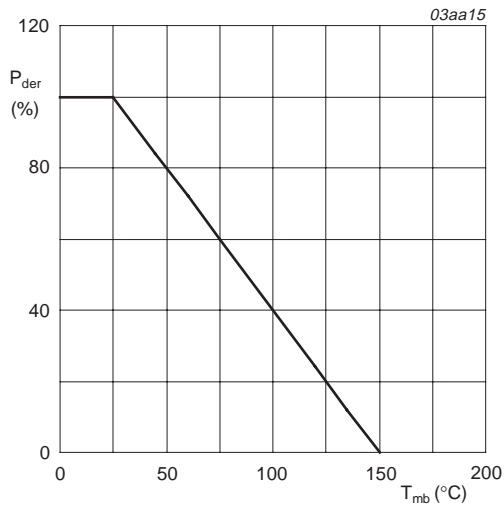
Type number	Package		Version
	Name	Description	
PH3120L	LFPAK	plastic single-ended surface mounted package; 4 leads	SOT669

4. Limiting values

Table 3: Limiting values

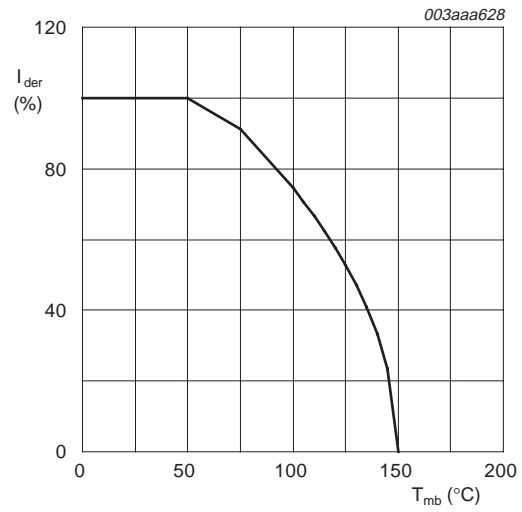
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2 and 3	-	100	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2	-	76	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	300	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	152	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 46.2\text{ A};$ $t_p = 0.32\text{ ms}; V_{DD} \leq 20\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V};$ starting at $T_j = 25\text{ °C}$	-	210	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

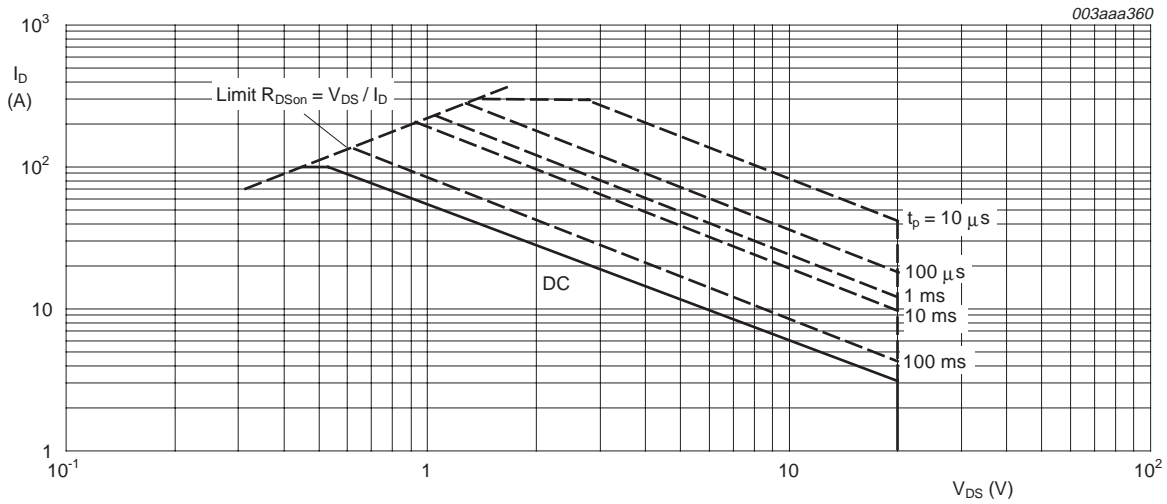
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$$V_{GS} \leq 10\text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig. 2. Normalized continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance

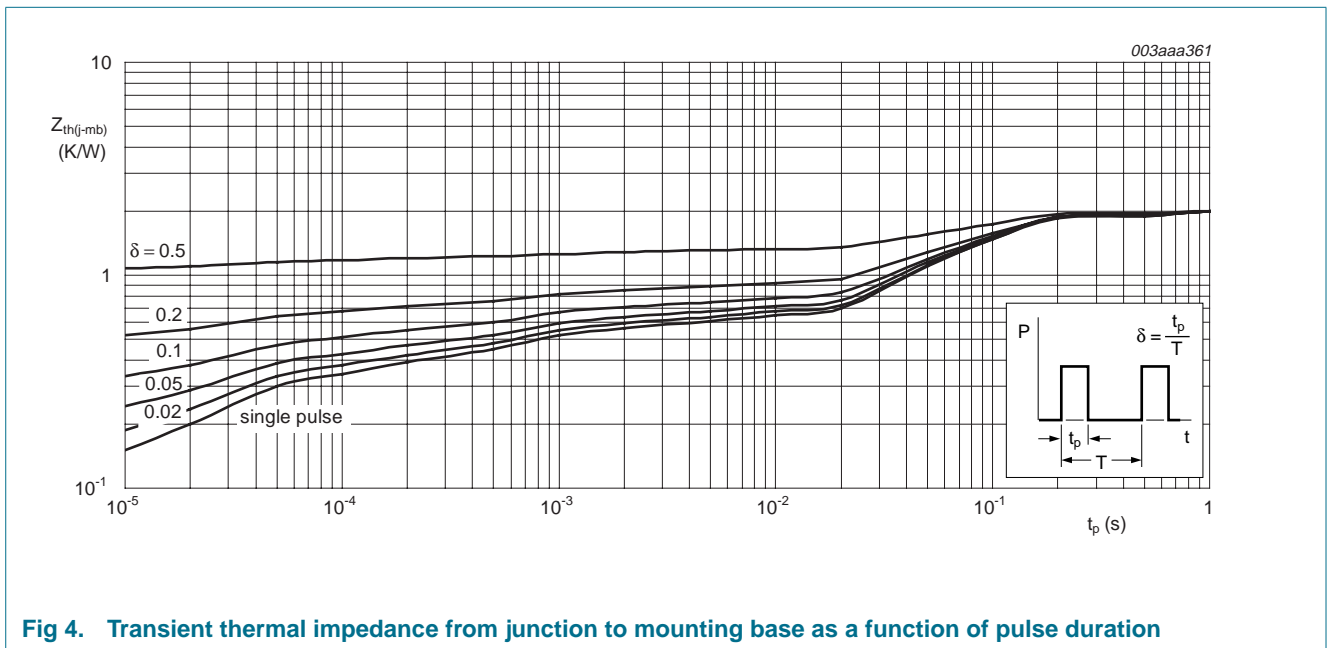
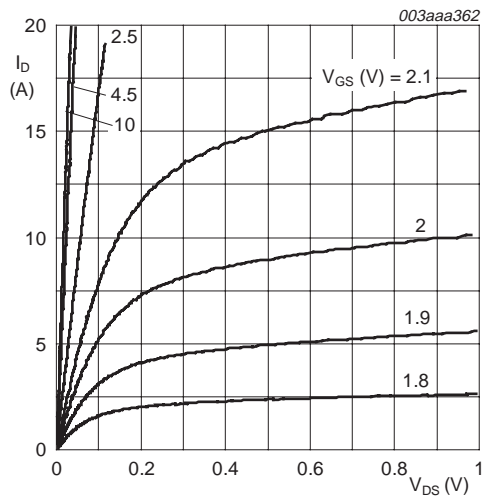


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

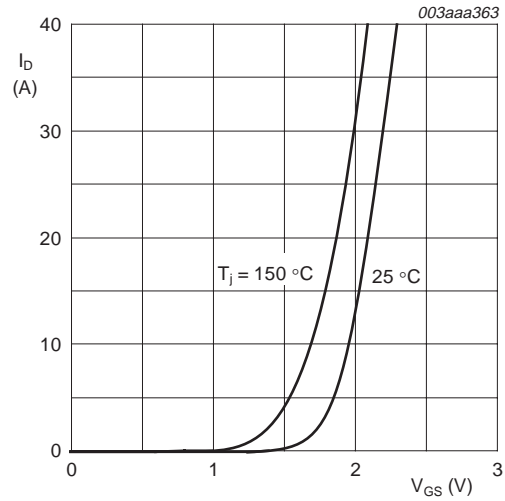
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 10 mA; V _{GS} = 0 V	20	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9 and 10				
		T _j = 25 °C	1	1.5	2	V
		T _j = 150 °C	0.65	-	-	V
I _{DSS}	drain-source leakage current	V _{DS} = 20 V; V _{GS} = 0 V				
		T _j = 25 °C	-	0.06	1	μA
		T _j = 150 °C	-	-	500	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±15 V; V _{DS} = 0 V	-	2	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; Figure 7 and 8				
		T _j = 25 °C	-	3	3.7	mΩ
		T _j = 150 °C	-	5.1	6.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; Figure 7 and 8	-	2.25	2.65	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = 50 A; V _{DD} = 10 V; V _{GS} = 4.5 V; Figure 13	-	48.5	-	nC
Q _{gs}	gate-source charge		-	12.7	-	nC
Q _{gd}	gate-drain (Miller) charge		-	12.8	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 10 V; f = 1 MHz; Figure 11	-	4457	-	pF
C _{oss}	output capacitance		-	1480	-	pF
C _{rss}	reverse transfer capacitance		-	940	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 10 V; I _D = 25 A;	-	34	-	ns
t _r	rise time	V _{GS} = 4.5 V; R _G = 4.7 Ω	-	90	-	ns
t _{d(off)}	turn-off delay time		-	114	-	ns
t _f	fall time		-	88	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 25 A; V _{GS} = 0 V; Figure 12	-	0.77	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V	-	63	-	ns



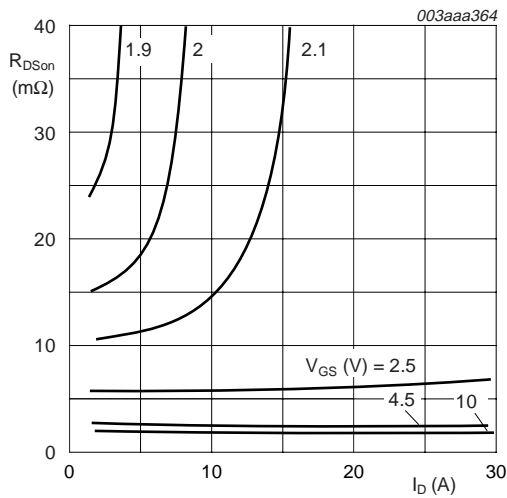
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



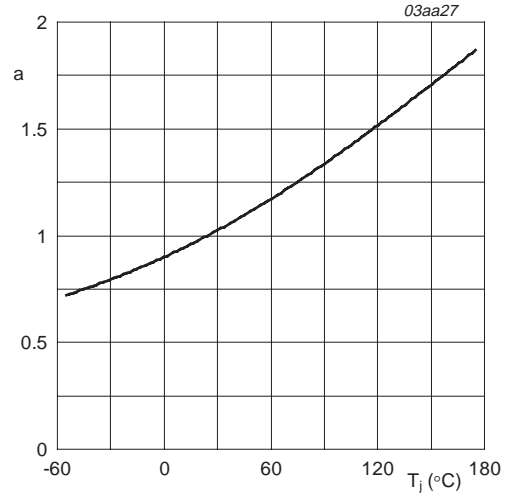
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



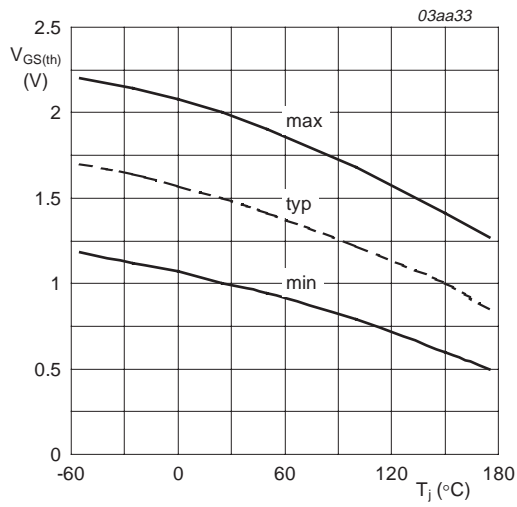
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



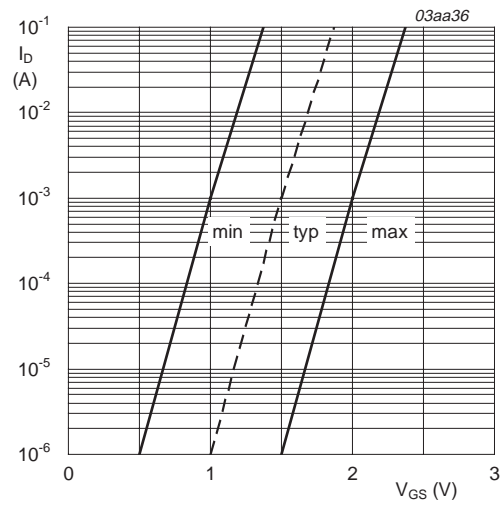
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



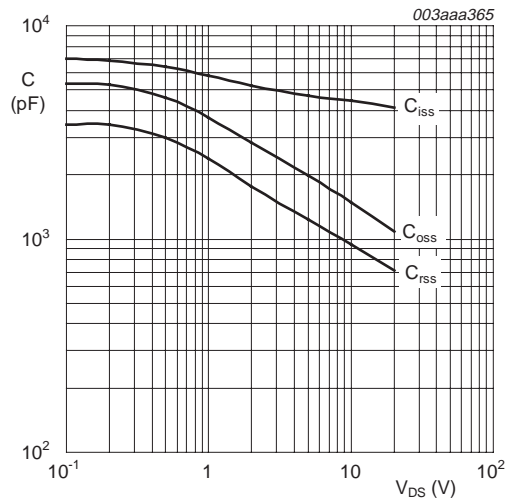
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



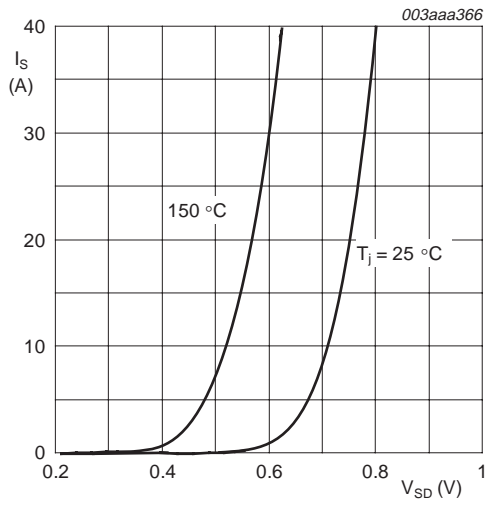
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



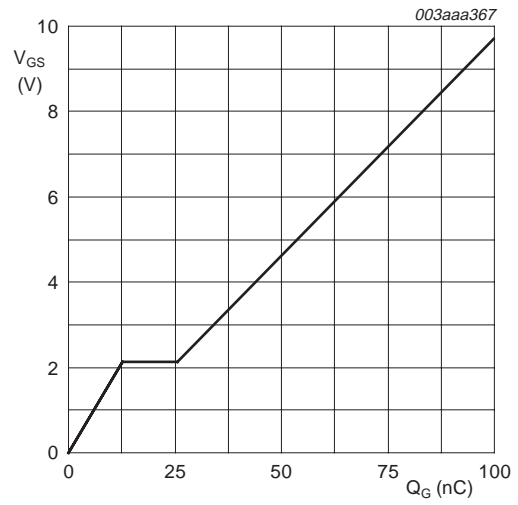
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ\text{C}$ and 150°C ; $V_{GS} = 0$ V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



$I_D = 50$ A; $V_{DD} = 10$ V

Fig 13. Gate-source voltage as a function of gate charge; typical values

7. Package outline

Plastic single-ended surface mounted package (LFPAK); 4 leads

SOT669

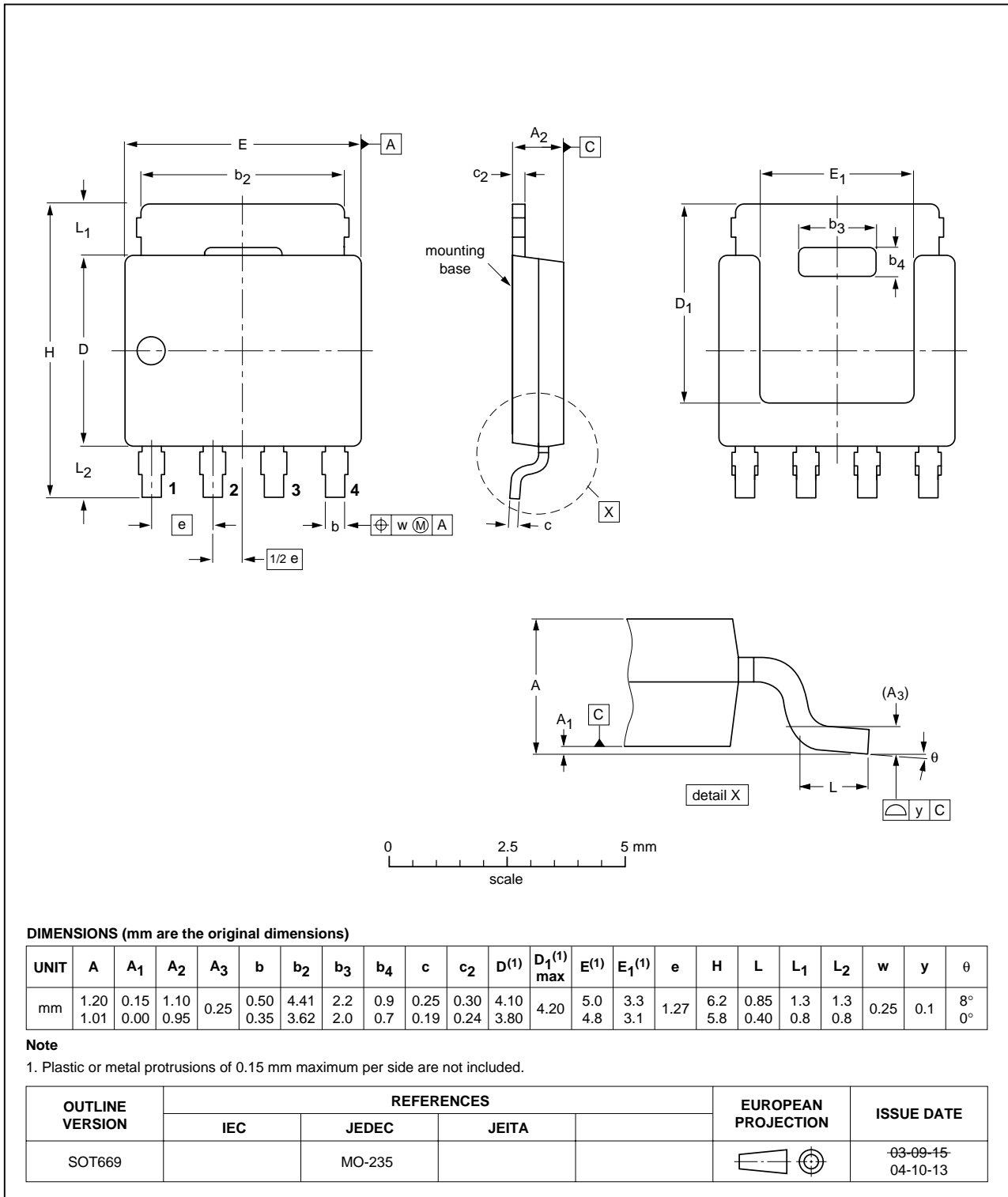


Fig 14. Package outline SOT669 (LF-PAK)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH3120L_2	20050120	Product data sheet	-	9397 750 14089	PH3120L-01
Modifications:					
			<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.• R_{DSon} data updated in Section 1.4 “Quick reference data” and Section 6 “Characteristics”• Figure 2 and 3 updated		
PH3120L-01	20040304	Preliminary data	-	9397 750 12812	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
5.1	Transient thermal impedance	4
6	Characteristics	5
7	Package outline	9
8	Revision history	10
9	Data sheet status	11
10	Definitions	11
11	Disclaimers	11
12	Trademarks	11
13	Contact information	11



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