Product Brief

PE42693 DIE

SP9T UltraCMOS™ 2.75 V Switch 100 – 3000 MHz, +68 dBm IIP3

Figure 1. Functional Diagram

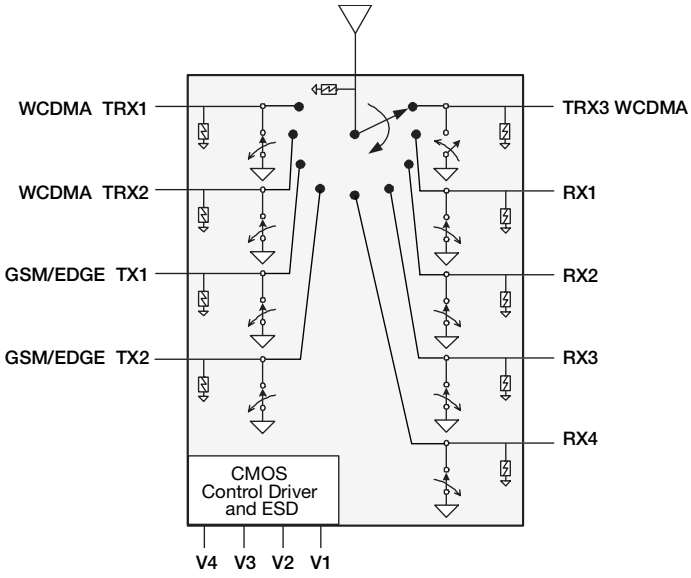
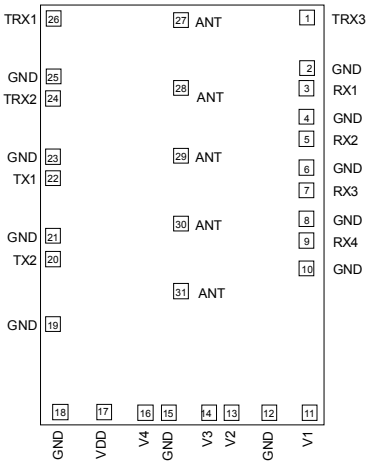
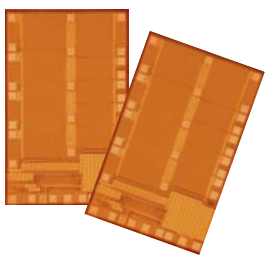


Figure 2. Die Top View



Note: Redundant antenna pads for flexible impedance matching

Figure 3. Package Type: Wirebond Die



Features

- Two GSM/PCS/EDGE compliant TX ports, three TRX ports (WCDMA band or receive), and four RX ports
- Four pin CMOS logic control with integral decoder/driver
- Exceptional harmonic performance: $2f_o$ = -87 dBc and $3f_o$ = -76 dBc
- Low TRX insertion loss: 0.7 dB at 900 MHz, 0.9 dB at 1900 MHz
- TX – RX Isolation of 51 dB at 900 MHz, 45 dB at 1900 MHz
- 1500 V HBM ESD tolerance all ports
- +68 dBm IIP3 @ 50 Ω
- -110 dBm IMD3
- No blocking capacitors required

Product Description

The PE42693 is a HaRP™-enhanced SP9T RF Switch developed on the UltraCMOS™ process technology. It addresses the specific design needs of the Quad-Band GSM Handset Antenna Switch Module Market for use in GSM/ PCS/EDGE/DCS/WCDMA handsets. The switch is comprised of two transmit ports that can be used for GSM/PCS/EDGE, three transmit/receive ports (TRX1, TRX2 and TRX3) that can be used for either WCDMA or as receive ports, and four symmetric receive ports. An on-chip CMOS decode logic facilitates four-pin low voltage CMOS control. High ESD tolerance of 1500 V at all ports, no blocking capacitor requirements, and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Table 1. Target Electrical Specifications @ +25 °C, V_{DD} = 2.75 V (Z_S = Z_L = 50 Ω)

Parameter	Condition	Typ	Units
Insertion Loss[1]	TRX - Ant (850 WCDMA) TRX - Ant (1950 / 2140 WCDMA) TX - Ant (850 / 900) TX - Ant (1800 / 1900) RX - Ant (850 / 900) RX - Ant (1800 / 1900)	0.7 0.8 / 0.9 0.7 0.85 1.1 1.25	dB dB dB dB dB dB
Return Loss	All Ports in On State	20	dB
Isolation	TX - RX (850 / 900) TX - RX (1800 / 1900) TRX - RX (850 / 900) TRX - RX (2200) TX - TRX (850 / 900) TX - TRX (2200) TX - TX (850 / 900) TX - TX (1800 / 1900)	51 45 43 34 34 28 31 26	dB dB dB dB dB dB dB dB
2nd Harmonic[2]	TX 850/900 MHz, +35 dBm output power, 50 Ω TX 1800/1900 MHz, +33 dBm output power, 50 Ω	-87 -86	dBc dBc
3rd Harmonic[2]	TX 850/900 MHz, +35 dBm output power, 50 Ω TX 1800/1900 MHz, +33 dBm output power, 50 Ω	-76 -77	dBc dBc
WCDMA Band I IMD3	TRX – Measured in a 50 Ω system at 2.14 GHz at the TX1 port. Input signals are referenced to the ANT port with +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz	-110	dBm
WCDMA Band I IIP3	TRX – Measured in a 50 Ω system at 2.14 GHz at the TX1 port. Input signals are referenced to the ANT port with +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz	+68	dBm
Switching time	50% of control to (10/90%) RF	2	µs

Notes: 1. Insertion loss specified with optimal ANT impedance matching with the outermost ANT bondpad.
2. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.

Note: All datasheet parameters are tested and specified using only the antenna pad connection closest to edge of the die. Additional antenna pad connections have been added to allow customers to select different wirebond lengths which can be used to optimize performance.

Table 2. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Units
Temperature range	T_{OP}	-40		+85	°C
V_{DD} Supply Voltage	V_{DD}	2.65	2.75	3.2	V
I_{DD} Power Supply Current (V_{DD} = 2.6V)	I_{DD}		13	20	µA
TX input power[3] (VSWR 3:1)	P_{IN}			+35	dBm
RX input power[3] (VSWR 3:1)	P_{IN}			+20	dBm
Control Voltage High	V_{IH}	1.4			V
Control Voltage Low	V_{IL}			0.4	V

Note: 3. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.

Part performance is not guaranteed under these conditions. Exposure to absolute maximum conditions for extended periods of time may adversely affect reliability. Stresses in excess of absolute maximum ratings may cause permanent damage.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any DC input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	+150	°C
T_{OP}	Operating temperature range	-40	+85	°C
P_{IN}(50 Ω)	TX input power (50 Ω)[4,5]		+38	dBm
	TRX input power (50 Ω)[4,5]		+35	
	RX input power (50 Ω) [4,5]		+23	
P_{IN} (∞ :1)	TX input power (VSWR ∞ :1) [4,5]		+35	dBm
	TRX input power (VSWR ∞ :1)[4,5]		+32	
V_{ESD}	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1500	V
	ESD Voltage (MM, JEDEC, JESD22-A114-B)		100	V

Notes: 4. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.
5. V_{DD} within operating range specified in Table 2.

Table 4. Pin Descriptions

Pad #	Pad Name	Description
1	TRX3[7]	RF I/O – TRX3
2	GND[6]	Ground
3	RX1[7]	RF I/O – RX1
4	GND[6]	Ground
5	RX2[7]	RF I/O – RX2
6	GND[6]	Ground
7	RX3[7]	RF I/O – RX3
8	GND[6]	Ground
9	RX4[7]	RF I/O – RX4
10	GND[6]	Ground
11	V1[8]	Switch control input, CMOS logic level
12	GND[6]	Ground
13	V2[8]	Switch control input, CMOS logic level
14	V3[8]	Switch control input, CMOS logic level
15	GND[6]	Ground
16	V4[8]	Switch control input, CMOS logic level
17	VDD[8]	Supply
18	GND[6]	Ground
19	GND[6]	Ground
20	TX2[7]	RF I/O – TX2
21	GND[6]	Ground
22	TX1[7]	RF I/O – TX1
23	GND[6]	Ground
24	TRX2[7]	RF I/O – TRX2
25	GND[6]	Ground
26	TRX1[7]	RF I/O – TRX1
27	ANT[9]	RF Common – Antenna
28	ANT[9]	RF Common – Antenna
29	ANT[9]	RF Common – Antenna
30	ANT[9]	RF Common – Antenna
31	ANT[9]	RF Common – Antenna

Notes: 6. GND traces should be physically short and connected to ground plane for best performance.
7. Blocking capacitors needed only when non-zero DC voltage present.
8. Application must ensure at least 40 dB of voltage isolation from the RF signal.
9. Redundant antenna pads for flexible impedance matching.

Figure 4. Pad Configuration (Top View)

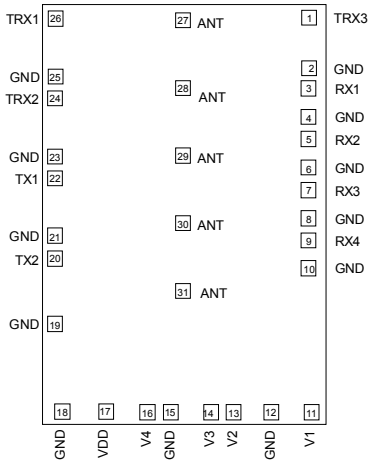


Table 5. Truth Table

Path	V4	V3	V2	V1
RX1-ANT	0	0	0	0
RX2-ANT	0	0	0	1
RX3-ANT	0	0	1	0
RX4-ANT	0	0	1	1
TX1-ANT	0	1	0	1
TX2-ANT	0	1	1	0
TRX1-ANT	1	1	0	0
TRX2-ANT	0	1	0	0
TRX3-ANT	1	0	0	1
ALL Off	Note	Note	Note	Note

Note: All unused logic states will turn all RF ports off.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 6. Ordering Information

Order Code	Package	Shipping Method
PE42693DTI	Wafer on Film Frame	Wafer (Gross Die / Wafer Quantity)
PE42693DBI	Die in Waffle Pack	238 Dice / Waffle Pack
EK-42693-01	Evaluation Kit	1/ box

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Data Sheet Identification

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Preliminary Specification

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Product Specification

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