Productivity Engineering
Gesellschaft für Prozessintegration mbH

PE12316
Triple
Incremental Encoder

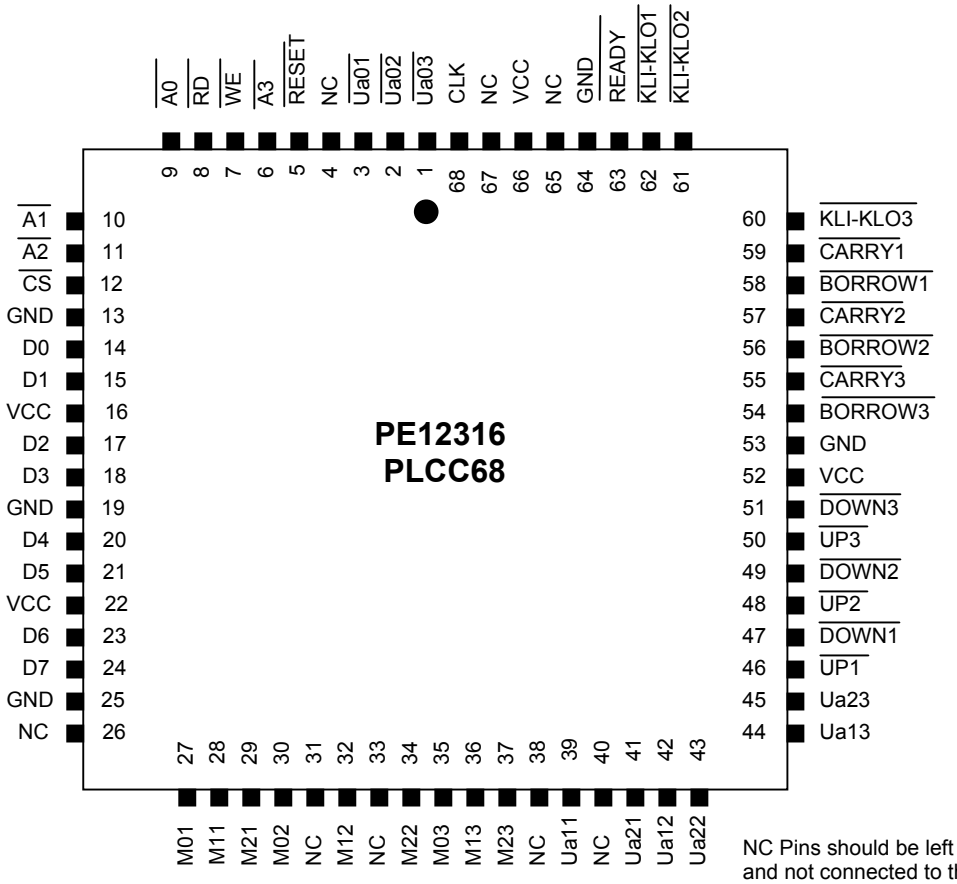
February 6, 2003 Preliminary (Version 1.1)

Features:

- Functional and pincompatible with TI CF32006 / THCT12316
- Three independent channels in one device
- Each channel compatible with PE12016
- Available as IP-Core or within PLCC68 Package
- Interfaces three mechanisms / axes to data bus
- Pulse width measurement
- Frequency measurement
- Cascadable 16-bit counters
- TTL compatible
- 5V and 3.3V Operation
- 8 Bit parallel tristatable Bus
- Simple read & write procedure
- High speed 20 MHz clock operation
- Direction discriminators identify & measure forward/backward rotation
- separate zero pulse input

New Feature:

- Each channel extendable to 24 Bit



NC Pins should be left open and not connected to the PCB. They are reserved for future upgrades.

Figure 1 Pinout

Description:

The PE12316 TRIPLE INCREMENTAL ENCODER INTERFACE consists of three channels each, which can independently determine the direction of displacement of a mechanical or axis based device on two input signals from transducers in quadrature. Alternatively, each channel can measure a pulse width using a known clock rate, or a frequency, by counting input pulses over a known time interval. It includes three 16/24-bit counters which may also be used separately. The PE12316 may be cascaded between channels on one device or between devices to provide accuracy greater than 16/24-bits, and is designed for use in many microprocessor-based systems.

Availability:

The PE12316 is available as a replacement IC or Netlist IP Core, fully compatible with the TI CF32006 functionality. The replacement IC is packaged within the popular PLCC68.

The IP Core can be targeted to any desired FPGA/CPLD or ASIC Technology and is delivered within the according netlist format. The database has been proven in a co-emulation together with the reference part by stimulating both devices with the same inputs and observing the identical results on the outputs.

Ressource Usage IP Core:

Gate count for ASIC Technologies is approximately 7000 Gates.

For FPGAs a technology with at least 20.000 FPGA Gates like XCS20 from Xilinx needs to be chosen.

Enhancements over CF32006:

The PE12316 has 3 counters with 24 Bit internally. Therefore an additional addressline /A3 is introduced on pin 6 to select the Bits 16-23 of each channel in conjunction with the other addressbits A0-A2.

NOTE: If /A3 is left unconnected, PE12316 is identical to CF32006.

Differences:

The PE12316 has some slight changes:
UA1X and UA2X are synchronized with the clock, eliminating the need to place a discrete ACT74 type Flipflop in front of these signals.

Due to this feature a latency of one clock cycle is introduced, resulting worst case in a +/-1 counter difference.

Applications:

The PE12316 enables mechanical devices to be interfaced with microprocessors. It may be used in many diverse applications, including robotics, tooling machines, elevators, conveyor belts and transport mechanisms. Since it contains three channels each PE12316 can support three measurements or axes of motion.

Architecture:

Within each channel there are four main elements:

1. The measurement and mode control logic generates up or down count pulses, internal signals I1 and I2, from:
   - Quadrature signals Ua1, Ua2 and zero pulse Ua0n*
   - Clock input
   - Mode controls M0n*, M1n* and M2n*
2. A 16-bit counter made up from two independently loadable 8-bit counters.
3. A 16-bit latch which “freezes” the counter value when required.
4. A multiplexer that allows the processor to read either upper or lower byte in the latch.

Supporting the three channels:

The control logic provides common micro-processor interface signals; the output multiplexer allows the processor to select data from one of the three channels and the three-state buffers place this data on the bus.

* The suffix n is a placeholder for either channel 1, channel 2 or channel 3 and will be used in this manner throughout the whole document.

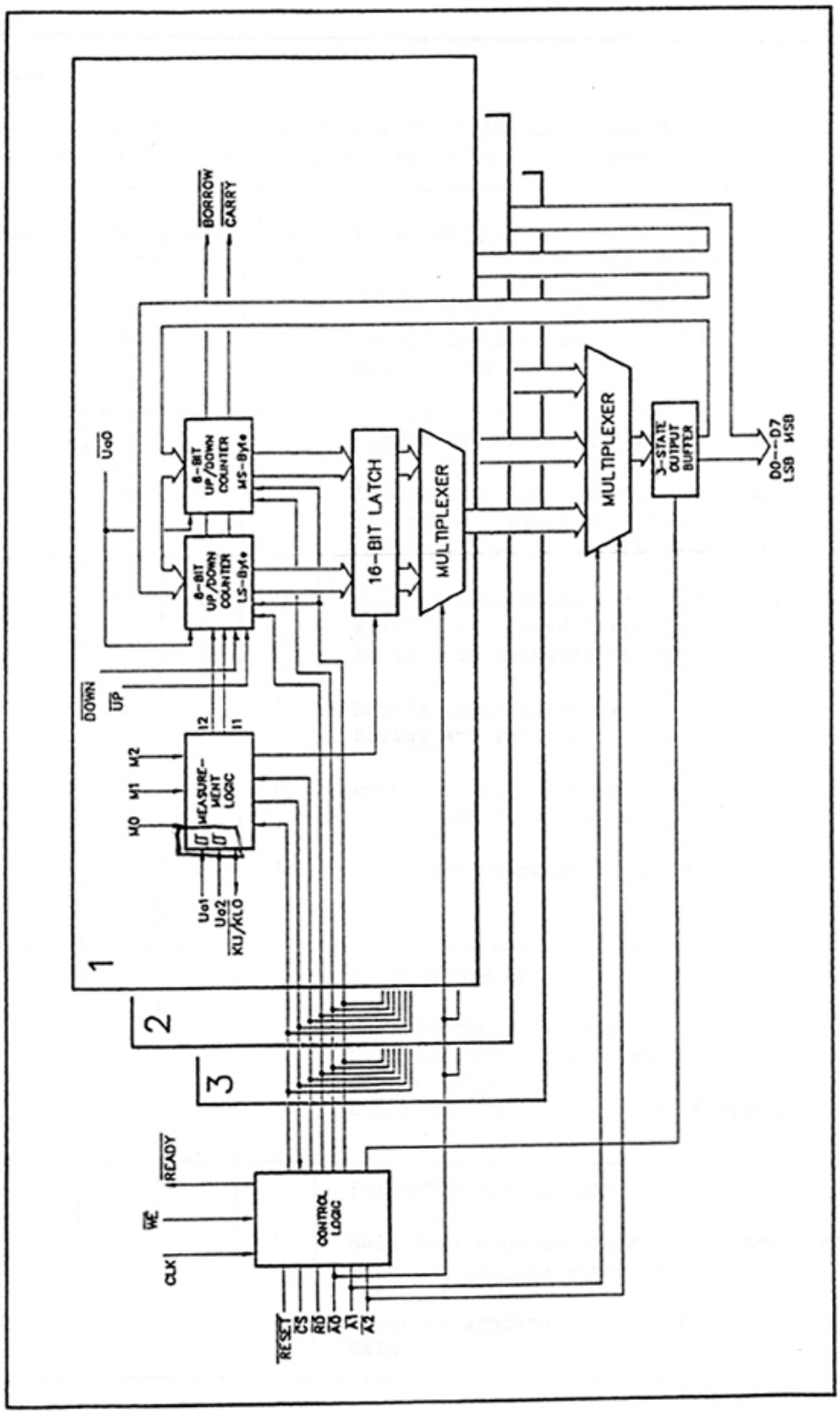


Figure 2 Block Diagramm for 16 Bit Mode

Operation:

The eight modes of operation of the PE12316 are summarized in ***Table 1***.

The modes of the three channels can be selected independently.

Mode	M2n	M1n	M0n	Mode Description
0	0	0	0	**COUNTER** 16-bit up/down counter (inhibits direction discriminator)
1	0	0	1	**DIRECTION DISCRIMINATOR** Single count pulse synchronous with Ua1n rising in forward direction and Ua1n falling in backward direction.
2	0	1	0	Single count pulse synchronous with Ua2n rising in forward direction and Ua2n falling in backward direction.
3	0	1	1	Double count pulse synchronous with Ua1n rising and falling.
4	1	0	0	Double count pulse synchronous with Ua2n rising and falling.
5	1	0	1	Quadruple count pulse synchronous with all edges.
6	1	1	0	**PULSE WIDTH MEASUREMENT** Ua1n is the gate signal Ua2n is high for up counting and low for down counting. Count is synchronous with rising clock.
7	1	1	1	**FREQUENCY MEASUREMENT** Ua1n is frequency signal to be measured Ua2n is the gate signal of known time interval. Count is synchronous with rising edge of Ua1n.

Table 1 Mode Description

Detailed Information about the different Modes:

Mode 0: 16-Bit Up/Down Counter Mode

In this mode the PE12316 may be used as three fast 16-bit synchronous up/down counters with cascade capability. This is operated using the /UP and /DOWN inputs.

The states of the counter outputs are transferred to a 16-bit latch. The contents of this 16-bit latch are multiplexed on a 8-bit parallel data bus (D0…D7) and enabled using /RD and /CS.

/A0 is the control input for the byte multiplexer. A high level at this input transfers the least significant byte to the data outputs; and a low level transfers the most significant byte.

The signals /A1 and /A2 select the channel for read or write according to the following table.

Channel number	/A1	/A2
1	H	H
2	L	H
3	H	L
No channel selected[1]	L	L

Table 2 Channel Selection

[1]Output buffers still selected if /RD and /CS active – data bus carries invalid data

The up/down counters are loaded in individual 8-bit bytes by the /WR and /CS signals, with the byte selected by the /A0 input, and the channel by the /A1 and /A2 inputs.

The counters and the control logic may be cleared all together using the /RESET signal. The counters are cleared individually using the /Ua0n signals.

Cascading to 32, 40, 48 or 56 bits is possible by connecting the /CARRY, /BORROW outputs of channel n with the /UP, /DOWN Inputs of the channel n+1. In cascaded mode the according /KLI-KLOn have to be connected together. For further details see ***Application Notes***.

Memory Map:

/A3	/A2	/A1	/A0	Channel	Content
1*	1	1	1	Channel 1	Bits 0-7
1*			0		Bits 8-15
0			1		Bits 16-23
1*	1	0	1	Channel 2	Bits 0-7
1*			0		Bits 8-15
0			1		Bits 16-23
1*	0	1	1	Channel 3	Bits 0-7
1*			0		Bits 8-15
0			1		Bits 16-23

* Defaultvalue due to internal pullup

Table 3 Memory Map

Mode 1-5: Direction Discriminator Modes

The quadrature signals Ua1n and Ua2n, identify forward or backward directions. If Ua1n leads Ua2n, the forward direction is indicated and the counter will count up; if Ua1n lags Ua2n, the reverse direction is indicated and the counter will count down.

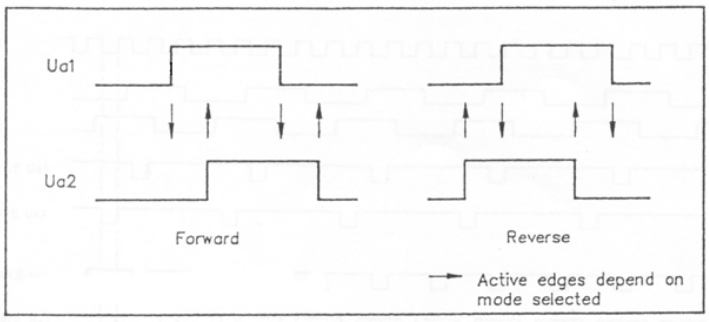


Figure 3 Direction Discriminator Modes

Ua1n and Ua2n are both stored in the first of a pair of consecutive D-type flip-flops on the clock falling edge, and transferred to the next on the clock rising edge.

By comparing the states of the four flip-flops and checking the mode inputs, the up or down count pulses are generated; see ***Figure 4*** and ***Figure 5***.

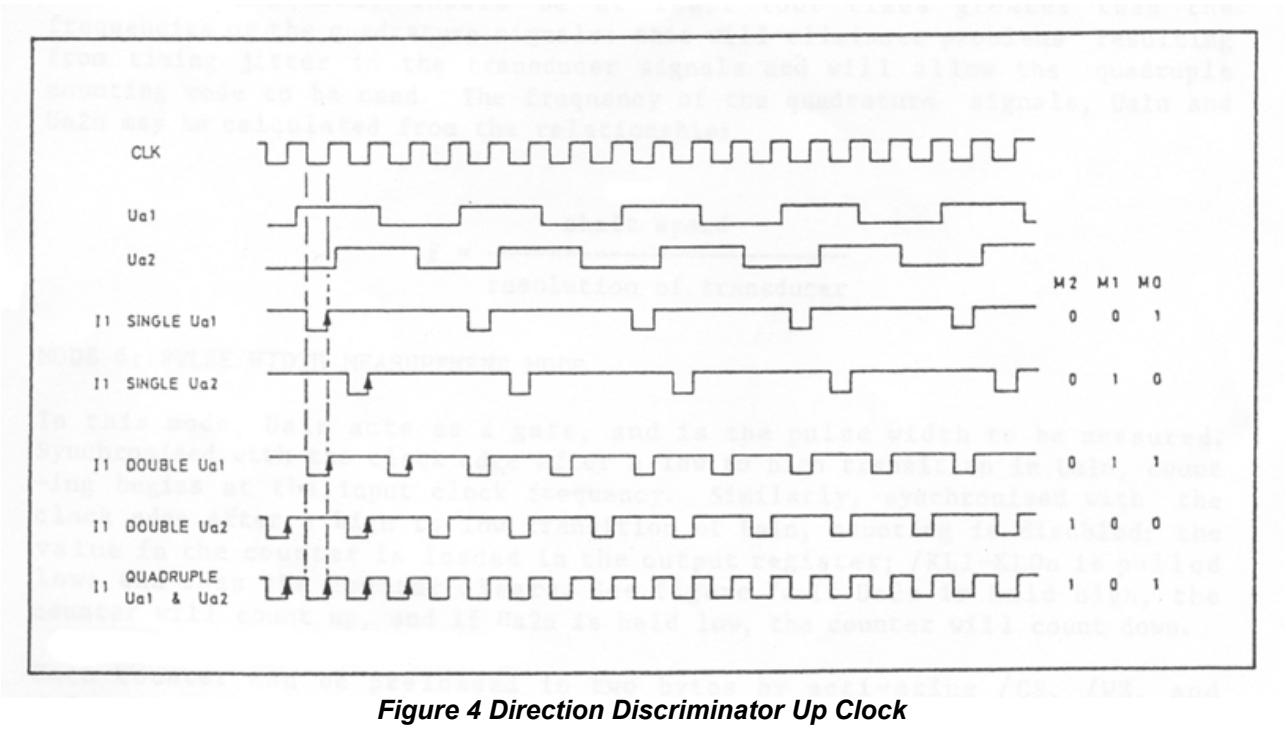


Figure 4 Direction Discriminator Up Clock

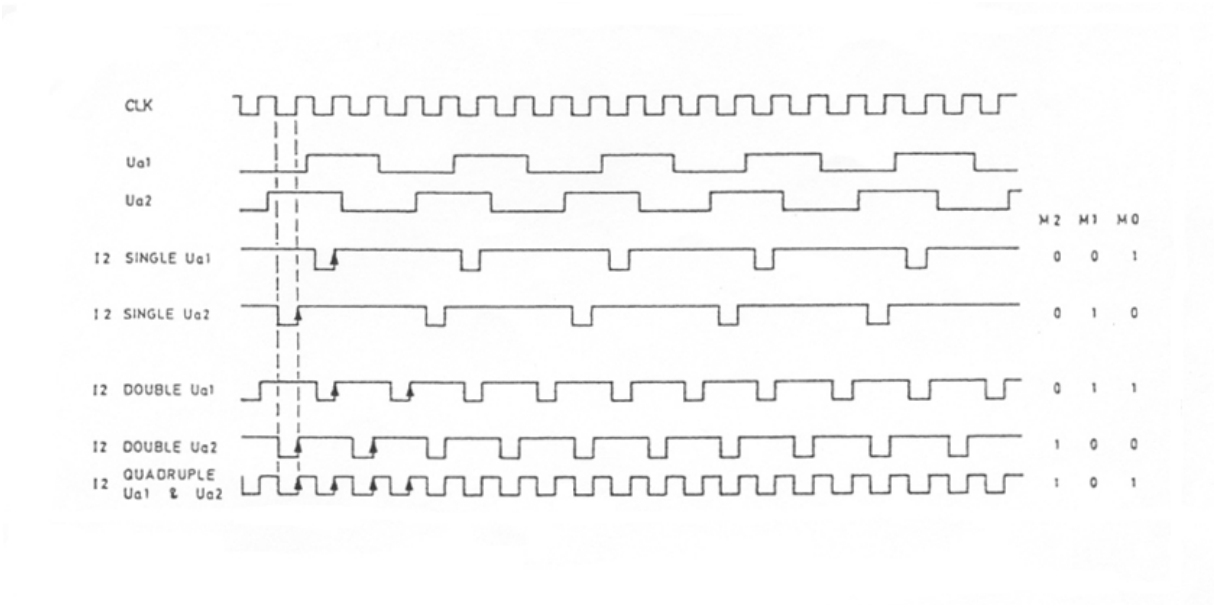


Figure 5 Direction Discriminator Down Clock

MODES 1 to 5 define which edge of the quadrature signals will be counted in accordance with ***Table 1***.

The clock frequency should be at least four times greater than the frequencies of the quadrature signals. This will eliminate problems resulting from timing jitter in the transducer signals and will allow the quadruple counting mode to be used. The frequency of the quadrature signals, Ua1n and Ua2n may be calculated from the relationship:

$$F = \frac{shaft\_speed}{resolution\_of\_transducer}$$

MODE 6: Pulse Width Measurement Mode

In this mode, Ua1n acts as a gate, and is the pulse width to be measured. Synchronised with the clock edge after a low to high transition in Ua1n, counting begins at the input clock frequency. Similarly, synchronised with the clock edge after a high to low transition of Ua1n, counting is disabled; the value in the counter is loaded in the output register; /KLI-KLOn is pulled low; and then the counter clears. See ***Figure 6***. If Ua2n is held high, the counter will count up, and if Ua2n is held low, the counter will count down.

Each counter can be preloaded in two or three bytes depending on 16 Bit or 24 Bit Mode by activating /CS, and /WE, and selecting the required byte with /A0 and /A3, and the required channel with /A1 and /A2.

This must be done while Ua1n is low. The output register should be read by activating /CS, /RD, and selecting the individual bytes with /A0 after Ua1n has fallen and before the next preload takes place.

The KLI-KLOn signal may be used as an interrupt to indicate to the processor when the output register has been loaded. In both the pulse width and frequency modes, the output register will not be loaded via /CS and /RD, but by the falling edge of Ua1n, or by pulling /KLI-KLOn low.

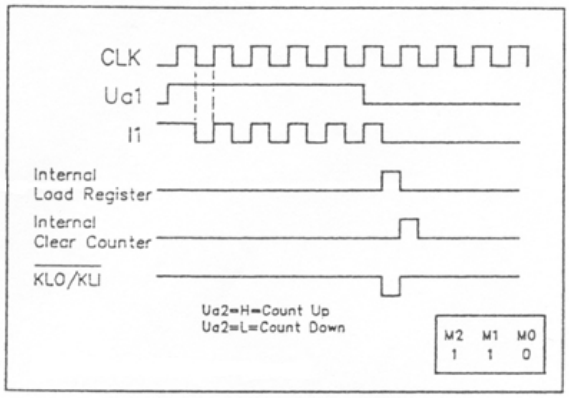


Figure 6 Pulse Width Measurement

MODE 7: Frequency Measurement Mode

In Mode 7, Ua1n is the signal of unknown frequency to be measured; Ua2n is a gate signal of known width. A low to high transition of Ua2n enables counting at the frequency of Ua1n.

When the gate (Ua2n) goes low, counting is disabled, the value of the counter is loaded into the output register, /KLI-KLOn is pulled low, and the counter is then cleared. See ***Figure 7***.

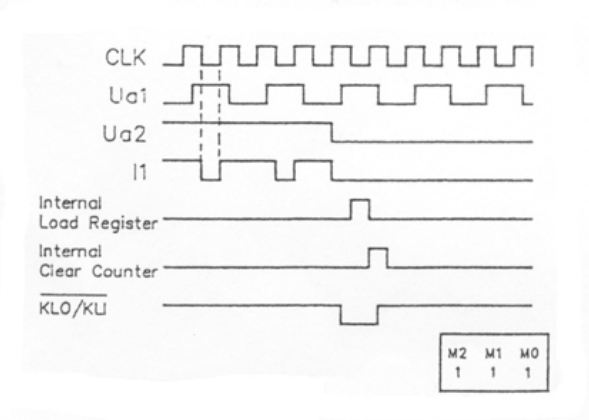


Figure 7 Frequency Measurement

Reset Operation:

A total reset is initiated by pulling the /RESET pin low. This will clear the counters to zero, reset the D flip-flops at the inputs of the quadrature signals (Ua1n and Ua2n), clear the latches that inhibit the load register pulse, and load zero into the output register.

To avoid a spurious count error (+/- 1) after a reset, the Ua1n and Ua2n inputs should be held to the values indicated in ***Table 4*** during and just after the reset pulse.

MODE	Ua1n	Ua2n
0	X	X
1-5	H	H
6-7	L	L

Table 4 Mode Selection

Cascading Devices

The /KLI-KLOn pins of all cascaded PE12316's should be tied together, so that all of the devices load their output registers at the same time. When the 'Master' generates a pulse for the other PE12316s, /KLI-KLOn on the 'Master' works as an output, and /KLI-KLOn on the 'Slaves' work as inputs. The /CARRY output of one device should be tied to the /UP input of the next device in the cascade. Similarly, /BORROW should be connected to /DOWN. For details see ***Figure 14***.

Write Operation

A number may be preloaded into the counter by pulling /CS and /WE low while using /A0 and /A3 to direct the value on the data bus to the selected byte of the counter and /A1 & /A2 to select the required channel. This will cause /READY to go low on the next falling clock edge, and remain low until /CS and /WE go high. See ***Figure 12***.

Read Operation

When in Modes 0 to 5 the contents of the counter can be read at any time by pulling /CS and /RD low. The channel is selected by using /A1 & /A2. Within this channel the most significant byte may be selected by setting /A3 to low, and the least significant byte may be read by setting /A0 and /A3 high. This will cause a load output register pulse to be generated and /KLI-KLOn will go low during the next low clock pulse. /READY will also go low as the clock goes low, and will stay low until /CS and/or /RD go high.

The load output register pulse stores the current value of the counter in a 16-bit latch register and /A0 /A3 direct the selected byte through a multiplexer to the outputs : /CS and /RD also enable the 3-stat outputs – see ***Figure 11***. The output register will be loaded immediately if /KLI-KLOn is pulled low externally, this signal normally comes from a cascaded device.

For Modes 6 & 7 see the earlier description.

Configuration

Special consideration should be paid to the automatic configuration features of the PE12316. The purpose of these features is to allow for the different order of byte reads (high then low or low then high) of different processors when doing a word read across a byte wide bus and also to configure cascaded devices automatically for correct word read sequence – see below.

Byte order Configuration

After a system reset has occurred, the first read operation will store the value of /A0 and /A3 in a latch within the device. From that time until the next system reset the load output register pulse during a read operation will only be generated if /A0 and /A3 are this stored value. This means that the internal load output register pulse is correctly generated for word operations regardless of the byte order of the particular processor. Special care should be taken if reading individual bytes to ensure these operations are always done in a consistent order.

Cascaded configuration

After a system reset the first device and channel to receive a read operation configures itself into 'Master' mode and outputs a pulse on /KLI-KLO. In cascaded operation the /KLI-KLO pins of the cascaded channels are connected together and the input pulse on /KLI-KLO of the cascaded channels configures these to 'Slave' mode. On all subsequent read operations the load output register pulse is only generated by the 'Master' channel (for the appropriate polarity of /A0, as noted above) and this is fed to the 'Slave' devices via the /KLI-KLO connection.
Special care should be taken when cascading devices or channels to always read in the same channel order, as well as the byte order already mentioned.

To freeze all three channels with a single read cycle (in cascaded or non-cascaded mode) the /KLI-KLOn pins of all channels are connected with a pull-up resistor to V_{CC} (see System Application). This ensures that only one channel is operating as the 'Master' and all others are 'Slaves'.

If an external "freeze" of the positioning system is required, an external /KLI-KLO pulse will program all channels as slaves. This is derived by generating an external /KLI-KLO pulse **before** the first read cycle appears after system reset.

Pin Description

Pin Name	Pin Number		I/O	Description
	68 PLCC			
/CS	12		Input	Chip Select. A low enables the device.
/RD	8		Input	Read. When this and /CS are active (low), the data from the output register will be present on the data bus.
D0 D1 D2 D3 D4 D5 D6 D7	14 15 17 18 20 21 23 24		Input/ Output	LSB Data Bus Buffer: 8-Bit Bi-directional Buffer with 3-state outputs connected to the microprocessor system. MSB
/BORROW1 /BORROW2 /BORROW3	58 56 54		Output	Counter underflow signal.
/CARRY1 /CARRY2 /CARRY3	59 57 54		Output	Counter overflow signal.
/KLI-KLO1 /KLI-KLO2 /KLI-KLO3	62 61 60		Input/ Output (OD)	Cascade load input / cascade load output. Open drain (OD) output with internal 75kOhm (nom) pull-up. External pull up required for full speed operation.
/READY	63		Output (OD)	When low signal indicates to the MPU that read or write may be completed. /READY falling edge synchronous with CLK Open Drain output needs external pull-up.
M21 M11 M01 M22 M12 M02 M23 M13 M03	29 28 27 34 32 30 37 36 35		Input Input Input Input Input Input Input Input Input	Mode Select Inputs (see ***Table 1***)
Ua11 Ua21	39 41		Input Input	Measuring input signals channel 1 (Schmitt-Trigger characteristics)

Pin Description

Pin Name	Pin Number		I/O	Description
	68 PLCC			
Ua12 Ua22 Ua13 Ua23	42 43 44 45		Input Input Input Input	Measuring input signals channel 2 (Schmitt Trigger characteristics) Measuring input signals channel 3 (Schmitt Trigger characteristics)
/Ua01 /Ua02 /Ua03	3 2 1		Input Input Input	Zero pulse for each channel. When active (low), the counter in the appropriate channel is cleared. Other logic is not affected. (Schmitt Trigger characteristics)
CLK	68		Input	Clock. Used for internal synchronisation and control timing. (Schmitt Trigger characteristics)
/A0	9		Input	Byte select. A high level selects the least significant byte. A low level selects the most significant byte.
/A1 /A2	10 11		Input Input	Channel select. See ***Table 2***
/A3	6		Input	Selects Bits 16-23 of chosen channel. Internal Pullup. For details see ***Table 3 Memory Map***.
/RESET	5		Input	Device Reset. When active (low), the mode control logic is reset to a known state and the counter is cleared. (Schmitt Trigger characteristics)
/WE	7		Input	Write enable. When /WE and /CS are active (low), the data that is on the bus is loaded into the counter addressed by /A0, /A1, /A2 and /A3.
/DOWN1 /DOWN2 /DOWN3	47 49 51		Input Input Input	Cascade Input for counting down.
/UP1 /UP2 /UP3	46 48 50		Input Input Input	Cascade Input for counting up.
V_{CC}	16,22, 52,66			Power Supply voltage
GND	13,19, 25,53, 64			Ground

Absolute Maximum Ratings over operating free air temperature:

Symbol	Parameter	Value	Units
V_{CC}	DC Supply Voltage	-0.3 to + 7.0	V
V_{IN}	DC Input Voltage	-0.3 to V_{CC} + 0.3	V
I_{IN}	DC Input Current	+/- 10	mA
Storage Temperature (Plastic Package)		-40 to +125	°C

DC Characteristics (referred to GND):

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{OH} All except, /READY and /KLI-KLO	Output High Level	I_{OH} = -20 uA	V_{CC}-0.1			V
V_{OH} D0-D7		I_{OH} = -8 mA, V_{CC} = 5.0V	2.4			V
V_{OH} All except D0-D7, /READY and /KLI-KLO		I_{OH} = -6 mA, V_{CC} = 3.3V	2.4			V
V_{OL}	Output Low Level	I_{OH} = 20 uA			0.1	V
V_{IH}	Input High Level	TTL Schmitt Trigger	2.0 2.4			V
V_{IL}	Input Low Level				0.5	V
I_{CC}	Supply current	20 MHz V_{CC}=Max		25		mA
VT+	Schmitt Trigger positive going threshold	V_{CC} = Min to Max			2.4	V
VT-	Schmitt Trigger negative going threshold	V_{CC} = Min to Max			0.5	V
V_{HYS}	Schmitt Trigger Hysteresis	V_{CC} = Min to Max	0.2			V
I_{OZ}	Tristate Output Leakage Current	V_{CC} = Max or GND	-10		+10	uA
I_{IH}	Input High current	V_{IN} = V_{CC}	-10		+10	uA
	Input with pullup		-200		-10	uA
I_{IL}	Input Low current	V_{IN} = GND	-10		+10	uA

Recommended Operating Conditions:

Symbol	Parameter	Value	Units
V_{CC}	DC Supply Voltage	4.5 to 5.5	V
V_{CC}	DC Supply Voltage (Low Power Application)	3.0 to 3.6	V
T_{AC}	Temperature Range	0 to +70	°C

Timing Requirements over Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Units
Tc1	CLK Cycle Time, duty cycle 50%	50			ns
Tc2	Pulse width low CLK	25			ns
Twrs	Pulse width, /RESET input low	50			ns
fmud	Maximum frequency, /UPn or /DOWNn, Input duty cycle 50%	20	25		MHz
Twud	Pulse width, /UPn or /DOWNn input low	25			ns
Twk	Pulse width, /KLI-KLOn input low	20			ns
Twrd1	Pulse width, /RD input low (Mode = 6 & 7)				ns
Twrd2	Pulse width, /RD input low (Mode = 0 to 5)		Tc1		ns
Tdrd	Time between two read cycles (LSB and MSB)	0			ns
Twwr	Pulse width, /WE input low	25			ns
Tdwr	Time between two read cycles (LSB and MSB)	0			ns
Tsd	Set up time, DATA prior to /WE **rising**	15			ns
Tsus	Set up time, /CS and /RD low before CLK falling edge	15			ns
Tsa	Set up time, /A0, /A1, /A2 prior to /WE and /CS low	10			ns
Tsud	Set up time, /UPn or /DOWNn rising edge before CLK falling edge	20			ns
Tsab	Set up time, Ua1n or Ua2n prior to CLK falling edge.	15			ns
Tsda	Set up time, DATA prior to /WE rising	Tsd			ns
Tsbb	Set up time, Ua2n stable before CLK falling edge	15			ns
Tsac	Set up time, Ua1 or Ua2 rising edge before CLK falling edge.	15			ns
Tsar	Set up time, /A0, /A1, /A2 stable before /CS and /RD low after reset	10			ns
Tsbc	Set up time, Ua1n or Ua2n falling edge	15			ns
Tsr	Set up time, /RESET high prior to CLK falling edge.	0			ns
Tsuc	Set up time, /UPn or /DOWNn rising edge prior to /KLI-KLOn (input) falling edge.	20			ns
Thdw	Hold time DATA after /WE rising	10			ns
Twgp	Pulse width, Ua1n input high (Mode = 6)	Min 2 x Tc1			ns
Twgp	Pulse width, Ua2n input high (Mode = 7)	Min 2 x Tc1			ns
Tdgp	Pulse width, Ua1n input low (Mode = 6)	Min 2 x Tc1			ns

Timing Requirements over Recommended Operating Conditions - continued

Symbol	Parameter	MIN	TYP	MAX	Units
Tdgf	Pulse width, Ua2n input low (Mode = 7)	Min 2 x Tc1			ns
Tha	Address hold time after /WE or /CS high	12			ns
Thab	Ua1n or Ua2n hold time after CLK falling edge	12			ns
Thda	D0-D7 hold time after /A0 change	10			ns
Thac	Ua1n high hold time after CLK falling edge	12			ns
Thbc	Ua2n hold time after CLK falling edge	12			ns
Twrn	Pulse width, /Ua0n input low	5			ns

Switching Characteristics, (V_{CC}= Min, Temperature +70 Degrees)

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
Tdd1	Access time, /RD and CLK to data output valid (Mode = 0 to 5)				65	ns
Tdd2	Access time, /RD to data output valid Mode = 0 to 5 2nd byte Mode = 6-7 both bytes				45	ns
Thdr	Propagation delay /RD, /WE or /CS inactive to /READY	From CS ↑			20	ns
Tdr	Propagation delay CLK ↓ to /READY low				30	ns
Tduc	Propagation delay /UPn or /DOWNn rising edge to /CARRYn or /BORROWn rising edge	From /UPn ↑ to /CARRY ↑			35	ns
Tdcc	Propagation delay from CLK to /CARRYn or /BORROWn rising edge	From /CLK ↑ to /CARRY ↑ or from /CLK ↑ to /BORROW ↑			25	ns
Tdco	Propagation delay CLK falling edge to /KLI-KLOn falling edge				55	ns
Tdcb	Propagation delay CLK rising edge to /CARRYn or /BORROWn rising edge	From /CLK ↑ to /CARRY ↑ or /BORROW ↑			25	ns
Ted	Enable Time /RD and /CS low to D0-D7				65	ns
Twco	/KLI-KLOn low output pulse width			Tc2		ns
Twcb	/CARRYn or /BORROWn low output pulse width			Twud		ns
Twcc	/CARRYn or BORROWn low output pulse width			Tc2		ns
Thdr	Release time, DATA after /RD, /CS		0		45	ns

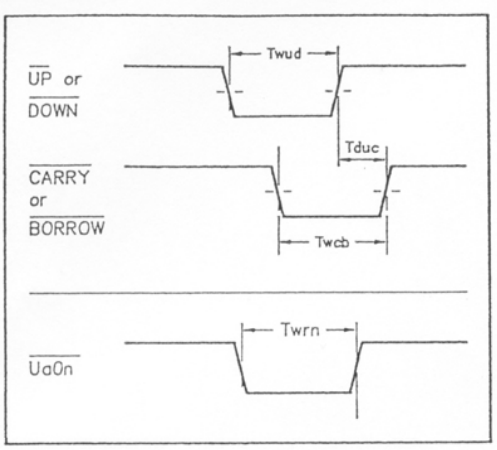


Figure 9 Timing – all modes

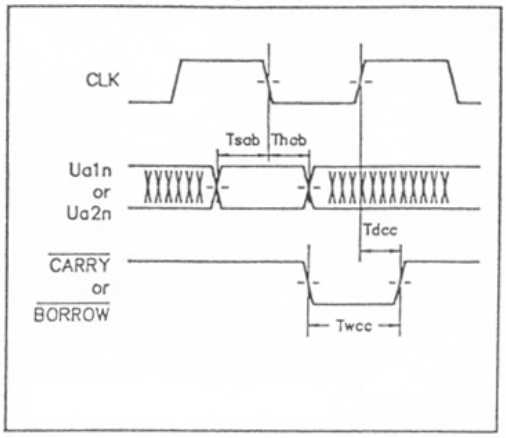


Figure 8 Timing –Mode 1 - 5

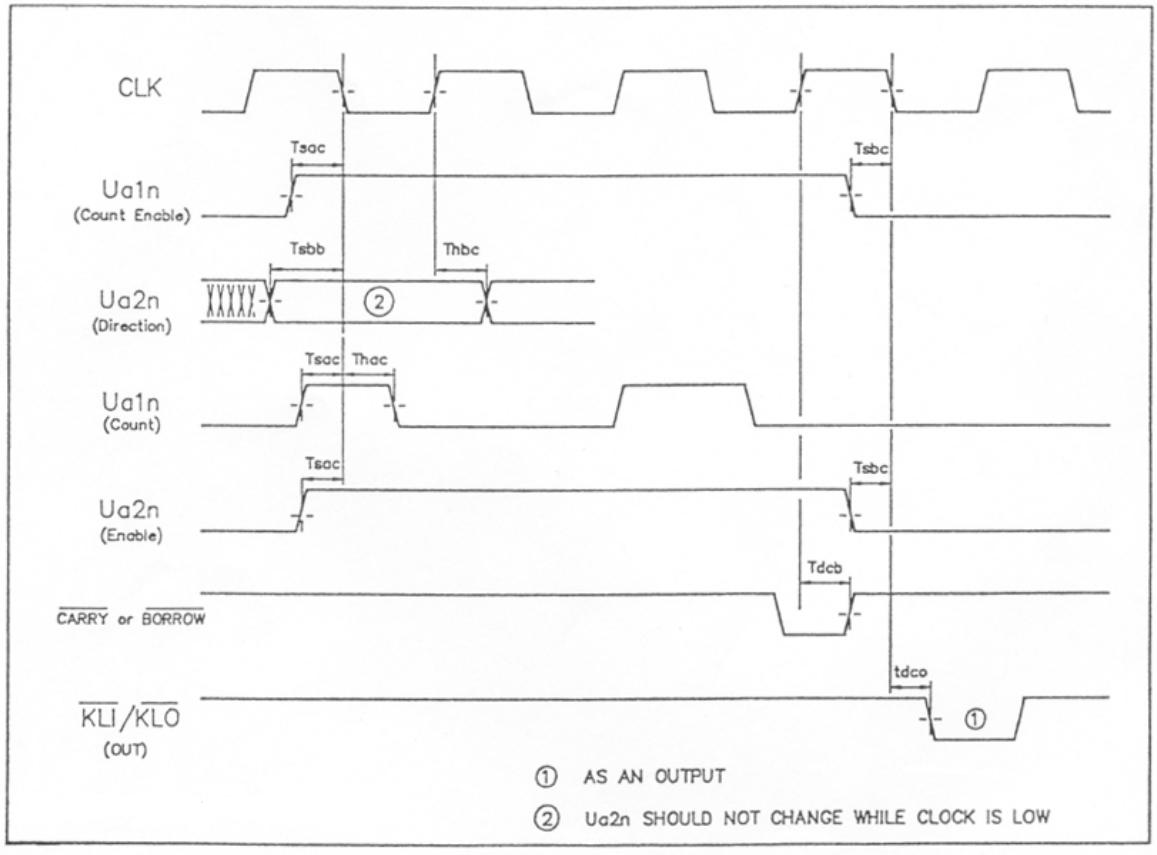


Figure 10 Timing – Mode 6-7

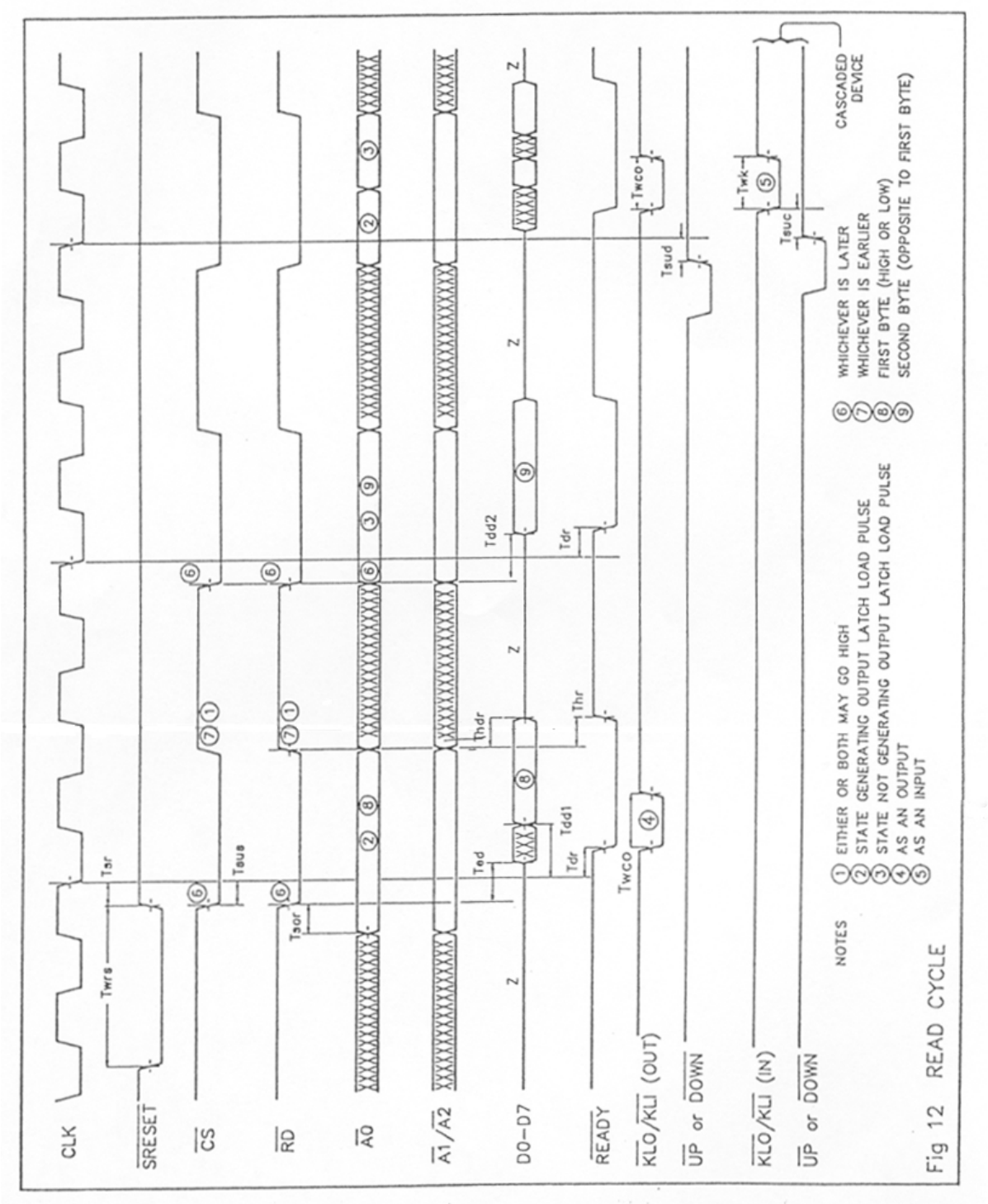


Figure 11 Read Cycle

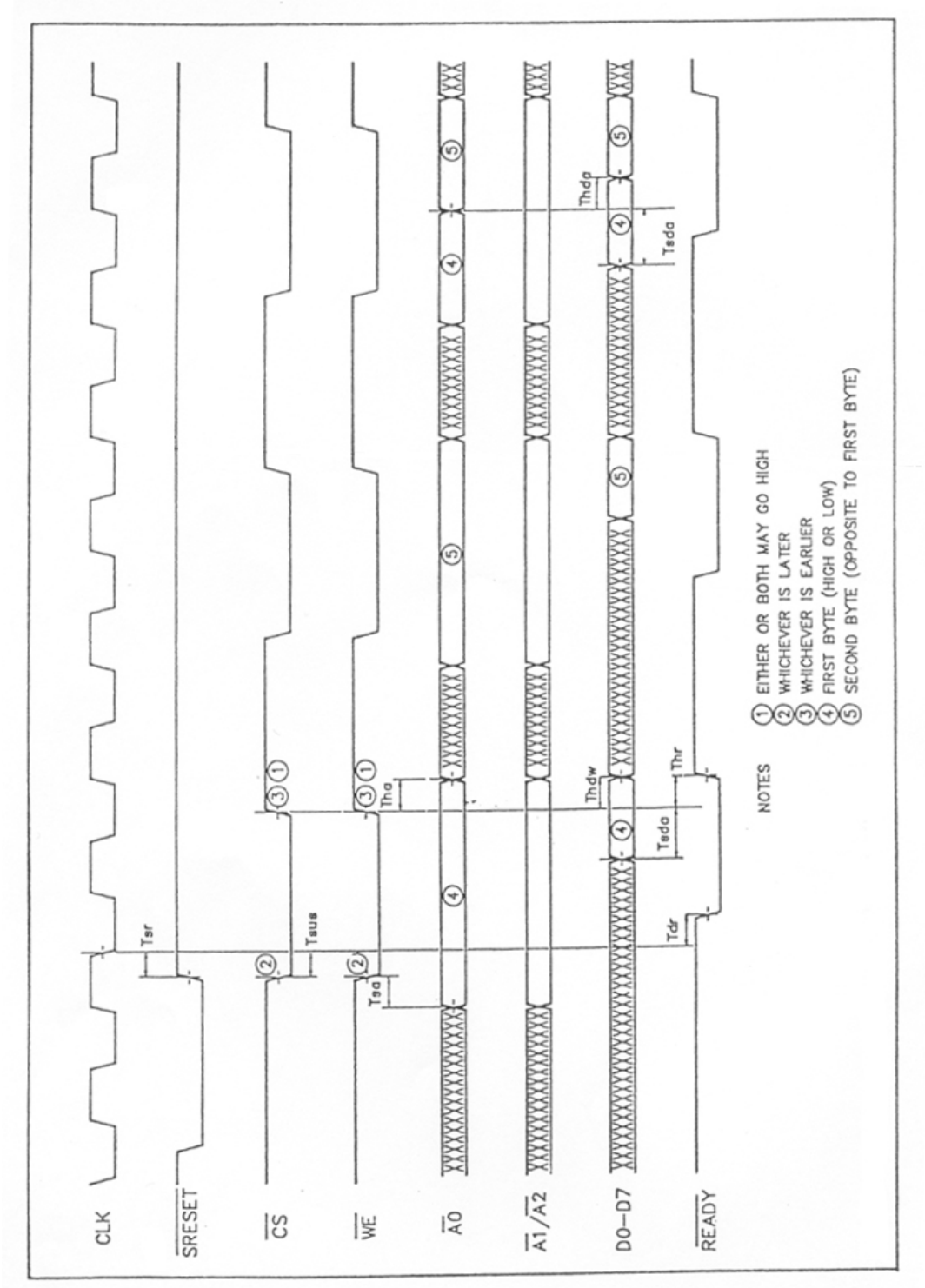


Figure 12 Write Cycle

System Application

Figure 13 shows a three axis microcomputer system using the PE12316. The clock of the microcomputer can be used to drive the PE12316 and addressing is either via memory mapped I/O or external I/O port addresses. The basic timing cycle must be chosen so that it matches that of the PE12316 read and write timing. In Mode 0, all Ua1n's and Ua2n's must be connected to V_{CC}. In all other modes /UPn and /DOWNn are tied to V_{CC}. If a parallel freeze of all three channels is required all /KLI-KLOn's are connected together. One external pull-up (6.8k – 12k) is required in this case. If the UaXn input are not used, they must be tied to V_{CC}. ***Figure 13*** shows the Mode 5 connection for quadruple count inputs of Ua1n and Ua2n.

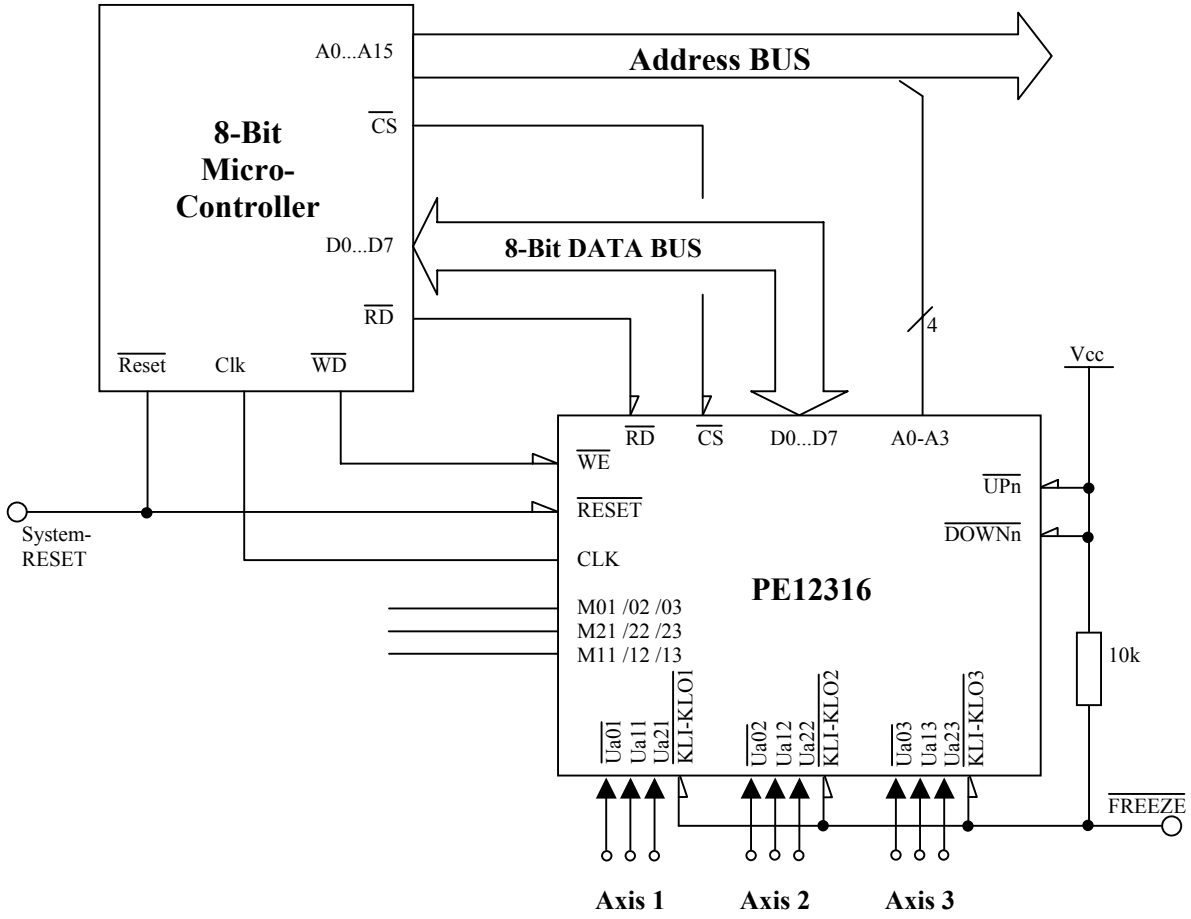


Figure 13 Three Axis Control System using PE12316

Cascading to 32 Bits

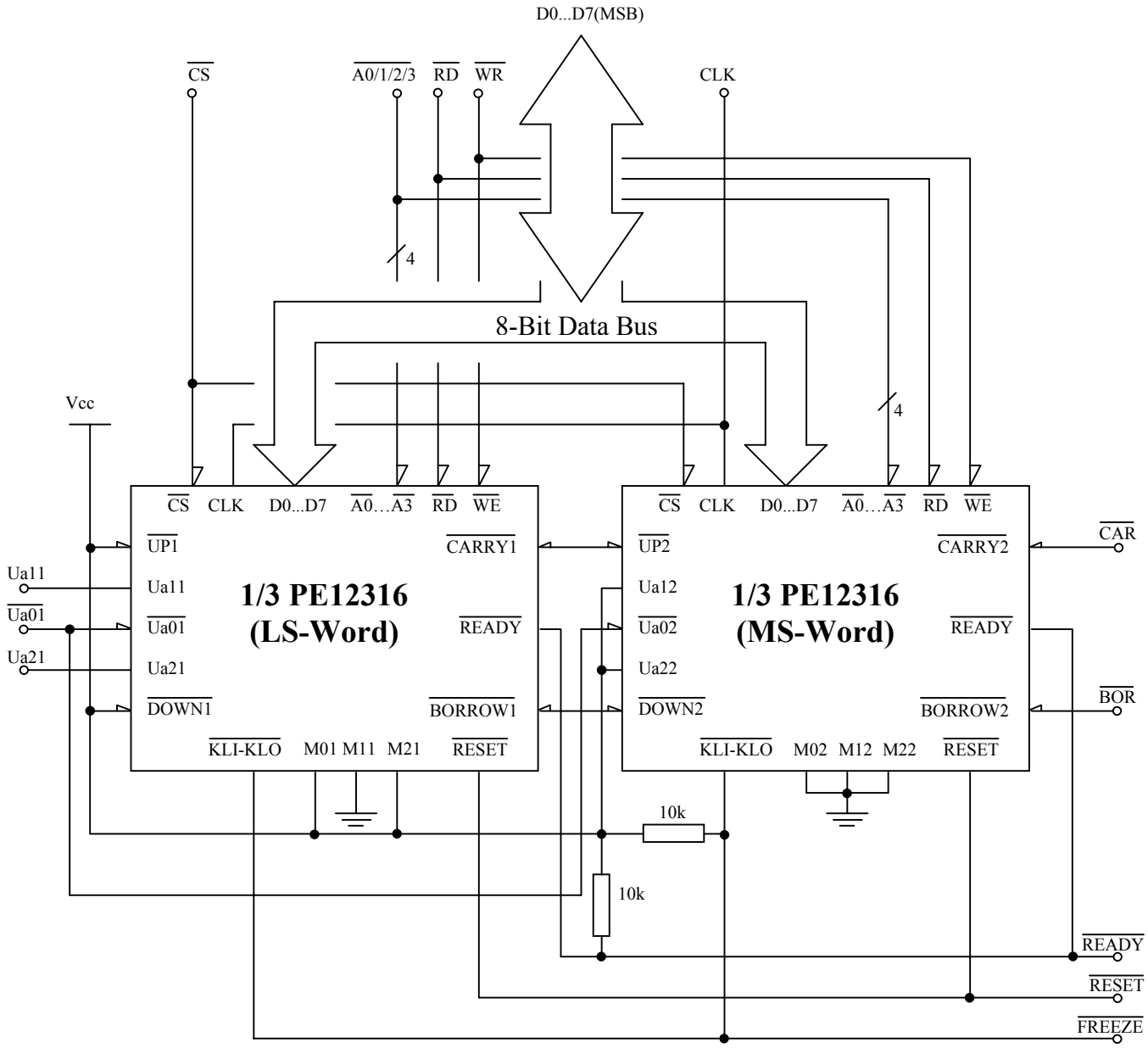


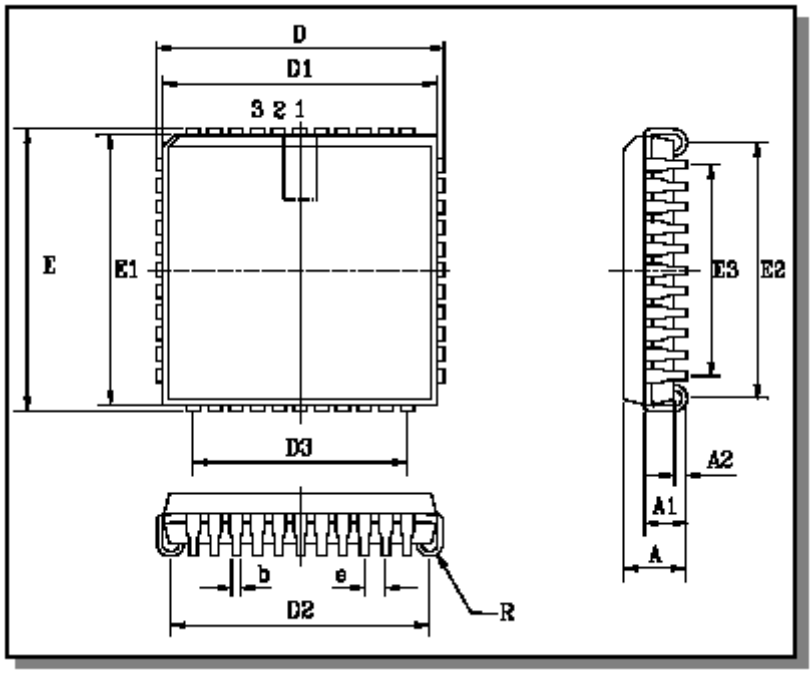
Figure 14 Two Cascaded Channels (One 32-bit channel shown)

In systems requiring a higher resolution, two PE12316's or two channels of the PE12316 can be cascaded to achieve 32 bit accuracy ***Figure 14*** shows the block diagram of this application. It shows the two PE12316 devices with one channel of each cascaded to 32 bit. The LS-word PE12316 is operating in Mode 5 and the MS-word in Mode 0 (count only). The /KLI-KLO signals of each channel are connected together with a pull up of 10k and can be used as an external freeze input. In this case, the first external /KLI-KLO pulse, programming the PE12316 into the SLAVE mode, must occur before the first read cycle, otherwise the device channel receiving the first read cycle will be programmed into the master mode and generate a /KLI-KLO pulse for the second device. /UP1 and /DOWN1 of the first device are tied to Vcc. Both /Ua01's are connected together and can recover the zero pulse from the resolver.

The system reset inputs of each PE12316 device (/RESET) are connected together and must be used to ensure that the system is started from a known state after the power-up. If /READY is used from the PE12316, both are wired-OR and a pull-up of 10k is connected to V_{CC} to generate a proper high level in the non-active state (open drain output).

PLCC68 Package Dimensions

Package Drawing:



Plastic Leaded Chip Carrier (PLCC)												
Package type		D/E	D1/E1	D2/E2	D3/E3	A	A1	A2	e	b	R	
PLCC 68	min	25.02	24.13	22.61	20.32	4.20	2.29	0.51	1.27	0.33	0.64	
	max	25.27	24.33	23.62		5.08	3.30			0.53	1.14	
Dimension: mm, coplanarity < 0.1 mm, original dimension: inch												

Figure 15 PLCC68 Package Dimension

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Application Notes:

24 Bit Access

To provide 24 Bit counting on each channel, /A3 on pin 6 is introduced. However it has to be kept in mind for cascading that /CARRY, /BORROW are derived from bits 0-15 of the counter to ensure compatibility with CF32006. The first channel in the chain can only be 16 bit wide to provide the correct interfacing signals CARRY/BORROW to the following channel. However the last channel in the chain can use the full 24 bit.
/A3 is located on pin 6 which is an "NC" pin on CF32006. This pin was not allowed to have a connection to the PCB board. Therefore no compatibility issue should arise.
As with all other addresslines, /A3 is low active. An internal pullup resistor ensures that /A3 can be left unconnected, if the 24 bit feature is not used. For details see ***Table 3 Memory Map***.

Possible Cascading Combinations:

First channel	Second channel	Third channel	Resulting bitwidth
16 Bit	16 Bit	none	32 Bit
16 Bit	24 Bit	none	40 Bit
16 Bit	16 Bit	16 Bit	48 Bit
16 Bit	16 Bit	24 Bit	56 Bit

Table 5 Cascading bitwidths

Read Cycle:

The Readcycle is intended and designed synchronous to the clock. Special care has to be taken for the parameter T_{sus} (the setup time of the falling edge of /RD before the falling CLK edge). If T_{sus} is not within spec, there is the possibility that the output register is not updated and the same value will be read twice. Therefore the microprocessor system collecting the data and PE12316 should either have the same clock or the /RD on the PE12316 has to be synchronized into the PE12316 clock domain via an ACT74 Type Flipflop.

Electrical Design Recommendations:

It is recommended that the PE12316 is used without a socket and with at least 4 decoupling capacitors (100 nF) connected to VCC and GND close to the package.

Figures

Tables

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