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NTE906
Integrated Circuit
Dual, High Frequency, Differential Amplifier

Description:

The NTE906 is an integrated circuit in a 12–Lead TO5 type package consisting of two independent differential amplifiers with associated constant–current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general–purpose devices which exhibit low 1/f noise and a value of f_T in excess of 1GHz. These features make the NTE906 useful from DC to 500MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the NTE906 provides close electrical and thermal matching of the amplifiers. This feature makes this device particularly useful in dual–channel applications where matched performance of the two channels is required.

Features:

- Power Gain: 23dB (Typ) @ 200MHz
- Noise Figure: 4.6dB (Typ) @ 200MHz
- Two Different Amplifiers on a Common Substrate
- Independently Accessible Input and Outputs

Absolute Maximum Ratings: (T_A = +25°C unless otherwise specified)

Power Dissipation, P_D
- Any One Transistor 300mW
- Total Package 600mW
- Derate Above +55°C . . . . . 5mW/°C

Operating Temperature Range, T_{opr} . . . . . –55° to +125°C

Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

The following ratings apply for each transistor:

Collector–Emitter Voltage, V_{CEO} 15V

Collector–Base Voltage, V_{CBO} 20V

Collector–Substrate Voltage (Note 1), V_{CIO} 20V

Emitter–Base Voltage, V_{EBO} 5V

Collector Current, I_C 50mA

Note 1. The collector of each transistor is isolated from the substrate by an integral diode. The substrate (Pin9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Electrical Characteristics: (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Static Characteristics (For Each Differential Amplifier)							
Input Offset Voltage	V_{IO}			–	0.25	–	mV
Input Offset Current	I_{IO}	$I_3 = I_9$ = 2mA		–	0.3	–	μA
Input Bias Current	I_{IB}			–	13.5	33	μA
Temperature Coefficient Magnitude of Input–Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$			–	1.1	–	μV/°C
(For Each Transistor)							
DC Forward Base–Emitter Voltage	V_{BE}	V_{CE} = 6V, I_C = 1mA		–	774	–	mV
Temperature Coefficient of Base–Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 6V, I_C = 1mA		–	–0.9	–	mV/°C
Collector Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0		–	0.0013	100	nA
Collector–Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	–	V
Collector–Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10μA, I_B = 0, I_E = 0		20	60	–	V
Emitter–Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0		5	7	–	V
Dynamic Characteristics							
1/f Noise Figure (For Single Transistor)	NF	f = 100kHz, R_S = 500Ω, I_C = 1mA		–	1.5	–	dB
Gain–Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 6V, I_C = 5mA		–	1.38	–	GHz
Collector–Base Capacitance	C_{CB}	I_C = 0, V_{CB} = 5V	Note 2	–	0.28	–	pF
			Note 3	–	0.28	–	pF
Collector–Substrate Capacitance	C_{CI}	I_C = 0, V_{CI} = 5V		–	1.65	–	pF
(For Each Differential Amplifier)							
Common–Mode Rejection Ratio	CMR	$I_3 = I_9$ = 2mA		–	100	–	dB
AGC Range, One Stage	AGC	Bias Voltage = –6V		–	75	–	dB
Voltage Gain, Single–Ended Output	A	Bias Voltage = –4.2V, f = 10MHz		–	22	–	dB
Insertion Power Gain	G_P	f = 200MHz, V_{CC} = 12V, For Cascode Configuration $I_3 = I_9$ = 2mA For Diff. Amplifier Configuration $I_3 = I_9$ = 4mA (each Collector $I_C \simeq$ 2mA	Cascode	–	23	–	dB
Noise Figure	NF		Cascode	–	4.6	–	dB
Input Admittance	Y_{11}		Cascode	–	1.5+j2.45	–	mmho
			Diff. Amp	–	0.878+j1.3	–	mmho
Reverse Transfer Admittance	Y_{12}		Cascode	–	0–j0.008	–	mmho
			Diff. Amp	–	0–j0.013	–	mmho
Forward Transfer Admittance	Y_{21}		Cascode	–	17.9–j30.7	–	mmho
			Diff. Amp	–	–10.5+j13	–	mmho
Output Admittance	Y_{22}		Cascode	–	–0.503–j15	–	mmho
			Diff. Amp	–	0.071+j0.62	–	mmho

Note 2. Pins 1 & 12 or Pins 6 & 7.

Note 3. Pins 10 & 11 or Pins 4 & 5.

Pin Connection Diagram
(Top View)