# SPDT SWITCH GaAs MMIC

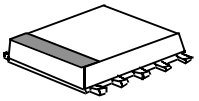
## ■GENERAL DESCRIPTION

NJG1516KC1 is a GaAs SPDT switch IC suited for antenna switch of cellular phone handset.

This switch features low loss, high isolation at high power, and exhibits wide operating frequency range from 50MHz to 3GHz at low voltage of 2.7V.

The ultra small & ultra thin FLP10-C1 package is applied.

## ■PACKAGE OUTLINE

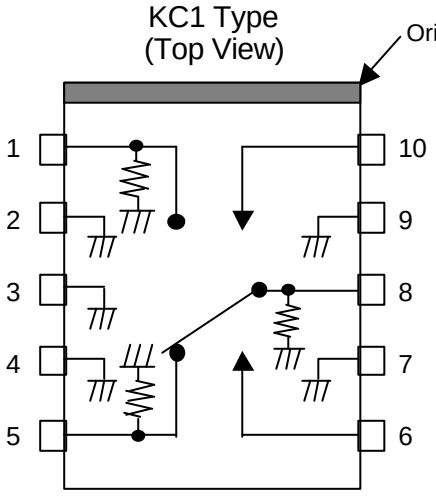


NJG1516KC1

## ■FEATURES

| | |
|---|---|
| ●Single low voltage control | +2.7V min. |
| ●Handling power | 36dBm typ.@f=2GHz, $V_{CTL}$=3.0V |
| ●Low insertion loss | 0.4dB typ. @f=1GHz, $P_{IN}$=31dBm, $V_{CTL}$=3V |
| | 0.4dB typ. @f=1GHz, $P_{IN}$=34.5dBm, $V_{CTL}$=3.5V |
| | 0.7dB typ. @f=2GHz, $P_{IN}$=31.5dBm, $V_{CTL}$=3V |
| ●High isolation | 27dB typ.@f=1GHz, $P_{IN}$=34.5dBm, $V_{CTL}$=3.0V |
| | 25dB typ.@f=2GHz, $P_{IN}$=31.5dBm, $V_{CTL}$=3.0V |
| ●Low current consumption | 38uA typ.@f=2GHz, $P_{IN}$=34.5dBm, $V_{CTL}$=3.0V |
| ●Very small package | FLP10-C1 (Package size: 3.0x2.8x0.75mm) |

## ■PIN CONFIGURATION




Pin Connection
1.P1
2.GND
3.GND
4.GND
5.P2
6.VCTL2
7.GND
8.PC
9.GND
10.VCTL1

## ■TRUTH TABLE

"H"=$V_{CTL\ (H)}$, "L"=$V_{CTL\ (L)}$

| $V_{CTL1}$ | H | L |
|---|---|---|
| $V_{CTL2}$ | L | H |
| PC - P1 | ON | OFF |
| PC - P2 | OFF | ON |

## ■ABSOLUTE MAXIMUM RATINGS

($T_a$=25°C)

| PARAMETER | SYMBOL | CONDITIONS | RATINGS | UNITS |
|---|---|---|---|---|
| Input Power | $P_{IN}$ | $V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=3.0V | 38 | dBm |
| Control Voltage | $V_{CTL}$ | $V_{CTL\ (H)}$-$V_{CTL\ (L)}$ | 12 | V |
| Power Dissipation | $P_D$ | | 500 | mW |
| Operating Temp. | $T_{opr}$ | | -40~+85 | °C |
| Storage Temp. | $T_{stg}$ | | -55~+125 | °C |

## ■ELECTRICAL CHARACTERISTICS

($V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=3V, $Z_S$=$Z_l$=50Ω, $T_a$=25°C)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Operating Voltage (LOW) | $V_{CTL(L)}$ | | -0.2 | 0 | 0.2 | V |
| Operating Voltage (HIGH) | $V_{CTL(H)}$ | f=1GHz, $P_{IN}$=34.5dBm | 2.7 | 3.0 | 9.0 | V |
| Control Current | $I_{CTL}$ | f=1GHz, $P_{IN}$=34.5dBm | - | 38 | 55 | uA |
| Insertion Loss 1 | LOSS1 | f=1GHz, $P_{IN}$=31dBm | - | 0.4 | 0.5 | dB |
| Insertion Loss 2 | LOSS2 | f=1GHz, $P_{IN}$=34.5dBm<br>$V_{CTL(H)}$=3.5V, $V_{CTL(L)}$=0V | - | 0.4 | 0.5 | dB |
| Insertion Loss 3 | LOSS3 | f=1GHz, $P_{IN}$=34.5dBm | - | 0.5 | 0.6 | dB |
| Insertion Loss 4 | LOSS4 | f=2GHz, $P_{IN}$=31.5dBm | - | 0.7 | 0.8 | dB |
| Isolation 1 (PC-P1, PC-P2) | ISL1 | f=1GHz, $P_{IN}$=34.5dBm | 26 | 27 | - | dB |
| Isolation 2 (PC-P1, PC-P2) | ISL2 | f=2GHz, $P_{IN}$=31.5dBm | 22 | 25 | - | dB |
| Maximum Input Power 1 *1 | $P_{IN}$1 | $V_{CTL(H)}$=2.7V, f=2GHz | - | - | 33.5 | dBm |
| Maximum Input Power 2 *1 | $P_{IN}$2 | $V_{CTL(H)}$=3V, f=2GHz | - | - | 34 | dBm |
| Maximum Input Power 3 *1 | $P_{IN}$3 | $V_{CTL(H)}$=4V, f=2GHz | - | - | 37 | dBm |
| Maximum Input Power 4 *1 | $P_{IN}$4 | $V_{CTL(H)}$=6V, f=2GHz | - | - | 38 | dBm |
| Maximum Input Power 5 *1 | $P_{IN}$5 | $V_{CTL(H)}$=9V, f=2GHz | - | - | 34.5 | dBm |
| Pout at 0.2dB Compression point | $P_{-0.2dB}$1 | f=2GHz | 34.5 | 36 | - | dBm |
| VSWR 1 (PC, P1, P2) | VSWR | f=0.05~2.5GHz, ON State | - | 1.45 | 1.55 | |
| Switching Time | $T_{SW}$ | f=0.05~2.5GHz | - | 70 | - | ns |

*1: Maximum Input Power: This value is defined as maximum input power of linear operating region or damage free operating region.

■**ELECTRICAL CHARACTERISTICS** (Cellular Band)

($V_{CTL(L)}$=0V, $V_{CTL(H)}$=2.7V, $Z_s$=$Z_l$=50Ω, $T_a$=25°C)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Frequency range | $f_{in}$ | | 800 | - | 1000 | MHz |
| Control voltage (HIGH) | $V_{CTL(H)}$ | $P_{IN}$=25dBm | 2.7 | - | 9 | V |
| Insertion Loss 5 | LOSS5 | $P_{IN}$=25dBm | - | 0.4 | 0.5 | dB |
| Isolation 3 (PC-P1, PC-P2) | ISL3 | $P_{IN}$=25dBm | 26 | 27 | - | dB |
| Pout at 0.2dB Compression point 2 | $P_{-0.2dB}$(2) | | 33.5 | 35 | - | dBm |
| Input 3rd Order Intercept Point 1 | IIP3(1) | f=900+901MHz, $P_{IN}$=25dBm, $V_{CTL(H)}$=3V, $V_{CTL(L)}$=0V *2 | - | 62 | - | dBm |
| Input 3rd Order Intercept Point 2 | IIP3(2) | f=900+901MHz, $P_{IN}$=25dBm $V_{CTL(H)}$=2.7V, $V_{CTL(L)}$=0V *2 | - | 60 | - | dBm |
| Second Harmonics | 2fo | f=900MHz, $P_{IN}$=25dBm 2nd Harmonics of Input Signal = -83dBc | | -80 | - | dBc |
| Third Harmonics | 3fo | f=900MHz, $P_{IN}$=25dBm 3rd Harmonics of Input Signal =-100dBc | - | -70 | - | dBc |
| VSWR 2 (PC, P1, P2) | VSWR2 | ON State | - | 1.15 | 1.25 | |

*2: The input IP3 is defined as following equation.

IIP3 = (3 x Pout – IM3) / 2 + LOSS

## ■TERMINAL INFORMATION

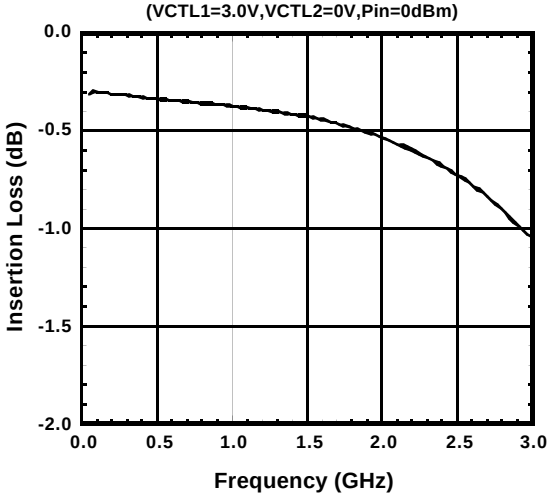
| No. | SYMBOL | EXPLANATION |
|---|---|---|
| 1 | P1 | RF port. This port is connected with PC port by controlling 6th pin ($V_{CTL(H)}$) to 2.7~9.0V and 4th pin ($V_{CTL(L)}$) to -0.2~+0.2V. An external capacitor is required to block the DC bias voltage of internal circuit. (50~100MHz: 0.01µF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF) |
| 2, 3, 4, 7, 9 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |
| 5 | P2 | RF port. This port is connected with PC port by controlling 4th pin ($V_{CTL(H)}$) to 2.7~9.0V and 6th pin ($V_{CTL(L)}$) to -0.2~+0.2V. An external capacitor is required to block the DC bias voltage of internal circuit. (50~100MHz: 0.01µF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF) |
| 6 | VCTL2 | Control port 2. The voltage of this port controls PC to P2 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.7~5.5V) or low-state (-0.2~+0.2V). The voltage of 6th pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching speed delay from 10pF~1000pF range. |
| 8 | PC | Common RF port. In order to block the DC bias voltage of internal circuit, an external capacitor is required. (50~100MHz: 0.01uF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF) |
| 10 | VCTL1 | Control port 1. The voltage of this port controls PC to P1 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.7–5.5V) or low-state (-0.2~+0.2V). The voltage of 4th pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching speed delay from 10pF~1000pF range. |

## ■ELECTRICAL CHARACTERISTICS

(f=50MHz~3GHz, with application circuit, losses of external circuit are excluded)

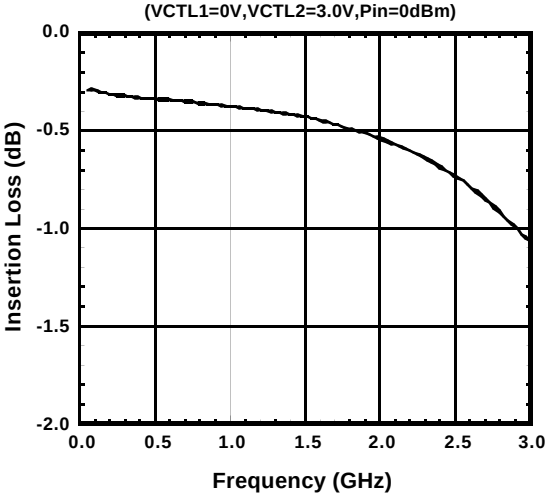
**PC-P1 Insertion Loss vs. Frequency**

(VCTL1=3.0V,VCTL2=0V,Pin=0dBm)



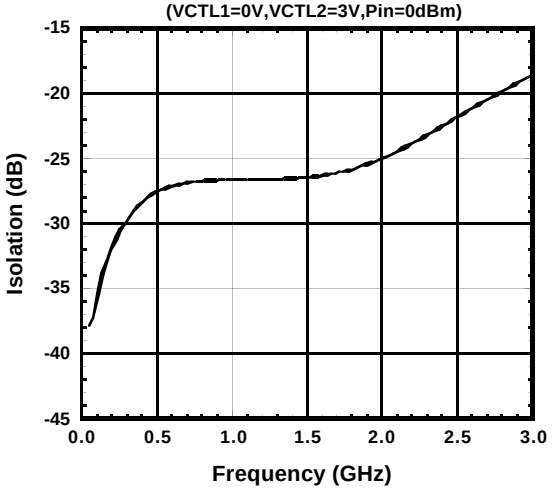

**PC-P2 Insertion Loss vs. Frequency**

(VCTL1=0V,VCTL2=3.0V,Pin=0dBm)



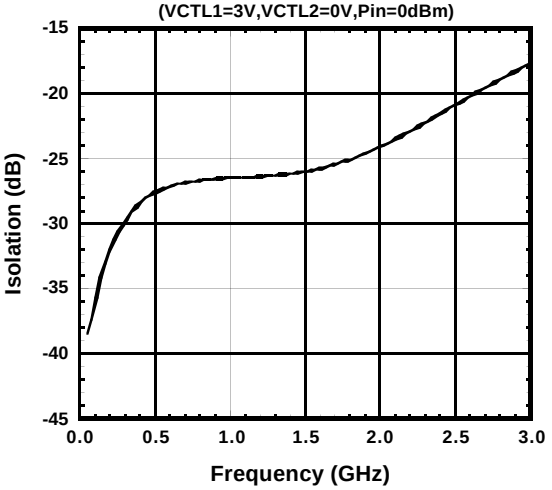

**PC-P1 Isoration vs. Frequency**

(VCTL1=0V,VCTL2=3V,Pin=0dBm)



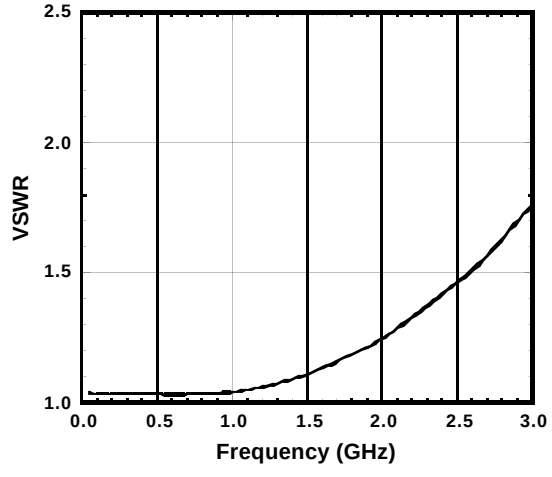

**PC-P2 Isoration vs. Frequency**

(VCTL1=3V,VCTL2=0V,Pin=0dBm)



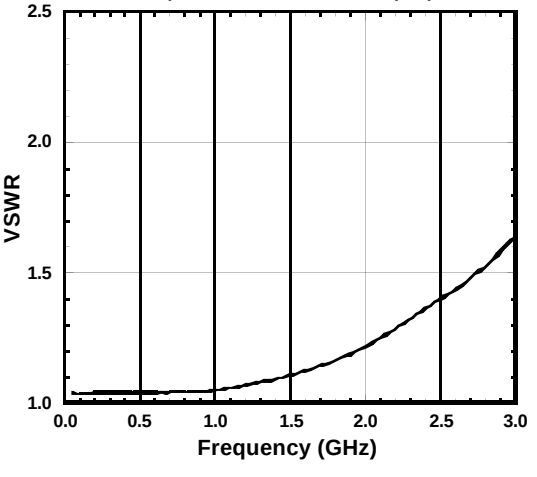

**PC-P1 VSWR vs. Frequency**

(VCTL1=3V,VCTL2=0V,PC port)




**PC-P1 VSWR vs. Frequency**

(VCTL1=3V, VCTL2=0V, P1 port)

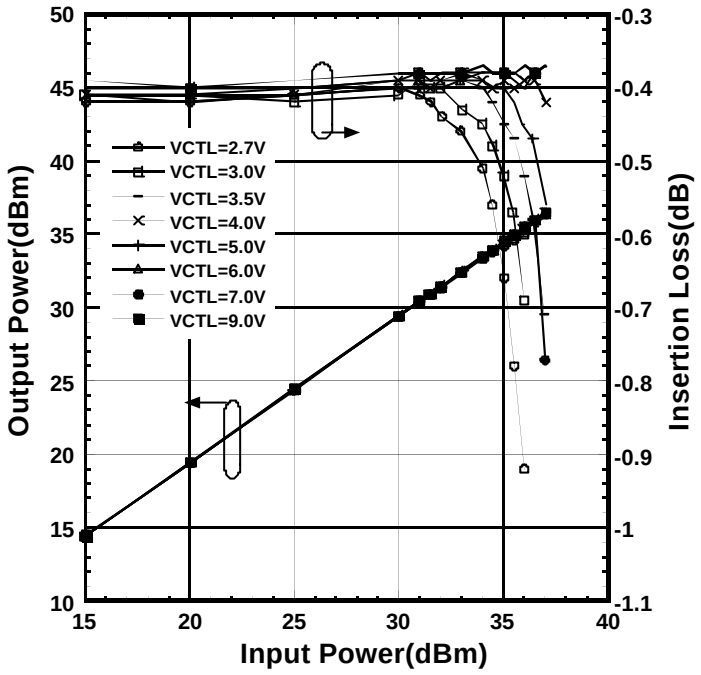


## ■ELECTRICAL CHARACTERISTICS

(f=1GHz, with application circuit (Parts list 3), losses of PCB, DC blocking capacitor are excluded)

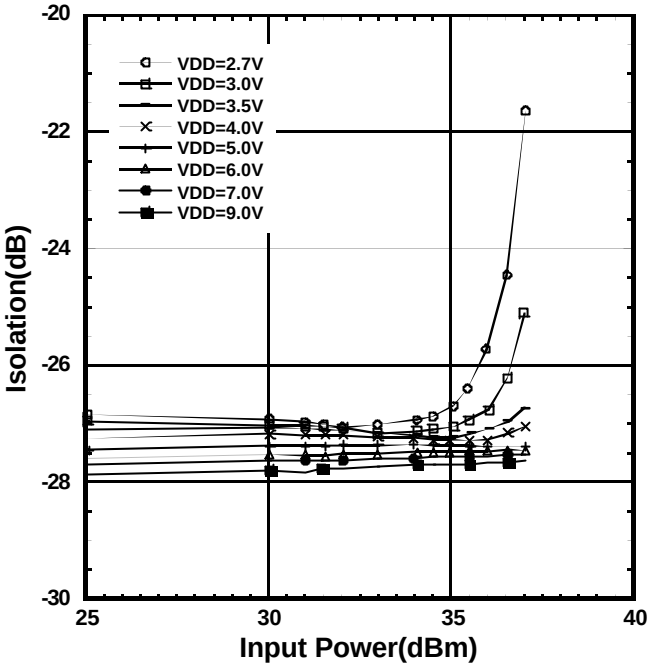
**Output Power,Insertion Loss vs. Input power**

**(PC-P1,f=1GHz)**



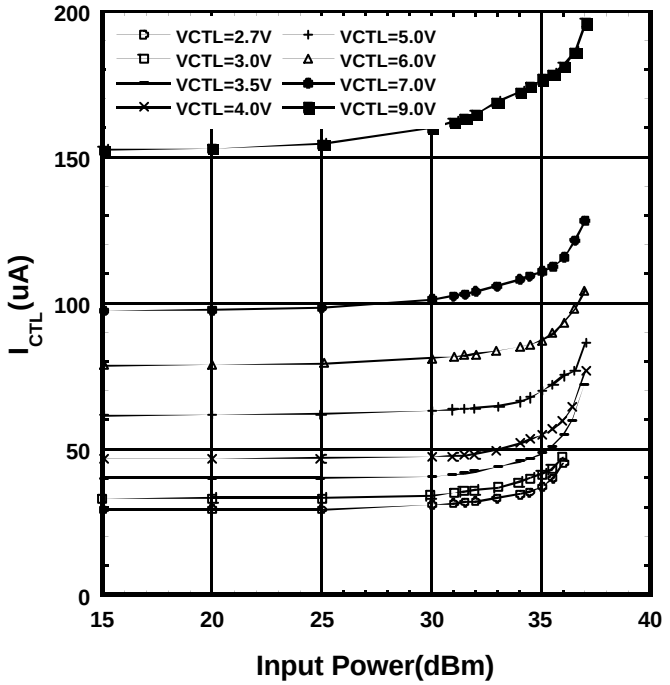

**PC-P1 Isolation vs. Input Power**

**(PC-P1,f=1GHz)**




**$I_{CTL}$ vs. Input Power**

**(PC-P1,f=1GHz)**

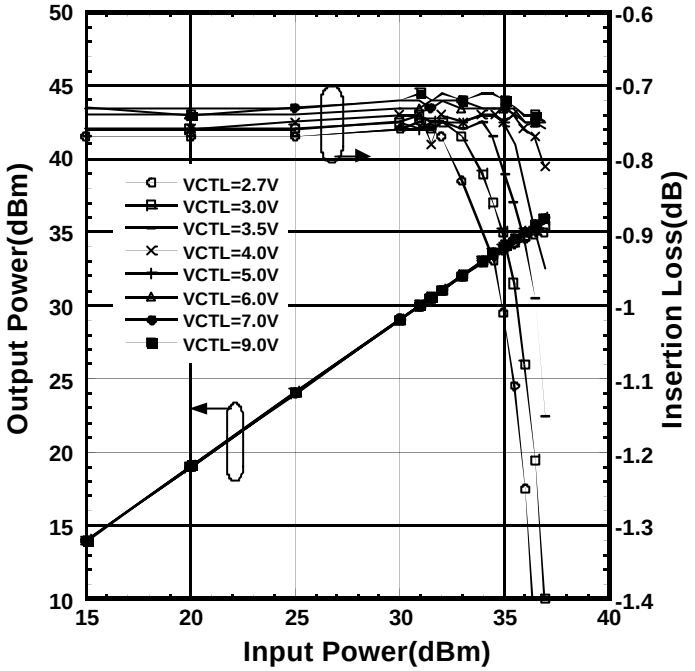


## ■ ELECTRICAL CHARACTERISTICS

(f=2GHz, with application circuit (Parts list 3), losses of PCB, connector and DC blocking capacitor are excluded)

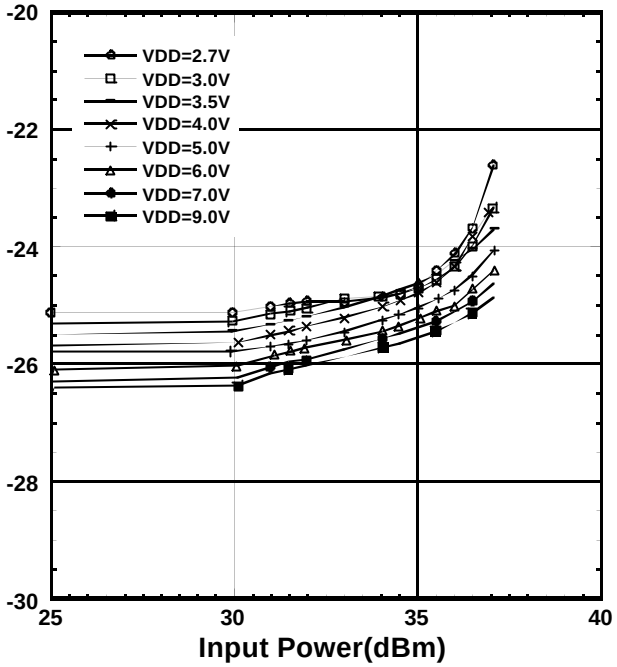
**Output Power,Insertion Loss vs. Input power**

**(PC-P1,f=2GHz)**



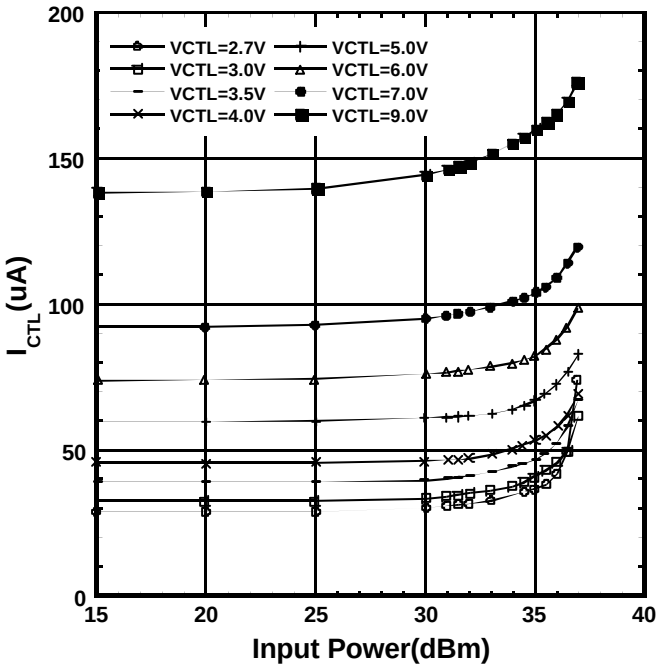

**PC-P1 Isoration vs. Input Power**

**(PC-P1,f=2GHz)**



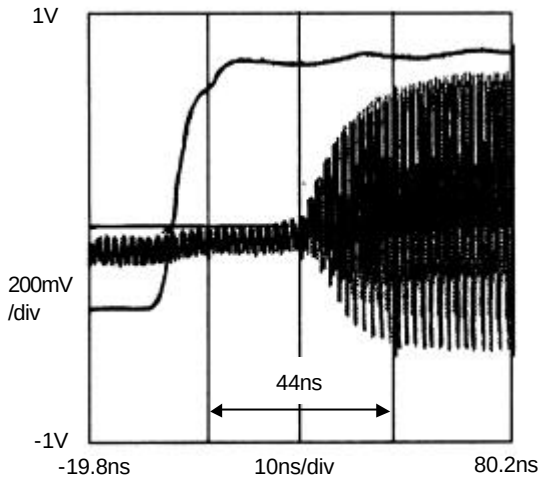

**$I_{CTL}$ vs. Input Power**

**(PC-P1,f=2GHz)**

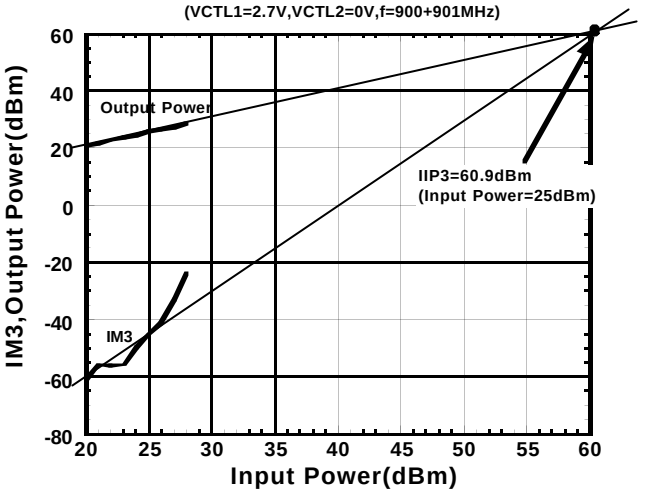


■**ELECTRICAL CHARACTERISTICS** (with application circuit, Parts list 3)

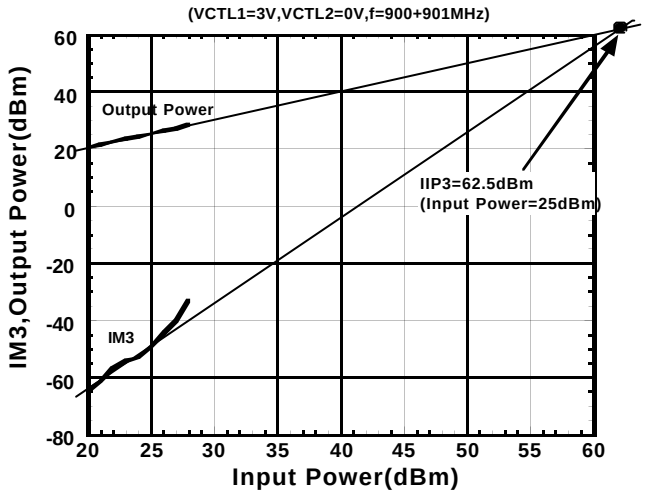
Switching speed
($V_{CTL1}$=3.0V, $V_{CTL2}$=0V)



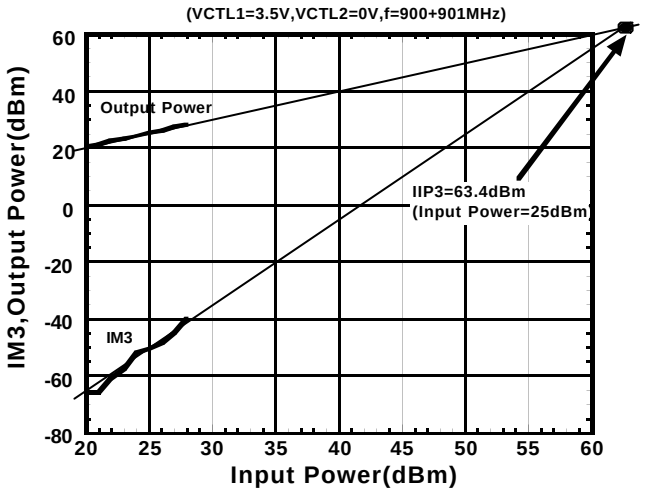

**Output Power,IM3 vs. Input Power**



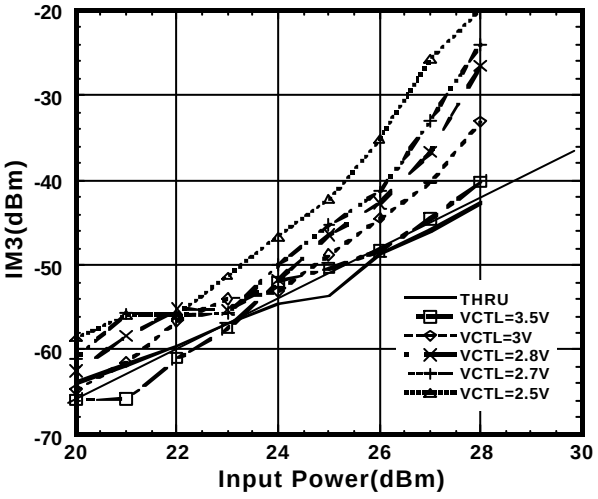

**Output Power,IM3 vs. Input Power**



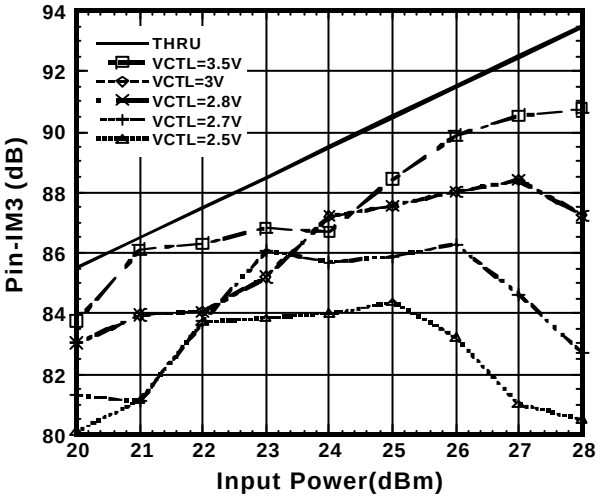

**Output Power,IM3 vs. Input Power**




**IM3 vs. Input Power**



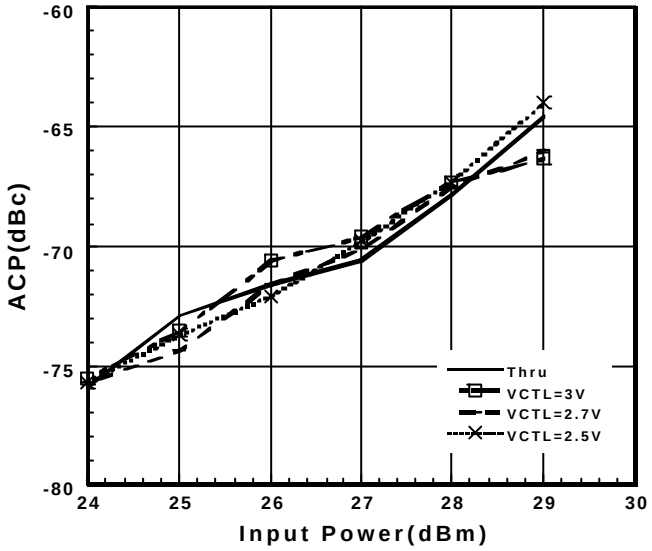

**Pin-IM3 vs. Input Power**



■**ELECTRICAL CHARACTERISTICS** (with application circuit, Parts list 3)

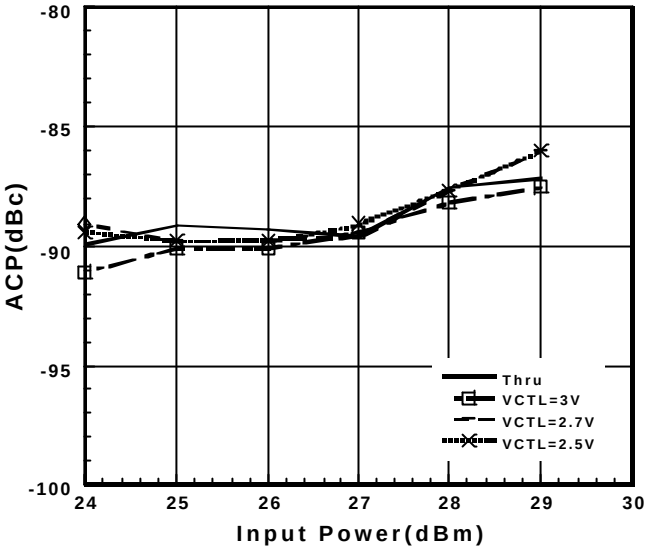
**ACP vs. Input Power**

**(f=1GHz,offset=0.9MHz)**



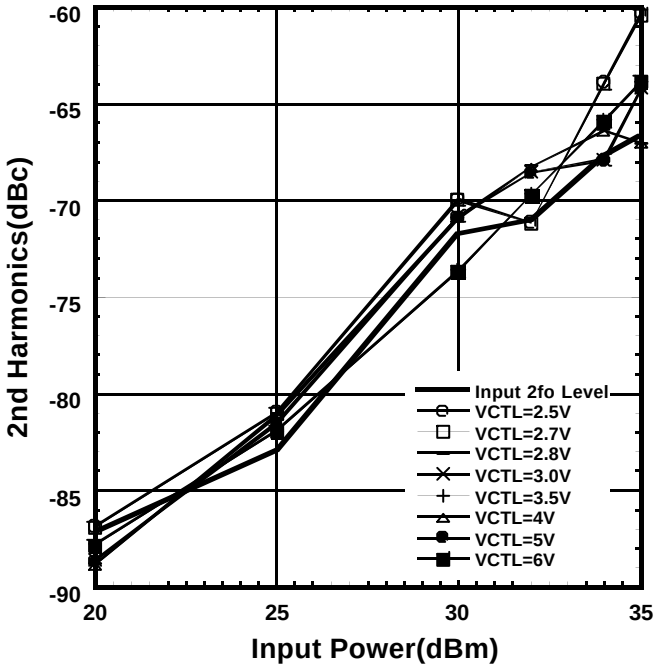

**ACP vs. Input Power**

**(f=1GHz,offset=1.98MHz)**



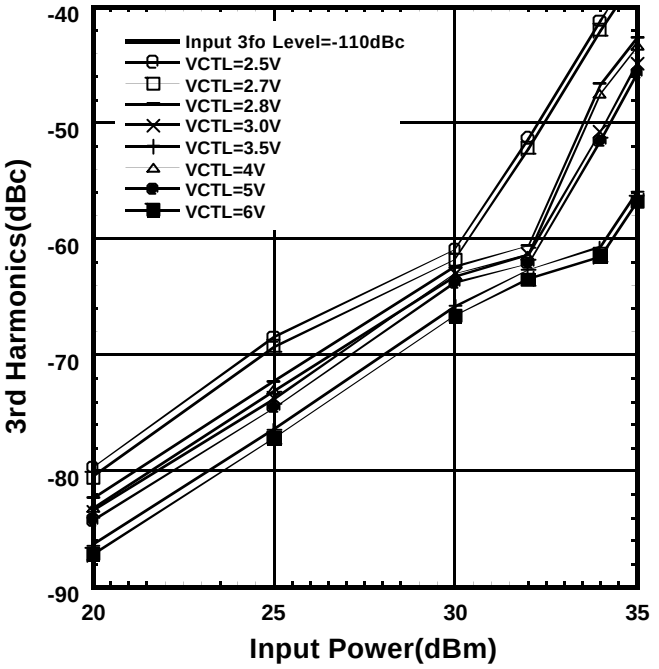

**2nd Harmonics vs. Input Power**

**(f=900MHz)**




**3rd Harmonics vs. Input Power**

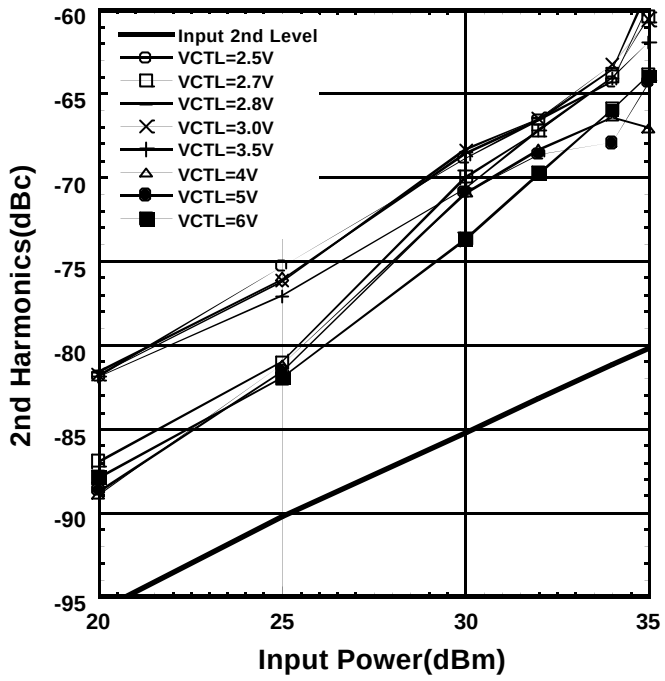
**(f=900MHz)**



■**ELECTRICAL CHARACTERISTICS** (with application circuit, Parts list 3)

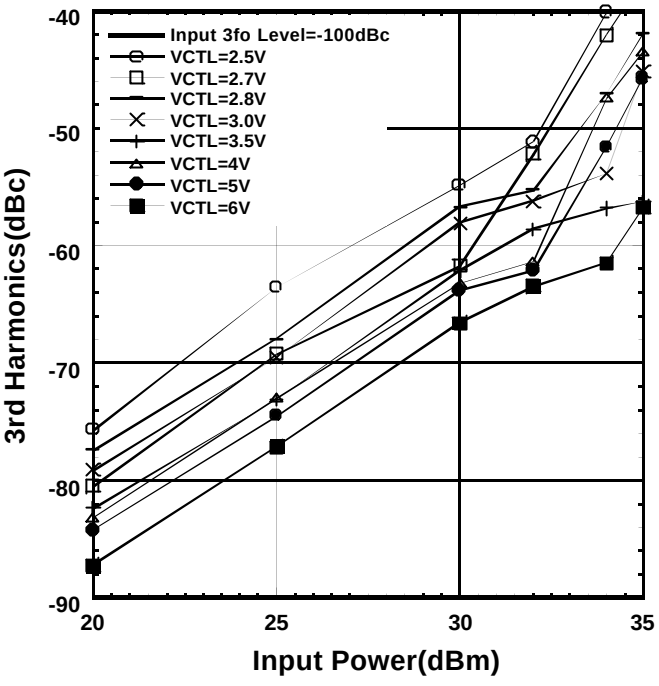
**2nd Harmonics vs. Input Power**

**(f=1800MHz)**



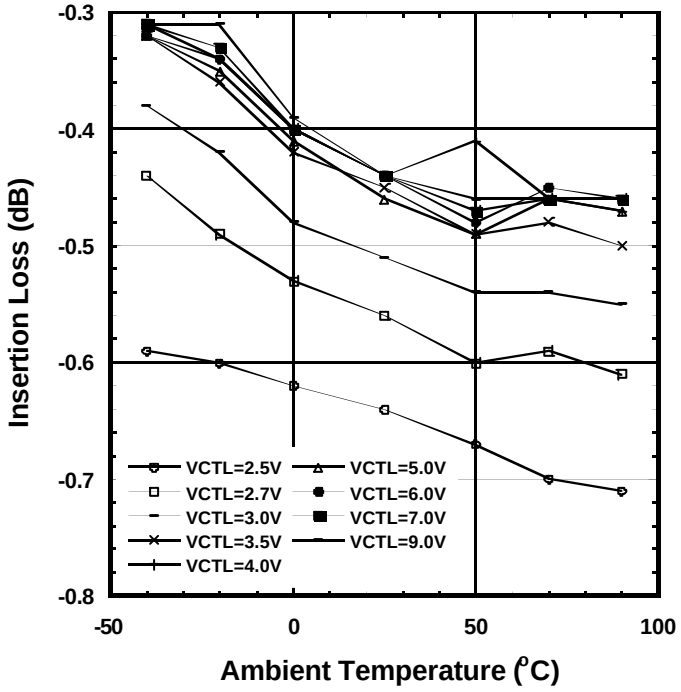

**3rd Harmonics vs. Input Power**

**(f=1800MHz)**



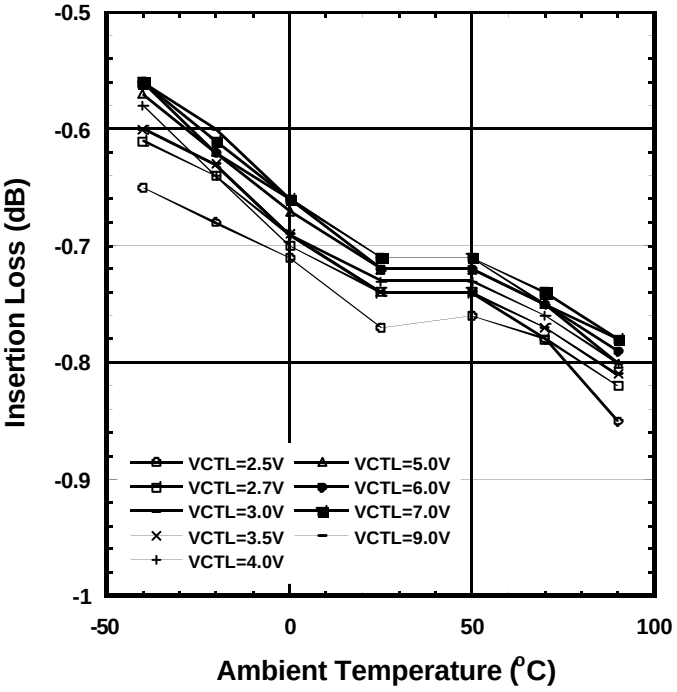

**Insertion Loss vs. Ambient Temperature**

**(PC-P1,f=1GHz,Input Power=34.5dBm)**




**Insertion Loss vs. Ambient Temperature**

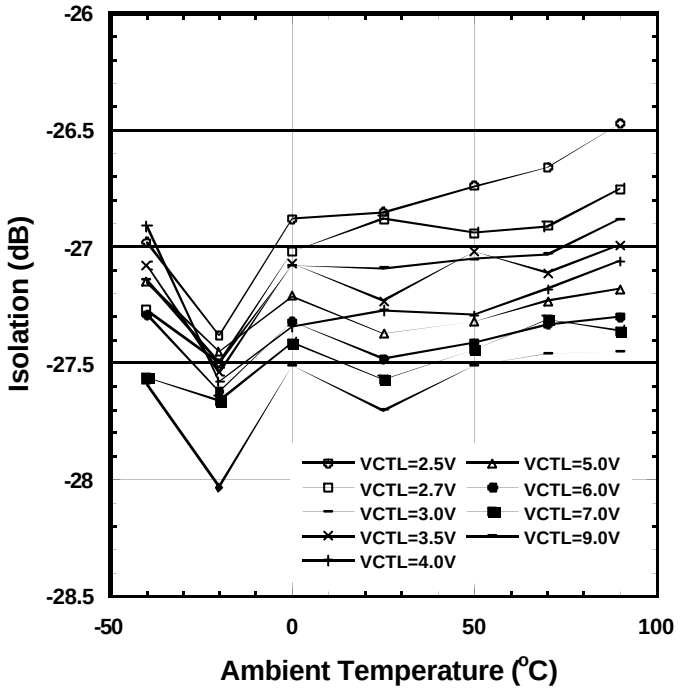
**(PC-P1,f=2GHz,Input Power=31.5dBm)**



■**ELECTRICAL CHARACTERISTICS** (with application circuit, Parts list 3)

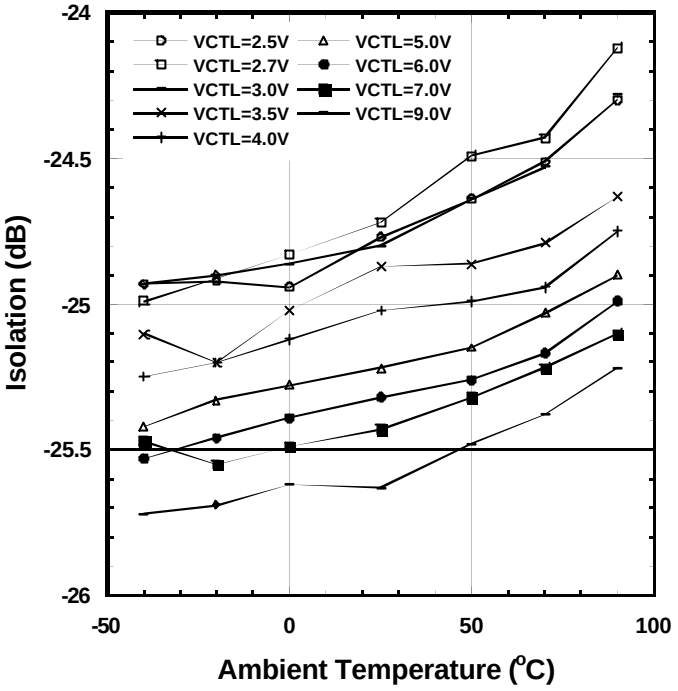
**Isolation vs. Ambient Temperature**

**(PC-P1,f=1GHz,Input Power=34.5dBm)**



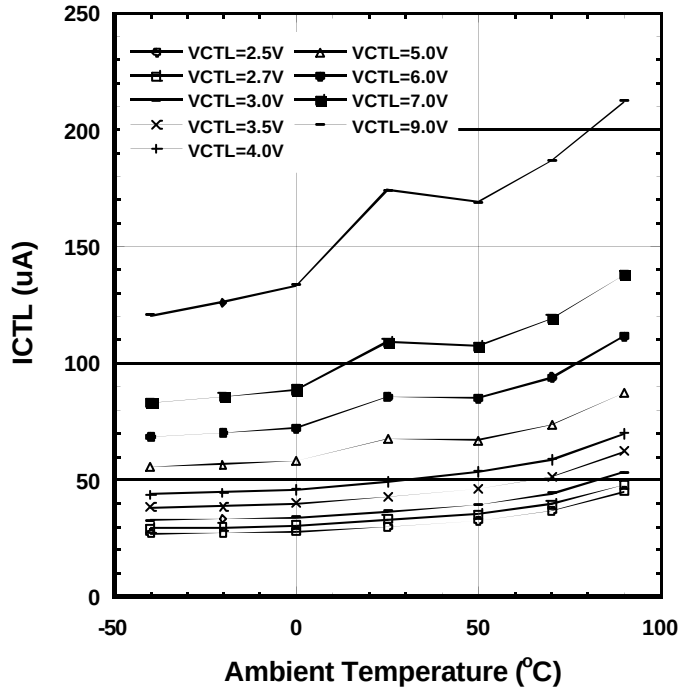

**Isolation vs. Ambient Temperature**

**(PC-P1,f=2GHz,Input Power=31.5dBm)**




**ICTL vs. Ambient Temperature**

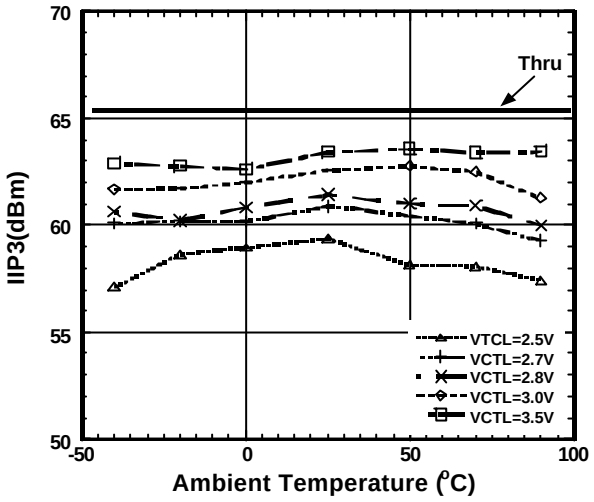
**(PC-P1,f=1GHz,Input Power=34.5dBm)**



■ **TEMPERATURE CHARACTERISTICS** (with application circuit, Parts list 3)

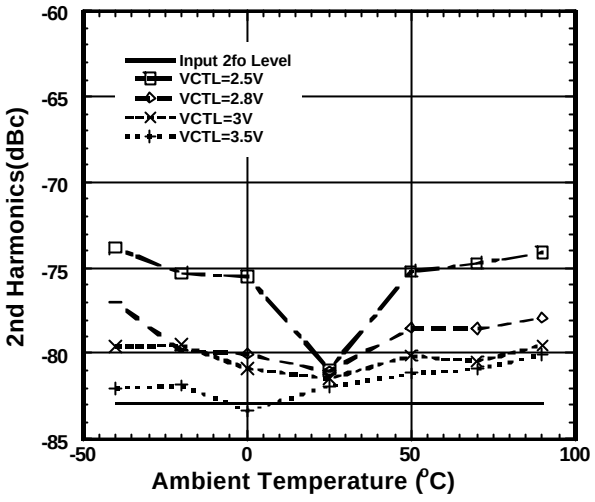
**IIP3 vs. Ambient Temperature**

(PC-P1,f=900+901MHz,Input Power=25dBm)



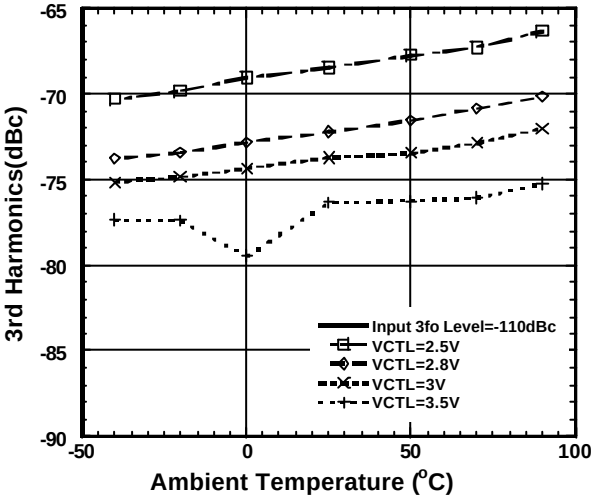

**2nd Harmonics vs. Ambient Temperture**

(f=900MHz,Input Power=25dBm)



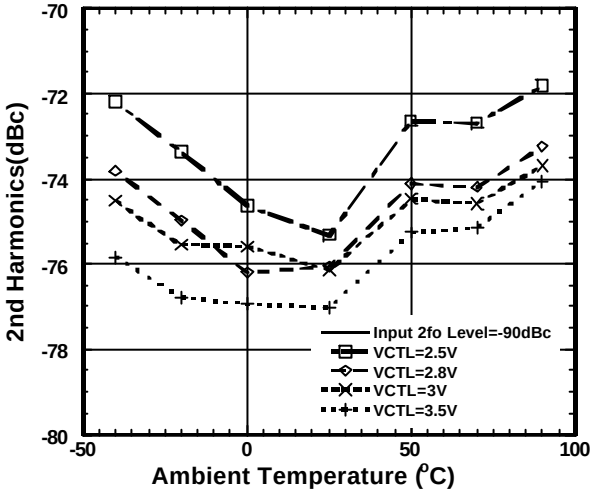

**3rd Harmonics vs. Ambient Temperture**

(f=900MHz,Input Power=25dBm)



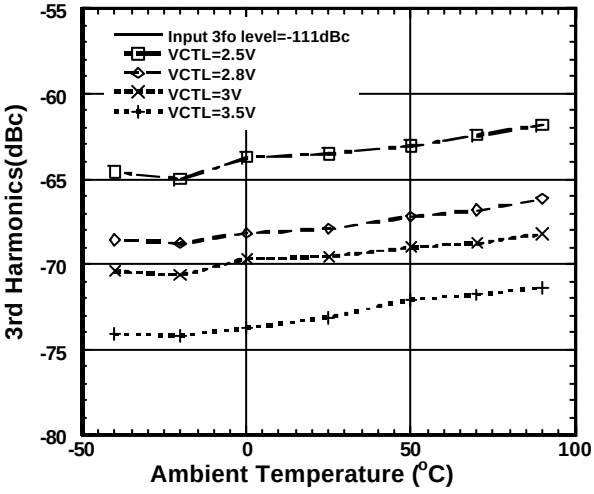

**2nd Harmonics vs. Ambient Temperture**

(f=1800MHz,Input Power=25dBm)

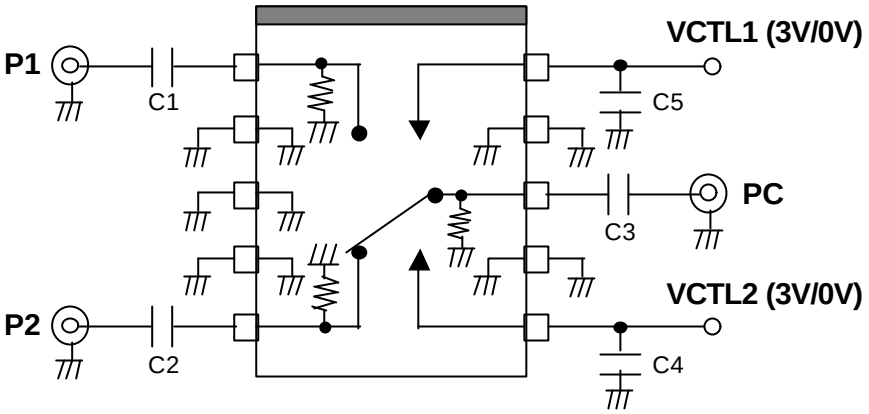



**3rd Harmonics vs. Ambient Temperture**

(f=1800MHz,Input Power=25dBm)

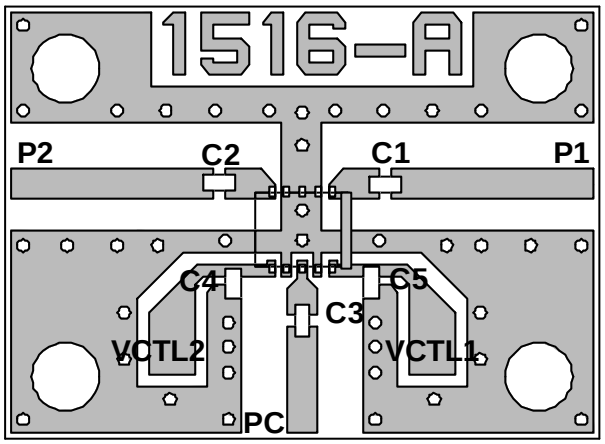


■**APPLICATION CIRCUIT 1** (Parts list 1~3)




■**RECOMMENDED PCB DESIGN**

(TOP VIEW)




PCB: FR-4, t=0.5mm
Capacitor: size 1005
Strip Line Width=1.0mm
PCB SIZE: 14.0x19.4mm

■Circuit losses including losses of capacitors and connectors.

| Frequency (GHz) | Loss (dB) |
|---|---|
| 0.8 | 0.12 |
| 1.0 | 0.13 |
| 1.5 | 0.17 |
| 1.8 | 0.19 |
| 2.0 | 0.20 |
| 2.5 | 0.26 |

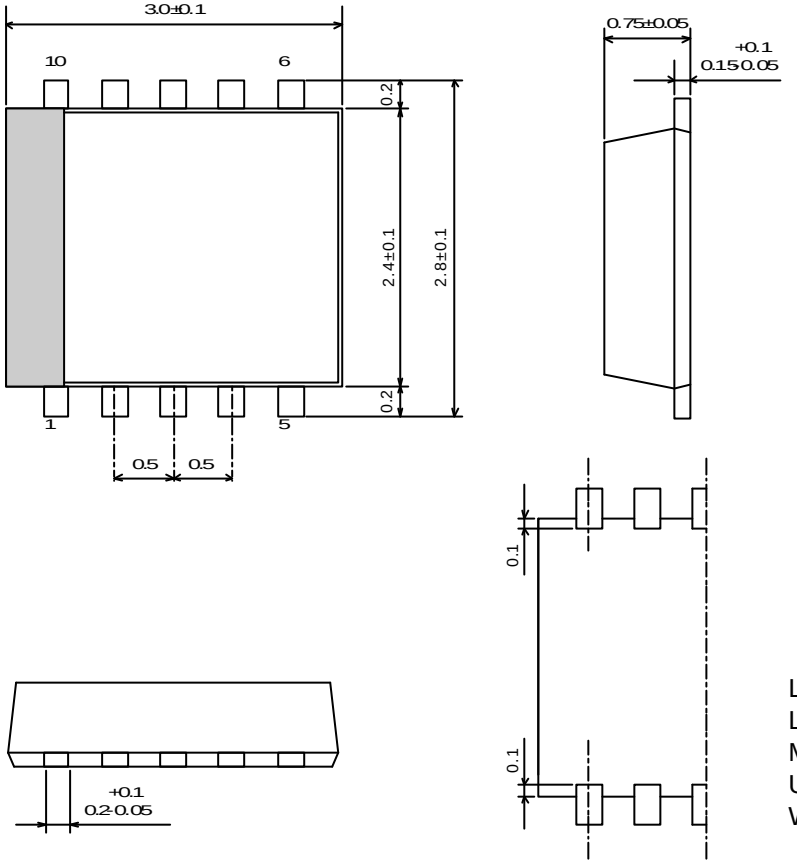
■PARTS LIST

| PART ID | 1 | 2 | 3 |
|---|---|---|---|
| Freq (MHz) | 50~100 | 100~500 | 500~2000 |
| C1~C3 | 0.01uF | 1000pF | 56pF |
| C4, C5 | 10pF | 10pF | 10pF |

**PRECAUTIONS**

[1]The DC blocking capacitors have to be placed at RF terminal of P1, P2 and PC.
[2]Bypass capacitors (C4, C5) should be placed close to terminals of VCTL1, VCTL2 to reduce stripline influence of RF characteristics.
[3]For good isolation, the GND terminal ($3^{rd}$, $6^{th}$, $7^{th}$ pin) must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.
[4] To avoid degradation of isolation or high power characteristics, please layout ground pattern right under this IC.

## ■ PACKAGE OUTLINE (FLP10-C1)




| | |
|---|---|
| Lead material | : Copper |
| Lead surface finish | : Solder plating |
| Molding material | : Epoxy resin |
| UNIT | : mm |
| Weight | : 15mg |

**Cautions on using this product**

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

[CAUTION]
The specifications on this databook are only given for information , without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.