DRAM

1 MEG x 4 DRAM

FAST PAGE MODE, WRITE-PER-BIT

FEATURES

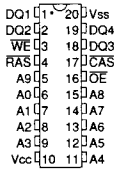
- Industry standard x4 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), and HIDDEN
- WRITE-PER-BIT access cycle (nonpersistent)
- 300 and 350 mil wide SOJ packages
- Two CBR options: CBR with $\overline{WE}$ a don't care (1 Meg compatible) and CBR with $\overline{WE}$ a HIGH (JEDEC test mode capable via WCBR)

OPTIONS — MARKING

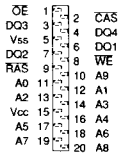
- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Ceramic DIP (400mil) — C
  - Plastic ZIP (350mil) — Z
  - Plastic SOJ (300mil) — DJ
  - Plastic SOJ (350mil) — DJW
  - Plastic TSOP (*) — TG
- $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh
  - CBR with $\overline{WE}$ a don't care — None
  - CBR with $\overline{WE}$ a HIGH — J
- Operating Temperature, T_A
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT

PIN ASSIGNMENT (Top View)

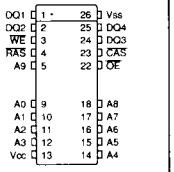
20-Pin CDIP (B-5)



20-Pin ZIP (C-3)



20-Pin SOJ (E-1, E-2)



*Consult factory on availability of TSOP packages

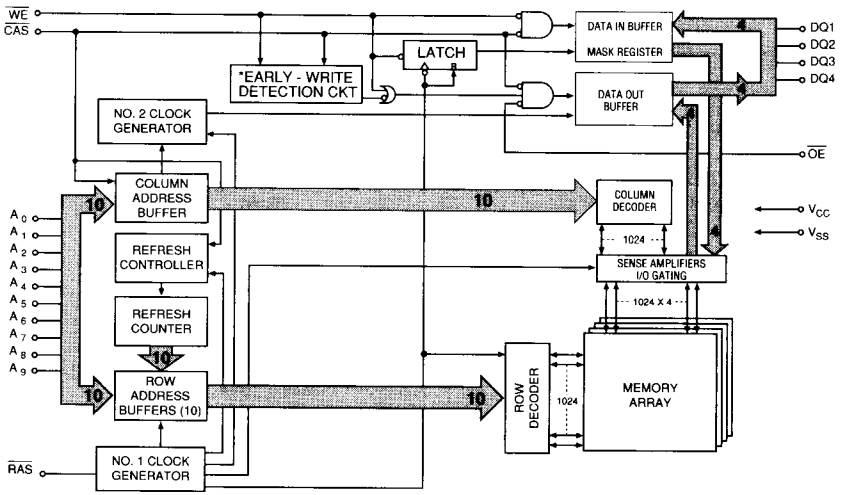
GENERAL DESCRIPTION

The MT4C4005 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$. The WRITE-PER-BIT feature allows the user to define WRITE MASK during a WRITE cycle when $\overline{RAS}$ goes LOW, depending on the state of $\overline{WE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses ^tR	Addresses ^tC	$\overline{OE}$	DATA IN / OUT DQ1-4	NOTES
Standby		H	X	X	X	X	X	High-Z	
READ		L	L	H	ROW	COL	L	Valid Data Out	
EARLY-WRITE		L	L	L	ROW	COL	X	Valid Data In	1
READ-WRITE		L	L	H→L	ROW	COL	L→H	Valid Data Out, Data In	1
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	L	Valid Data Out	
	2nd Cycle	L	H→L	H	n/a	COL	L	Valid Data Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	X	Valid Data In	1
	2nd Cycle	L	H→L	L	n/a	COL	X	Valid Data In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	L→H	Valid Data Out, Data In	1
	2nd Cycle	L	H→L	H→L	n/a	COL	L→H	Valid Data Out, Data In	1
$\overline{RAS}$-ONLY REFRESH		H	X	X	ROW	n/a	X	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	L	Valid Data Out	
	WRITE	L→H→L	L	L	ROW	COL	X	Valid Data In	1
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	Standard	H→L	L	X	X	X	X	High-Z	
	"J" Option	H→L	L	H	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided. Refer to Figure 1.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3, 5

MASKED WRITE ACCESS CYCLE

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ4 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

For nonpersistent MASK WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C4005 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

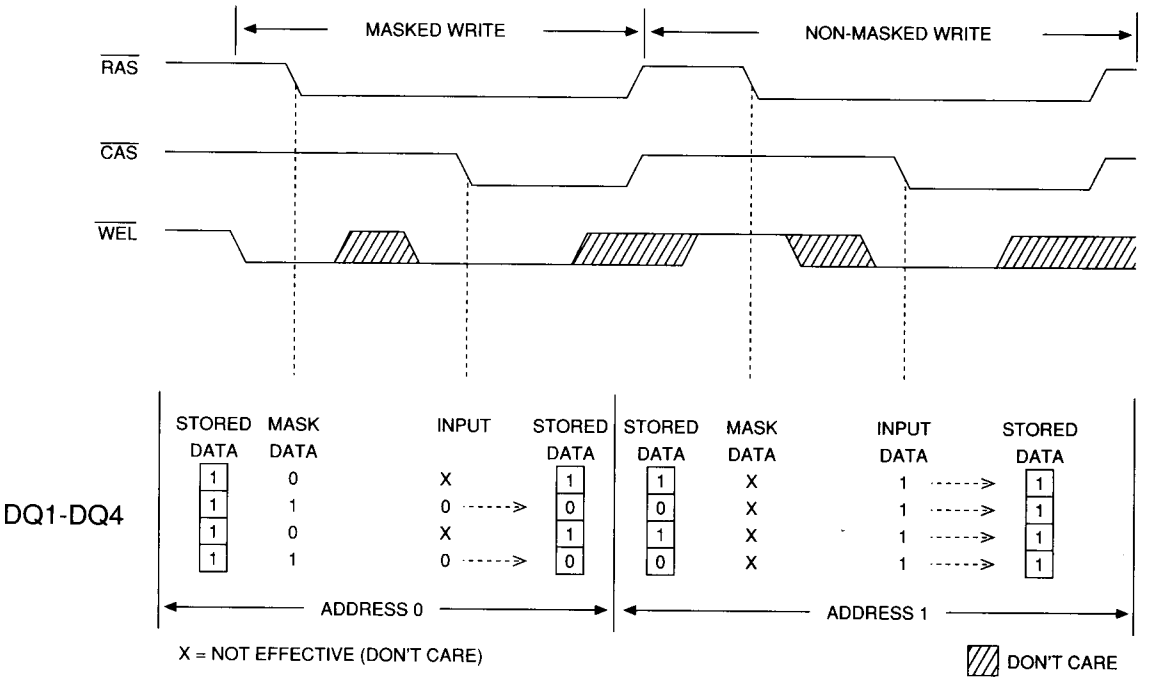


Figure 1
MT4C4005 MASKED WRITE EXAMPLE

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	90		95		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	21, 27

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

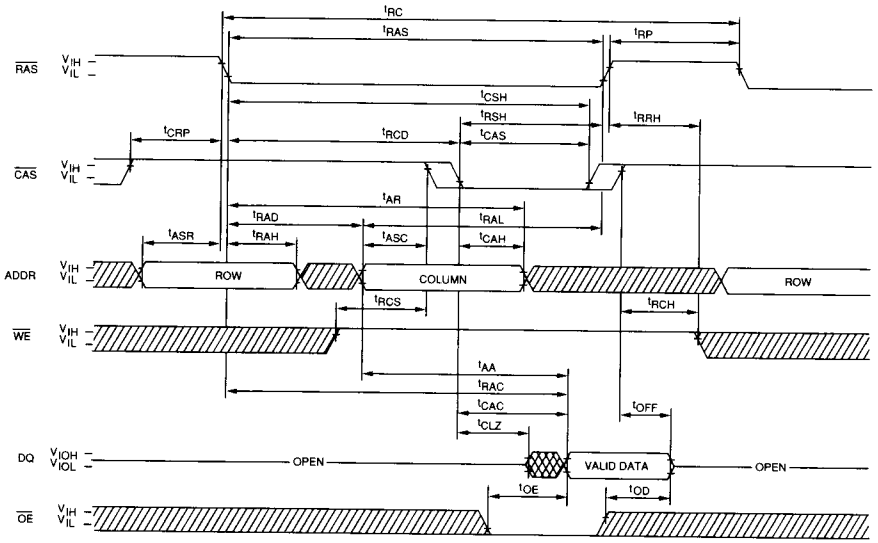
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^{t}WCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		60		ns	
Write command pulse width	^{t}WP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		20		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22
Data-in hold time	^{t}DH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	90		100		110		ns	21
Column address to $\overline{WE}$ delay time	^{t}AWD	60		65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	45		50		50		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	^{t}REF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}WRH	10		10		10		ns	25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}WRP	10		10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^{t}WTH	10		10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^{t}WTS	10		10		10		ns	25
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
Output disable	^{t}OD	15		20		20		ns	27
Output enable	^{t}OE	15		20		20		ns	23
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		20		20		ns	26
WRITE-PER-BIT setup time	^{t}WBS	0		0		0		ns	
WRITE-PER-BIT hold time	^{t}WBH	10		10		10		ns	
WRITE-PER-BIT mask setup time	^{t}WDS	0		0		0		ns	
WRITE-PER-BIT mask hold time	^{t}WDH	10		10		10		ns	

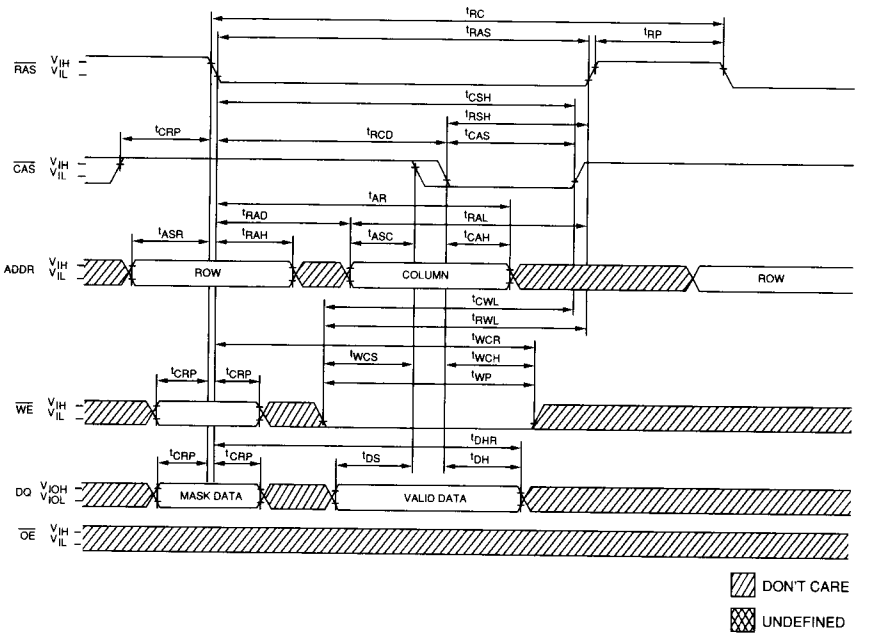
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

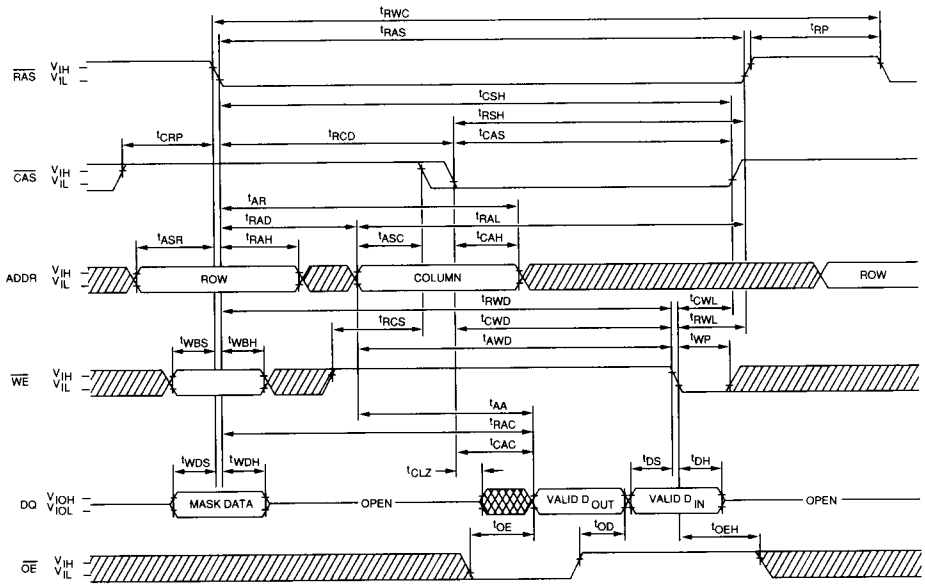
READ CYCLE



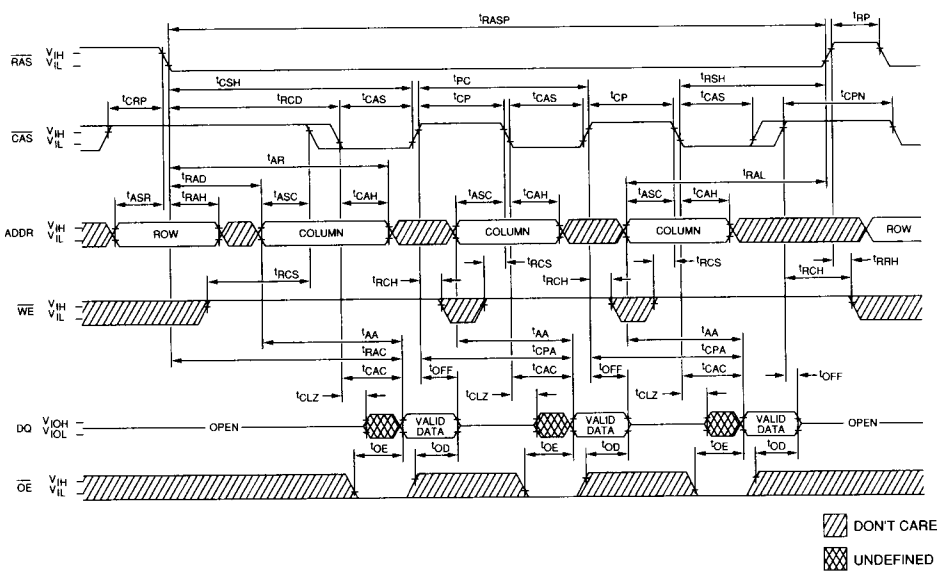
EARLY-WRITE CYCLE



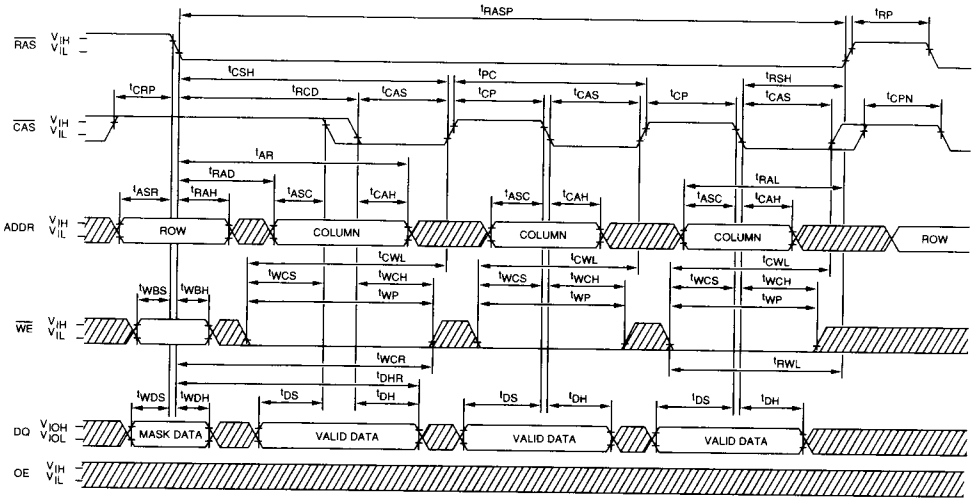
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



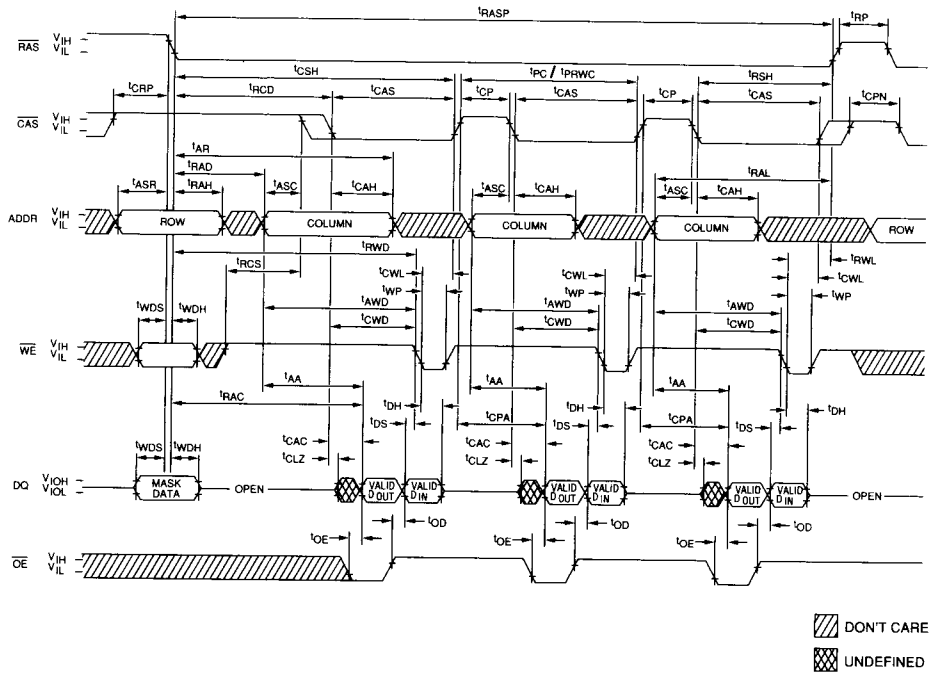
FAST-PAGE-MODE READ CYCLE



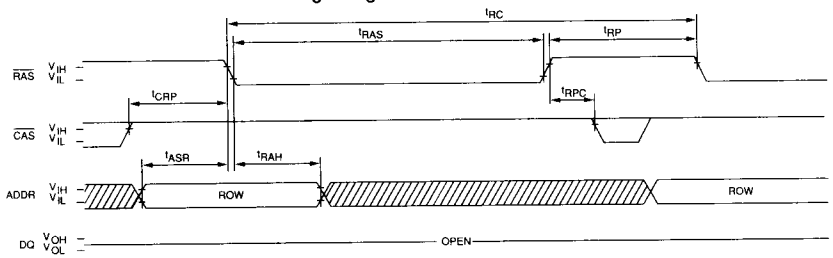
FAST-PAGE-MODE EARLY-WRITE CYCLE



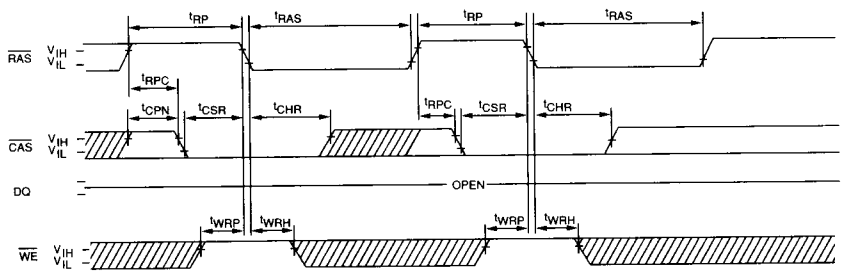
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



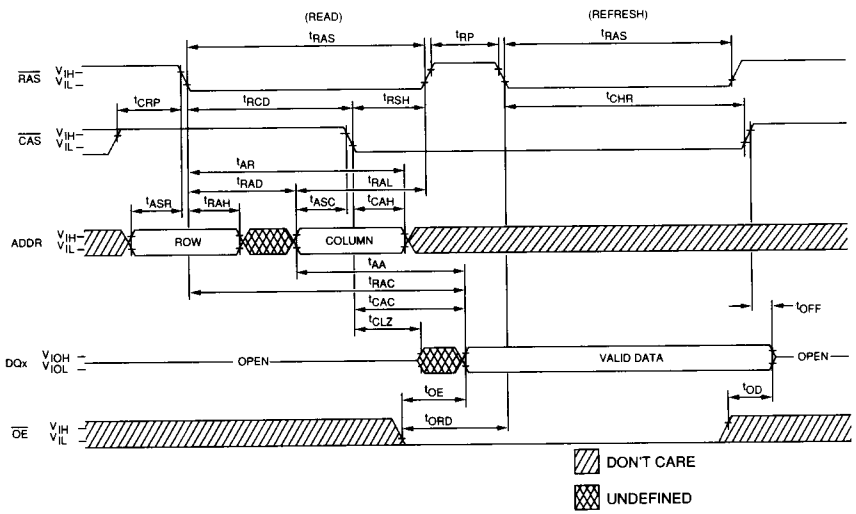
RAS-ONLY REFRESH CYCLE
(ADDR = A_0 - A_9; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A_0 - A_9, and OE = DON'T CARE)



HIDDEN REFRESH CYCLE
(WE = HIGH; OE = LOW) [24]



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a don't care. The 4 Meg, on the other hand, specifies the CBR REFRESH mode to be a $\overline{W}$CBR, which is CBR with the $\overline{WE}$ pin held at a logical HIGH level.

The reason for $\overline{W}$CBR instead of CBR on the 4 Meg is that a CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode ($\overline{W}$CBR). In contrast, the 1 Meg test mode is entered by applying a HIGH signal to the test pin (pin 4 on DIP, pin 5 on SOJ and pin 8 on ZIP). This HIGH signal is usually a "supervoltage" (V in ≥ 7.5V) so normal TTL or CMOS HIGH levels will not cause the part to enter the test mode.

POWER-UP

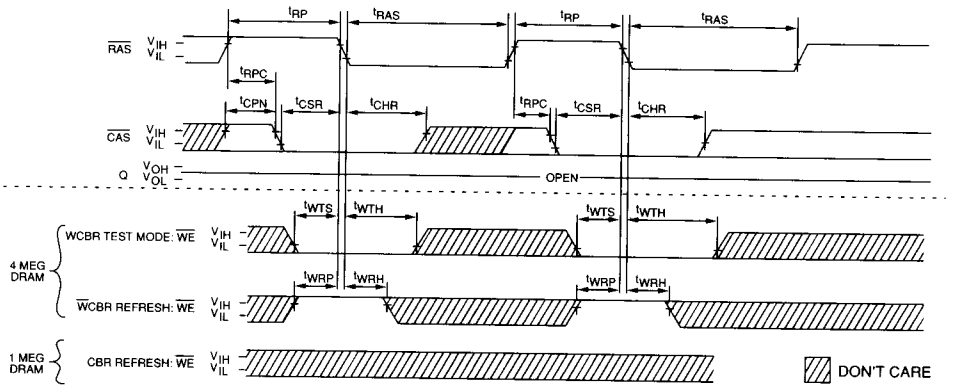
The 4 Meg $\overline{W}$CBR constraint may also introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any 8 $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that 8 $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a $\overline{W}$CBR REFRESH cycle.

SUMMARY

1. The optional 1 Meg test pin is the A10 pin on the 4 Meg (x1 only).
2. For optional test mode, the 1 Meg requires a valid HIGH on the test pin while the 4 Meg requires a CBR cycle with $\overline{WE}$ LOW.
3. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be don't care while the 4 Meg CBR requires $\overline{WE}$ to be HIGH ($\overline{W}$CBR).
4. The 8 $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or $\overline{W}$CBR REFRESH cycles.

SPECIAL FEATURE

A memory system currently using 1 Meg DRAMs with $\overline{WE}$ as a don't care during CBR REFRESH does not allow for direct upgrading to 4 Meg DRAMs. Micron, realizing some companies will have this situation, provides a special feature on its 4 Meg DRAM, that requires "supervoltage" to access the 4 Meg JEDEC WCBR test function. This allows the Micron 4 Meg DRAM to be refreshed in the same manner as any 1 MEG DRAM. Note that the eight power-up cycles should only be refresh cycles in order to guarantee that any 4 Meg DRAM, including Micron's, does not inadvertently power-up in the test mode.



COMPARISON OF 4 MEG TEST MODE AND $\overline{W}$CBR TO 1 MEG CBR