OKI Semiconductor

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MSM7575

Multi-Function PCM CODEC

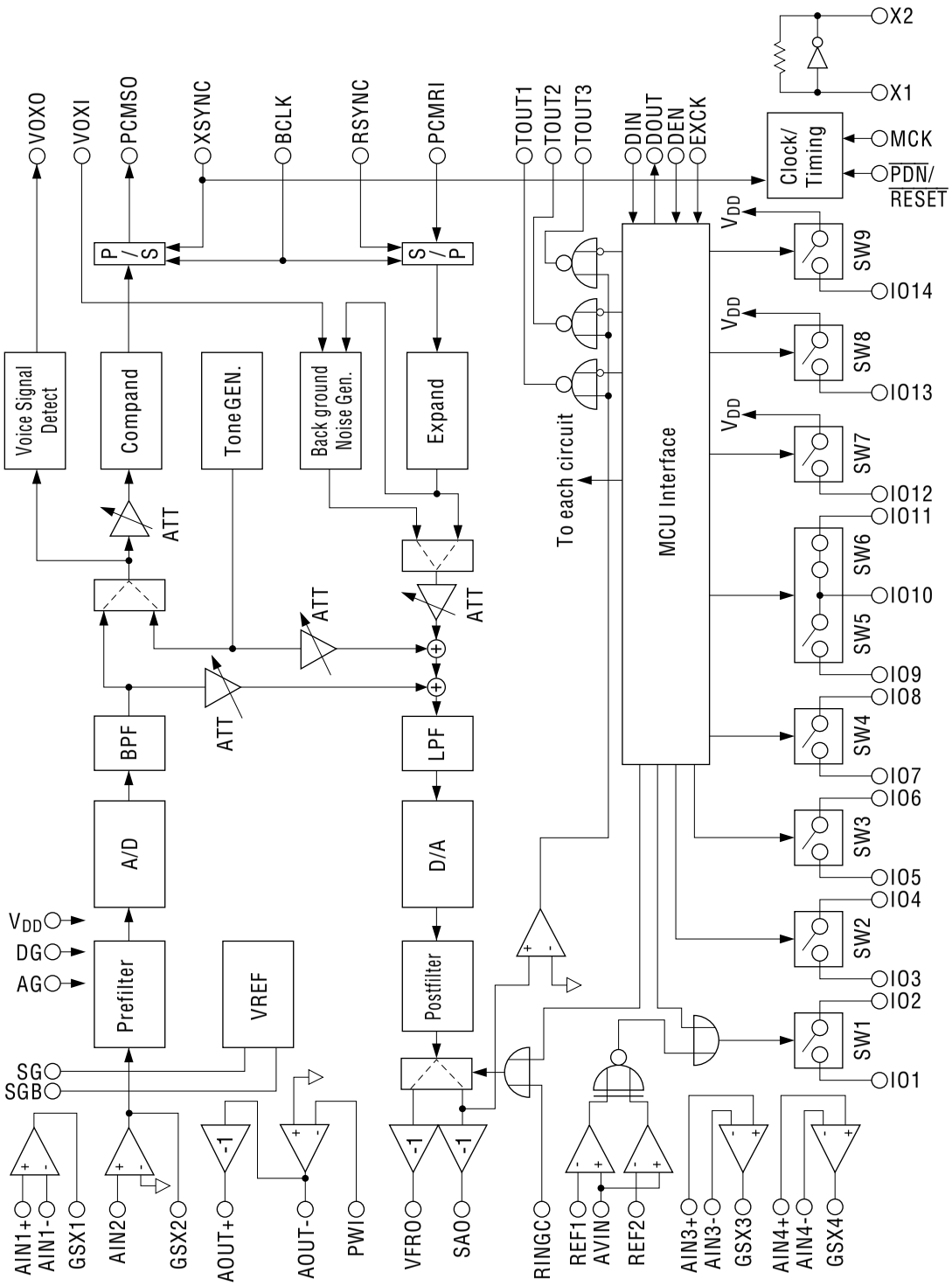
GENERAL DESCRIPTION

The MSM7575, developed for advanced digital cordless telephone systems, is a single channel full duplex CODEC which performs mutual transcoding between the analog voice band signal and the 64 kbps PCM serial data.
This device performs DTMF tone and several kinds of tone generation, transmit/receive data mute and gain control, side-tone pass and its gain control, and VOX function.
Using advanced circuit technology, this device operates from a single 3 V power supply and provides low power consumption.

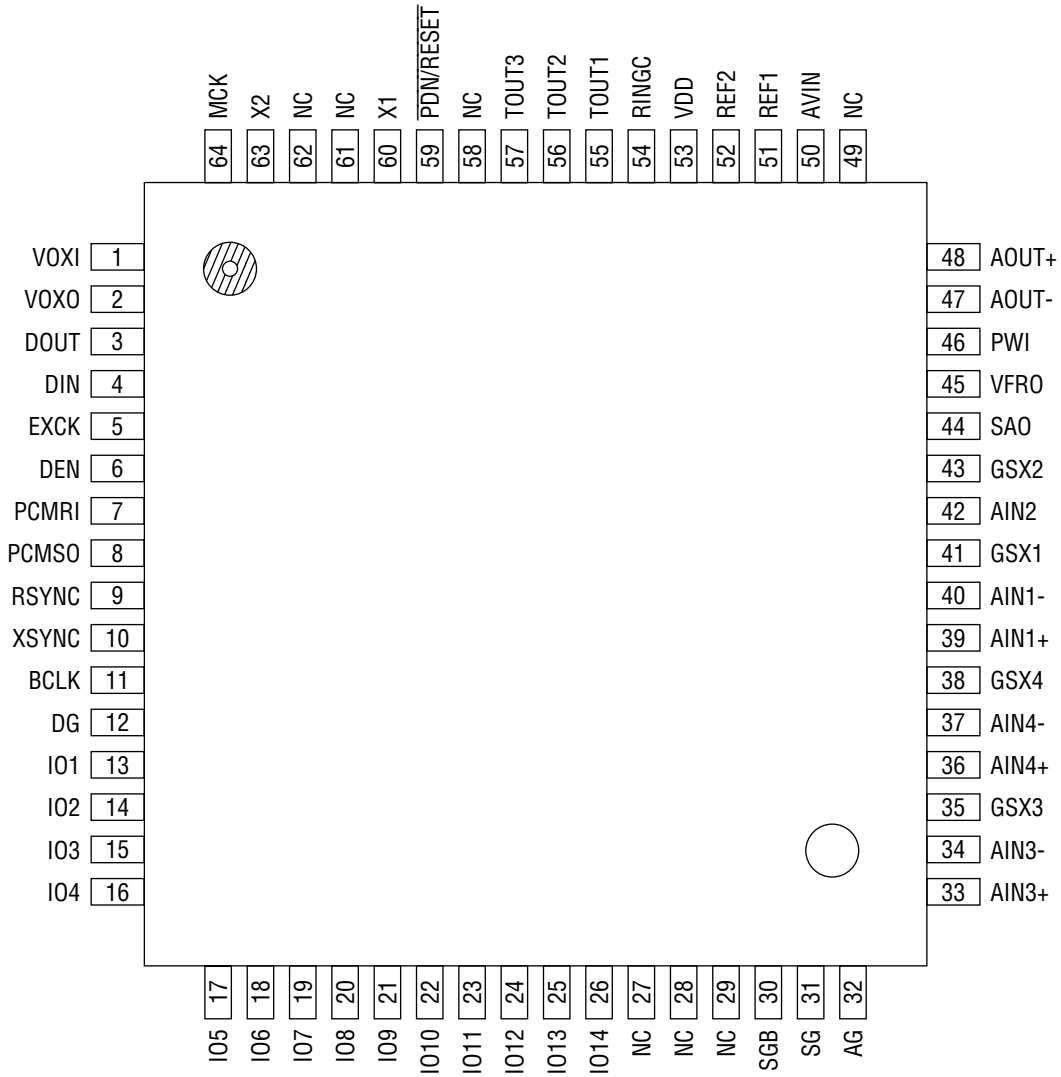
FEATURES

- Single 3 V Power Supply Operation V_{DD}: 2.7 V to 3.6 V
- Transmit/Receive Full-Duplex Single Channel Operation
- Transmit/Receive Synchronous Mode Only
- PCM Interface Data Format : A-law/μ-law/linear (2's complement) Selectable
- Serial PCM Transmission Data Rate : 64 kbps to 2048 kbps
- Low Power Consumption
  - Operating Mode : 24 mW Typ. (V_{DD} = 3.0 V)
  - Power-Down Mode : 0.03 mW Typ. (V_{DD} = 3.0 V)
- Two Analog Input Amplifier Stages: Externally Gain Adjustable
- Analog Output Stage
  Push-pull Drive (direct drive of 350 Ω + 120 nF)
- Master Clock Frequency : 9.600/19.200 MHz Selectable
- Transmit/Receive Mute, Transmit/Receive Programmable Gain Control
- Side Tone Path with Programmable Attenuation (8-step Level Adjustment)
- Built-in DTMF Tone Generator
- Built-in Various Ringing Tones Generator
- Built-in Various Ring Back Tone Generator
- Control by Serial MCU Interface
- Built-in VOX Control
  - Transmit side : Voice/Silence Signal Detect
  - Receive side : Background Noise Generation
- Built-in Op-amps and Analog Switches for Various Analog Interfaces.
- Package:
  64-pin plastic QFP (QFP64-P-1414-0.80-BK)(Product name : 7575GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

NC : No connect pin

PIN AND FUNCTIONAL DESCRIPTIONS

AIN1+, AIN1–, AIN2, GSX1, GSX2

Transmit analog input and the output for transmit gain adjustment. The pin AIN1– (AIN2) connects to the inverting input of the internal transmit amplifier, and the pin AIN1+ connects to the non-inverting input of the internal transmit amplifier. The pin GSX1 (GSX2) connects to output of the internal transmit amplifier. Gain adjustment should be referred to Fig. 1.

VFRO, AOUT+, AOUT–, PWI, SAO, RINGC

Used for the receive analog output and the output for receive gain adjustment. VFRO is an output of the receive filter. AOUT+ and AOUT– are differential analog signal outputs which can directly drive Z_L = 350 Ω + 120 nF or the 1.2 kΩ load. Gain adjustment should be referred to Fig. 1.

The ORed signal with the control register data CR4-B5 and the external pin RINGC determines the output pins (AOUT+ and AOUT- /SAO+ and SAO-) for the speech signal and an acoustic component of the sounder tone, DTMF tone, R tone, F tone, various kinds of tones at either the VFRO pin or the SAO pin.

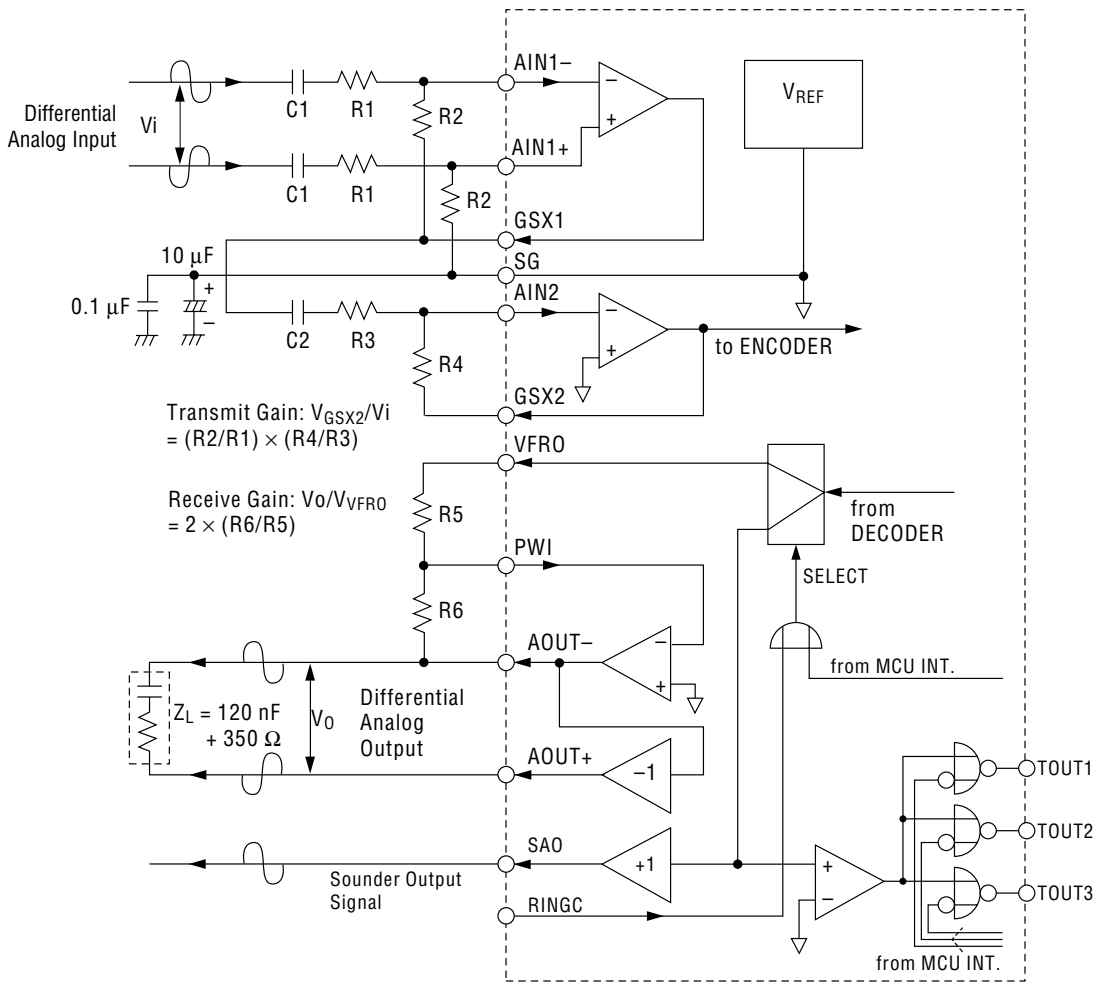


Figure 1 Analog Input/Output Interface

TOUT1, TOUT2, TOUT3

These are pins for outputs of the NOR gates whose inputs are the comparator output signal between the SAO output level and the SG level, and each register signal stored by the MCU interface.
The each output is NOR-gated with the comparator output and the invented signal of CR1-B7 at TOUT3, the inverted signal of CR1-B6 at TOUT2, and the inverted signal of CR1-B5 at TOUT1.

AVIN, REF1, REF2

These pins are for inputs of two comparators internal to the device. AVIN is connected to each non-inverting input of comparator1 and comparator2. REF1 is connected to an inverting input of comparator1 and REF2 is connected to an inverting input of comparator2. The output of each comparator is connected to the input of ENOR. The interval analog switch SW1 is ON/OFF controlled by the output which is the logical OR of the ENOR and the CR5-B7 signal. When CR5-B7 is at "0", the SW1 is turned to OFF if AVIN is within the voltage range of REF1 and REF2 and the SW1 is turned to ON if AVIN is out of the voltage range of REF1 and REF2.

AIN3+, AIN3-, GSX3, AIN4+, AIN4-, GSX4

These pins are for inputs and outputs of the internal op-amps. Refer to BLOCK DIAGRAM for the connection.

IO1 to IO14

These pins are for inputs and outputs of the internal analog switch. Refer to BLOCK DIAGRAM and FUNCTIONAL DESCRIPTION for the connection and the control method.

X1, X2

Crystal oscillator connection pins. X2 is for the clock output pin. When a conventional external clock is used, X1 should be connected to the ground, X2 should be left open, and the clock should be input to the MCK pin.

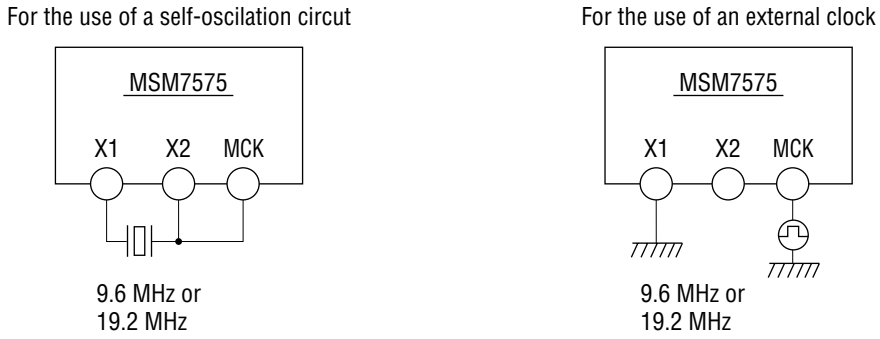


Figure 2 Connection to a Crystal Oscillator or an External Clock

SG, SGB

Analog signal ground output.
The output voltage is about 1.4 V. The bypass capacitors (10 µF in parallel with 0.1 µF ceramic type) should be put between this pin and AG to get the specified noise characteristics. This output voltage is 0 V during power-down.

AG

Analog ground.

DG

Digital ground.
This ground is separated from the analog signal ground(AG) in this device. The DG pin must be kept as close to the AG pin possible on the PCB.

V_{DD}

+3 V power supply.

$\overline{\text{PDN/RESET}}$

Power down and reset control input.
"L" level makes the whole chip enter to power down state, and, at the same time, all of control register data are reset to the initial state. Set this pin to "H" level during normal operating mode. The power down state is controlled by a logical OR with CR0-B5 of the control register. When using the pin $\overline{\text{PDN/RESET}}$ for the power down and reset control, CR0-B5 should be set to digital "0".

MCK

Master clock input.
The frequency must be 9.6 MHz or 19.2 MHz. The applied clock frequency is selected by the control register data CR0-B6. The master clock signal is allowed to be asynchronous with BCLK, XSYNC, and RSYNC.

PCMSO

Transmit PCM data output.
This PCM output signal is output from MSB in synchronization with the rising edge of BCLK or XSYNC. A pull-up resistor must be connected to this pin, because this output is configuared as an open drain.
During power down, this output is at high impedance state.

PCMRI

Receive PCM data input.
This PCM input signal is shifted on the falling edge of BCLK and input from MSB.

BCLK

Shift clock input for the PCM data (PCMSO, PCMRI).
The frequency is set in the range of 64 kHz to 2048 kHz.

XSYNC

8 kHz synchronous signal input for Transmit PCM data.
This signal should be synchronized with BCLK. XSYNC is used for indicating MSB of the transmit serial PCM.
Be sure to input the XSYNC signal because it is also used as the input of the timing circuit and the clock source of the tone generator.

RSYNC

8 kHz synchronous signal input for Receive PCM data.
This signal should be synchronized with BCLK signal. RSYNC is used for indicating the MSB of the receive serial PCM.

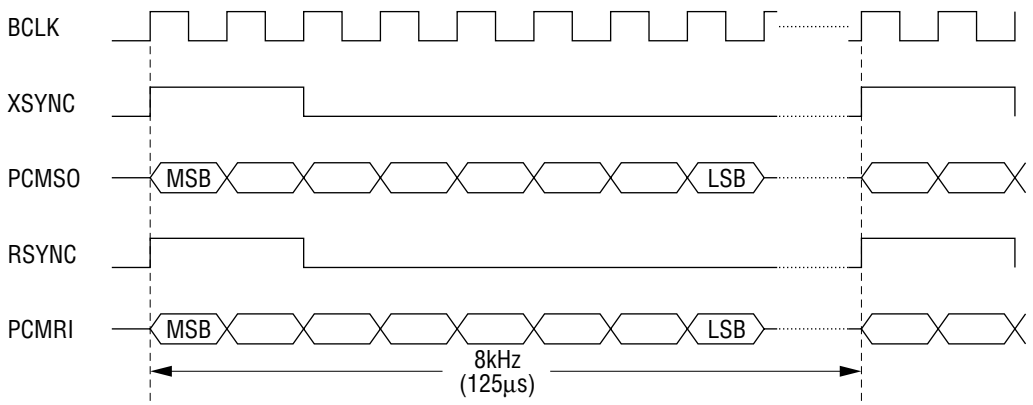


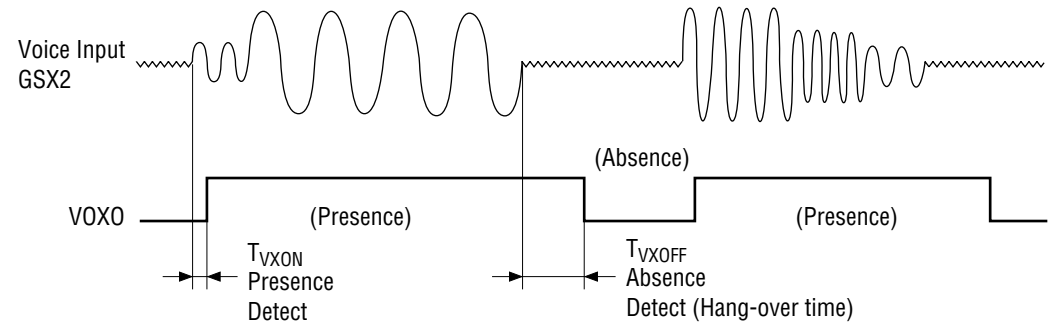
Figure 3 PCM Interface Basic Timing Diagram

VOXO

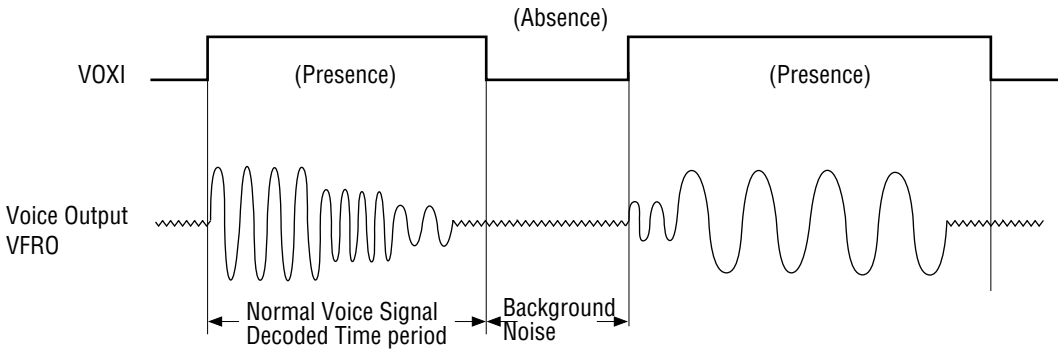
Transmit VOX function signal output.
VOX function is to recognize the presence or absence of the transmit voice signal by detecting the signal energy. "H" and "L" levels set to this pin correspond to the presence and the absence, respectively. This result appears also at the register data CR7-B7. The signal energy detect threshold is set by the control register data CR6-B6, B5.

VOXI

Signal input for receive VOX function.
The "H" level at VOXI indicates the presence of voice signal, the decoder block processes normal receive signal, and the voice signal appears at analog output pins . The "L" level indicates the absence of voice signal, the background noise generated in this device is transferred to the analog output pins. The background noise amplitude is set by the control register CR6. Because this signal is ORed with the register data CR6-B3, the control register data CR6-B3 should be set to digital "0".



(a) Transmit VOX Function Timing Diagram



(b) Receive VOX Function (CR6-B3: digital "0") Timing Diagram

Note: VOXO, VOXI function become valid when setting CR6-B7 to digital "1".

Figure 4 VOX Function

DEN , EXCK, DIN, DOUT

Serial control ports for MCU interface. Reading and writing data is performed by an external MCU through these pins. Total 8 registers with 8 bits are provided on the devices.
DEN is the "Enable" control signal input, EXCK is the data shift clock input, DIN is the address and data input, and DOUT is the data output from which inverted data of the contents of the register is output.
Fig.5 shows the input or output timing diagram.

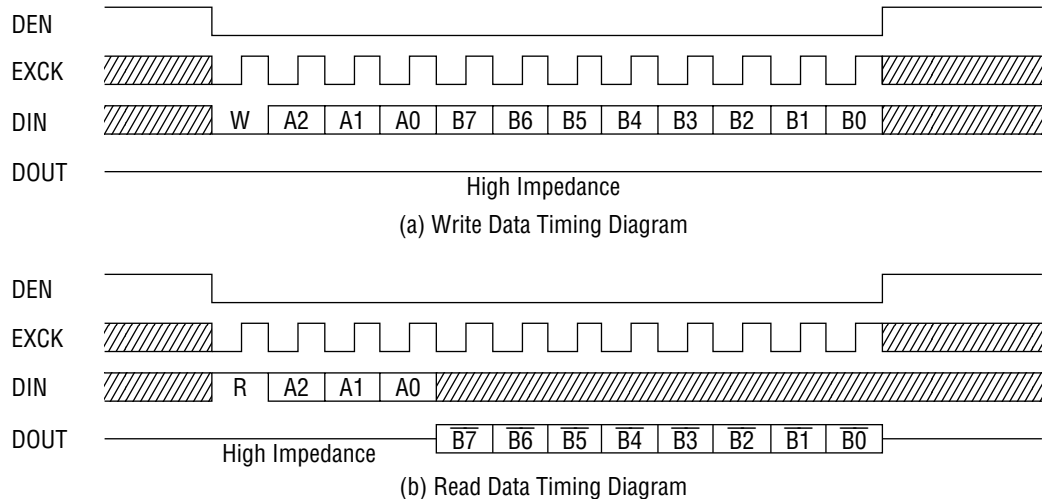


Figure 5 MCU Interface Input/Output Timing

Register map is shown below.

Table-1

Name	Address			Control and Detect Data								R/W
	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	A/μ SEL	MCK SEL	PDN ALL	PDN TX	PDN RX	—	LNR	PDN SAO/AOUT	R/W
CR1	0	0	1	TOUT3 -CONT	TOUT2 -CONT	TOUT1 -CONT	—	—	—	—	RX PAD	R/W
CR2	0	1	0	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR3	0	1	1	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0	R/W
CR4	1	0	0	DTMF/ OTHERS SEL	TONE SEND	SAO/ VFRO	TONE4	TONE3	TONE2	TONE1	TONE0	R/W
CR5	1	0	1	SW7- CONT	SW8- CONT	SW9- CONT	SW5& SW6-CONT	SW4- CONT	SW3- CONT	SW2- CONT	SW1- CONT	R/W
CR6	1	1	0	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LEVEL SEL	RX NOISE LVL1	RX NOISE LVL0	R/W
CR7	1	1	1	VOX OUT	TX NOISE LVL1	TX NOISE LVL0	—	—	—	—	—	R

R/W : Enable to read/write R : Read only register.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +5	V
Analog Input Voltage	V_{AIN}	—	– 0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{op}	—	–30 to +85	°C
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	+2.7	—	+3.6	V
Operating Temperature Range	Ta	—	–25	+25	+70	°C
Input High Voltage	V_{IH}	MCK, XSYNC, RSYNC, PCMRI, RINGC, BCLK, VOXI, $\overline{\text{PDN/RESET}}$, DEN, EXCK, DIN	$0.45 \times V_{DD}$	—	V_{DD}	V
Input Low Voltage	V_{IL}	MCK, XSYNC, RSYNC, PCMRI, RINGC, BCLK, VOXI, $\overline{\text{PDN/RESET}}$, DEN, EXCK, DIN	0	—	$0.16 \times V_{DD}$	V
Master Clock Frequency	f_{MCK1}	MCK (CR0–B6 = "0")	–0.01%	9.600	+0.01%	MHz
	f_{MCK2}	MCK (CR0–B6 = "0")	–0.01%	19.200	+0.01%	MHz
Bit Clock Freqency	f_{BCK}	BCLK	64	—	2048	kHz
Synchronous Signal Frequncy	f_{SYNC}	XSYNC, RSYNC	—	8.0	—	kHz
Clock Duty Ratio	D_C	MCK, BCLK, EXCK	30	50	70	%
Digital Input Rise Time	t_{Ir}	MCK, XSYNC, RSYNC, PCMRI, RINGC, BCLK, VOXI, $\overline{\text{PDN/RESET}}$, DEN, EXCK, DIN	—	—	50	ns
Digital Input Fall Time	t_{If}	MCK, XSYNC, RSYNC, PCMRI, RINGC, BCLK, VOXI, $\overline{\text{PDN/RESET}}$, DEN, EXCK, DIN	—	—	50	ns
Transmit Sync Signal Setting Time	t_{XS}	BCLK to XSYNC	100	—	—	ns
	t_{SX}	XSYNC to BCLK	100	—	—	ns
Receive Sync Signal Setting Time	t_{RS}	BCLK to RSYNC	100	—	—	ns
	t_{SR}	RSYNC to BCLK	100	—	—	ns
Synchronous Signal Width	t_{WS}	XSYNC, RSYNC	1 BCLK	—	100	µs
PCM Set-up Time	t_{DS}	—	100	—	—	ns
PCM Hold Time	t_{DH}	—	100	—	—	ns
Digital Output Load	R_{DL}	PCMSO (Pull-up Resistor)	500	—	—	Ω
	C_{DL}	TOUT1, TOUT2, TOUT3, PCMSO, VOXO, DOUT	—	—	100	pF
Bypass Capacitors for SG	C_{SG}	SG to AG	10 + 0.1	—	—	µF

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating Mode, (V_{DD} = 3.0 V)	—	8	6	mA
	I_{DD2}	Power Down Mode, (V_{DD} = 3.0 V)	—	0.01	0.1	mA
Input High Voltage	V_{IH}	—	0.45×V_{DD}	—	V_{DD}	V
Input Low Voltage	V_{IL}	—	0.0	—	0.16×V_{DD}	V
Input Leakage Current	I_{IH}	V_I = V_{DD}	—	—	2.0	µA
	I_{IL}	V_I = 0 V	—	—	0.5	µA
Output High Voltage	V_{OH}	I_{OH} = 0.4 mA	0.5 × V_{DD}	—	V_{DD}	V
		I_{OH} = 1 µA	0.8 × V_{DD}	—	V_{DD}	V
Output Low Voltage	V_{OL}	1 LSTTL, Pull-up: 500 Ω	0.0	0.2	0.4	V
Output Leakage Current	I_O	PCMSO	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF
Output Resistance	R_{OSG}	SG	—	25	50	kΩ

Transmit Analog Interface Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	AIN1+ , AIN1– , AIN2	10	—	—	MΩ
Output Load Resistance	R_{LGX}	GSX1, GSX2	20	—	—	kΩ
Output Load Capacitance	C_{LGX}	GSX1, GSX2	—	—	100	pF
Output Amplitude	V_{OGX}	GSX1, GSX2, R_L = 20 kΩ	—	—	1.30 (*1)	V_{PP}
Input Offset Voltage	V_{OFGX}	Pre–OPAMPs	–20	—	20	mV

*1 –7.7 dBm (600 Ω) = 0 dBm0, + 3.17 dBm0 = 1.30 V_{PP} (µ-law Selected)

Receive Analog Interface Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	R_{INPW}	PWI, AIN3+/–, AIN4+/–, REF1, REF2, AVIN		10	—	—	MΩ
Output Load Resistance	R_{LVF}	VFRO, SAO		20	—	—	kΩ
	R_{LAO}	AOUT+, AOUT–, GSX3, GSX4		1.2	—	—	kΩ
Output Load Capacitance	C_{LVF}	VFRO, SAO		—	—	100	pF
	C_{LAO}	AOUT+, AOUT–, GSX3, GSX4		—	—	100	pF
Output Voltage Level	V_{OVF}	VFRO, SAO R_L = 20 kΩ		—	—	1.30 (*1)	V_{PP}
	V_{OAO}	AOUT+, AOUT–, GSX3, GSX4	R_L = 1.2 kΩ	—	—	1.30 (*1)	V_{PP}
			Z_L = 350 kΩ + 120 nF(See Fig.1)	—	—	1.30 (*1)	V_{PP}
Offset Voltage	V_{OFVF}	VFRO, SAO		–100	—	100	mV
	V_{OFAO}	AOUT+, AOUT– (Gain = 0 dB, Power amp only) GSX3, GSX4		–20	—	20	mV
Comparator Input Voltage Range	G_{DB}	AVIN, REF1, REF2		0.85	—	V_{DD}–0.75	—
Analog Switch "ON" Resistance	R_{SW}	I01-I02, I03-I04, I05-I06, I07-I08, I09-I010, I010-I011, I012-V_{DD}, I013-V_{DD}, I014-V_{DD}		100	—	400	Ω

*1 –7.7 dBm (600 Ω) = 0 dBm0, + 3.17 dBm0 = 1.30 V_{PP} (μ-law Selected)

AC Chracteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)	Others				
Transmit Frequency Response	L_{OSS} T1	0 to 60	0	—	25	—	—	dB
	L_{OSS} T2	300 to 3000			–0.15	—	0.20	dB
	L_{OSS} T3	1020			Reference			dB
	L_{OSS} T4	3300			–0.15	—	0.80	dB
	L_{OSS} T5	3400			0	—	0.80	dB
	L_{OSS} T6	3968.75			13	—	—	dB
Receive Frequency Responce	L_{OSS} R1	0 to 3000	0	—	–0.15	—	0.20	dB
	L_{OSS} R2	1020			Reference			dB
	L_{OSS} R3	3300			–0.15	—	0.80	dB
	L_{OSS} R4	3400			0	—	0.80	dB
	L_{OSS} R5	3968.75			13	—	—	dB
Transmit Signal to Distortion Ratio	SD T1	1020	3	(*2)	35	—	—	dB
	SD T2		0		35	—	—	dB
	SD T3		–30		35	—	—	dB
	SD T4		–40		28	—	—	dB
	SD T5		–45		23	—	—	dB
Receive Signal to Distortion Ratio	SD R1	1020	3	(*2)	35	—	—	dB
	SD R2		0		35	—	—	dB
	SD R3		–30		35	—	—	dB
	SD R4		–40		28	—	—	dB
	SD R5		–45		23	—	—	dB
Transmit Gain Tracking	GT T1	1020	3	—	–0.2	—	0.2	dB
	GT T2		–10		Reference			dB
	GT T3		–40		–0.2	—	0.2	dB
	GT T4		–50		–0.5	—	0.5	dB
	GT T5		–55		–1.2	—	1.2	dB
Receive Gain Tracking	GT R1	1020	3	—	–0.2	—	0.2	dB
	GT R2		–10		Reference			dB
	GT R3		–40		–0.2	—	0.2	dB
	GT R4		–50		–0.5	—	0.5	dB
	GT R5		–55		–1.2	—	1.2	dB
Idle Channel Noise	N_{IDLT}	—	AIN = SG	(*2)	—	—	–68 (–75.7)	dBm0p (dBmp)
	N_{IDLR}	—	—	(*2) (*3)	—	—	–72 (–79.7)	
Absolute Signal Amplitude	A_{VT}	1020	0	GSX2	0.285	0.320 (*4)	0.359	Vrms
	A_{VR}			VFRO	0.285	0.320 (*4)	0.359	Vrms

AC Characteristics (Continued)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)	Others				
Power Supply Noise	P_{SRRT}	Noise Freq.	Noise Level	—	30	—	—	dB
Rejection Ratio	P_{SRRR}	: 0 to 50 kHz	: 50 mV_{PP}		30	—	—	dB
Digital Input/Output Setting Time	t_{SDX}	—	1LSTTL + 100 pF pull-up: 500 Ω	See Fig.4	0	—	200 *5(100)	ns
	t_{XD1}				0	—	200 *5(100)	ns
	t_{XD2}				0	—	200 *5(100)	ns
	t_{XD3}				0	—	200 *5(100)	ns
Serial Port Digital Input/Output Setting Time	t_{M1}	—	C_{Load} = 100 pF	See Fig.7	50	—	—	ns
	t_{M2}				50	—	—	ns
	t_{M3}				50	—	—	ns
	t_{M4}				50	—	—	ns
	t_{M5}				100	—	—	ns
	t_{M6}				50	—	—	ns
	t_{M7}				50	—	—	ns
	t_{M8}				0	—	50	ns
	t_{M9}				50	—	—	ns
	t_{M10}				50	—	—	ns
	t_{M11}				0	—	50	ns
Shift Clock Frequency	F_{EXCK}	—	—	EXCK	—	—	10	MHz

*2 Use the P-message weighted filter
*3 PCMRI input code "11010101"(A-law)
"11111111"(μ-law)
*4 0.320 Vrms = 0 dBm0 = –7.7 dBm
*5 Value in ( ) is for C_{Load} = 10 pF Pull-up ≤ 20 kΩ

Note: All ADPCM coder and decoder characteristics comply with ITU-T Recommendation G.721.

AC Characteristics (DTMF and Other Tones)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Frequency Difference	D_{FT1}	DTMF Tones		–7	—	+7	Hz
	D_{FT2}	Other Tones		–7	—	+7	Hz
Original (reference) Tone Signal Level *6	V_{TL}	Transmit Tones	DTMF (Low)	–18	–16	–14	dBm0
	V_{TH}		DTMF (High) and Other Tones	–16	–14	–12	dBm0
	V_{RL}	Receive Tones	DTMF (Low)	–4	–2	0	dBm0
	V_{RH}		DTMF (High) and Other Tones	–2	0	+2	dBm0
Relative Level of DTMF Tones	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		+1	+2	+3	dBm0

*6 Not contain the setting value of the programmable gain

AC Characteristics (Programmable Gain Stages)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Gain Accuracy	D_G	All gain stages, to programmed value	–1	0	+1	dB

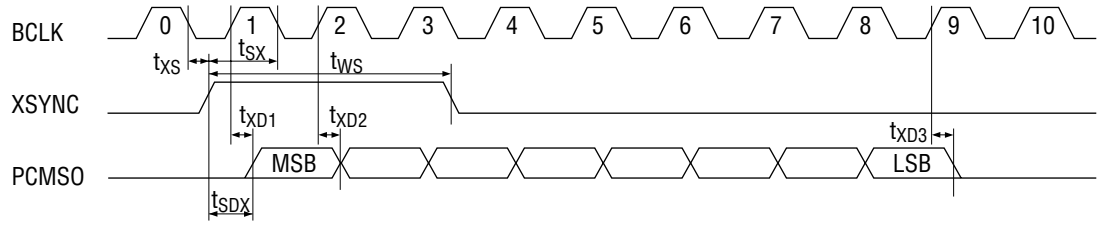
AC Characteristics (VOX Function)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Transmit VOX Detect Time	t_{VXON}	OFF → ON	VOXO, Fig.4	—	5	—	ms
(Voice signal ON/OFF detect time)	t_{VXOF}	ON → OFF		150/310	160/320	170/330	ms
Transmit VOX Detect Level Accuracy (Threshold Level)	D_{VX}	To the setting of detect level by CR6-B6, B5.		–2.5	0	+2.5	dB

TIMING DIAGRAM

Transmit Side PCM Data Interface



Receive Side PCM Data Interface

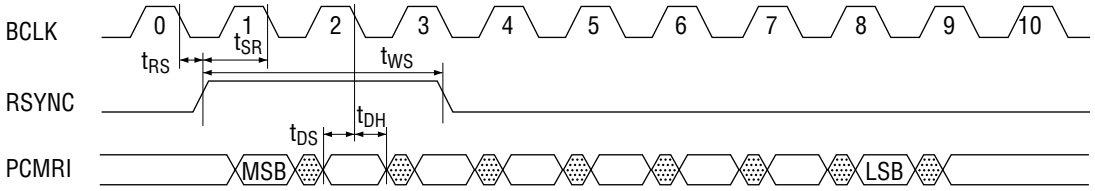


Figure 6 PCM Data Interface

Serial Port Data Transfer for MCU Interface

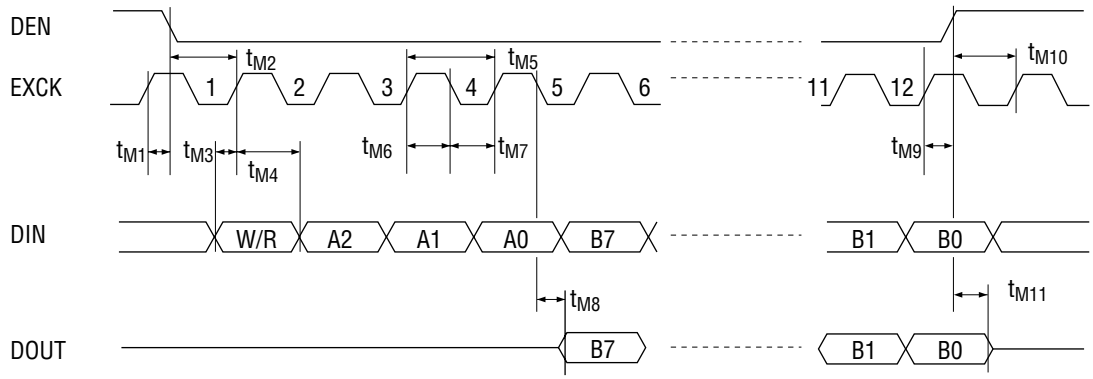


Figure 7 MCU Interface

FUNCTIONAL DESCRIPTION

Control Registers

(1) CR0 (Basic operating mode)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	A/μ SEL	MCK SEL	PDN ALL	PDN TX	PDN RX	—	LNR	PDN SAO/AOUT
Initial Value	0	0	0	0	0	0	0	0

Note) "Initial": Reset state by $\overline{\text{PDN/RESET}}$

B7 ...PCM Companding law select: 0/μ-law, 1/A-law
B6 ...Master clock frequency select: 0/9.600 MHz, 1/19.200 MHz
B5 ...Power down (whole system): 0/Power on, 1/Power down
When using this data for power down control, pin $\overline{\text{PDN/RESET}}$ should be set at "H"level. The control registers are not reset by this signal.
B4 ...Power down (Transmit only): 0/Power on, 1/Power down
B3 ...Power down (Receive only including the op-amps of GSX3, GSX4 and comparator): 0/Power on, 1/Power down
B2 ...Not used
B1 ...PCM interface linear code select:
0/Companding law selected by CR0-B7
1/14-bit Linear code (2's complement) in spite of the value of CR0-B7
B0 ...Power Down for Sounder output amps: (SAO), or Receiver output amp (AOUT, VFRO):
When this data is set to digital "1", the circut which is not selected by CR4-B5 are at the power down state.
When this data is set to digital "0", sounder amplifiers and receiver amplifiers are in the power-on state.

(2) CR1

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	TOUT3 –CONT	TOUT2 –CONT	TOUT1 –CONT	—	—	—	—	RX PAD
Initial Value	0	0	0	0	0	0	0	0

B7 ... TOUT3 control bit :
0/TOUT3 = "0", 1/Enable TOUT3
B6 ... TOUT2 control bit :
0/TOUT2 = "0", 1/Enable TOUT2
B5 ... TOUT1 control bit :
0/TOUT1 = "0", 1/Enable TOUT1
B4 ... Not used
B3 ... Not used
B2 ... Not used
B1 ... Not used
B0 ... Receive side PAD : 1/inserted,12 dB loss
0/no PAD

(3)CR2 (PCM CODEC operational mode setting and transmit/receive gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0
Initial Value	0	0	1	1	0	0	1	1

B7 ... PCM Coder disable : 0/Enable, 1/Disable (transmit PCM idle pattern)
B6, B5, B4 ... Transmit gain adjustment, refer to Table-2.
B3 ... PCM Decoder disable : 0/Enable, 1/Disable (receive PCM idle pattern)
B2, B1, B0 ... Receive gain setting, refer to Table-2.

Table-2 Transmit/Receive Gain Setting table

B6	B5	B4	Transmit Gain	B2	B1	B0	Receive Gain
0	0	0	–6 dB	0	0	0	–6 dB
0	0	1	–4 dB	0	0	1	–4 dB
0	1	0	–2 dB	0	1	0	–2 dB
0	1	1	0 dB	0	1	1	0 dB
1	0	0	+2 dB	1	0	0	+2 dB
1	0	1	+4 dB	1	0	1	+4 dB
1	1	0	+6 dB	1	1	0	+6 dB
1	1	1	+8 dB	1	1	1	+8 dB

This programmable gain table should be assigned, not only for transmit/receive voice signal, but also for the transmitted DTMF and other tones. The transmission of these tone signals are enabled, by the CR4-B6 data described later, The original (reference) signal amplitude of these tones are analogically defined as follows.

DTMF low-group-tones ..... –16 dBm0/Tone
DTMF high-group-tones and others ..... –14 dBm0/Tone

For example, when selecting +8 dB (B6, B5, B4) = (1,1,1) as a transmit gain, each tone signal amplitude with analogical expression on the pin PCMSO becomes as follows .

DTMF low-group tones ..... –8 dBm0
DTMF high-group tones and other tones ..... –6 dBm0

Gain setting of side tone (path to receive side from transmit side) and receive side tone is performed by register CR3.

(4) CR3 (Side tone and other tone generator gain setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Side. Tone GAIN2	Side. Tone GAIN1	Side. Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0
Initial Value	0	0	0	0	0	0	0	0

B7, B6, B5 ... Side tone path gain setting, refer to Table-3.
B4 ... Tone generator enable : 0/Disable, 1/Enable
B3, B2, B1, B0 ... Tone generator gain adjustment for receive side, refer to Table-4

Table-3 Side Tone Gain Setting Table

B7	B6	B5	Side Tone Path Gain
0	0	0	OFF
0	0	1	–21 dB
0	1	0	–19 dB
0	1	1	–17 dB
1	0	0	–15 dB
1	0	1	–13 dB
1	1	0	–11 dB
1	1	1	–9 dB

Table-4 Receive Tone Generator Gain Setting Table

B3	B2	B1	B0	Tone Generator Gain	B3	B2	B1	B0	Tone Generator Gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

The tone generator gain setting table for receive side, shown by Table-4, depends upon the following reference level.

DTMF low-group tones ..... –2 dBm0
DTMF high-group tones and others 0 dBm0

For example, when selecting –6 dB (B3, B2, B1, B0) = (1, 1, 1, 1) as a tone generator gain, each DTMF tone signal amplitude on SAO or VFRO is as follows.

DTMF low-group tone ..... –8 dBm0
DTMF high-group tone or other tones ..... –6 dBm0

(5) CR4 (Tone genereator operating mode and frequency setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	DTMF/OTHERS SEL	TONE SEND	SAO/ VFRO	TONE4	TONE3	TONE2	TONE1	TONE0
Initial Value	0	0	0	0	0	0	0	0

B7 ... DTMF or Other tones select : 0/Others, 1/DTMF
B6 ... Tone transmit enable (Transmit side) : 0/Voice signal (transmit), 1/Tone transmit
B5 ... Tone output pin select (Receive side) : 0/VFRO, 1/SAO
B4, B3, B2, B1, B0 ... Tone frequency setting, referred to Table-5-1, -2.

(a) B7 = 1 (DTMF tone)

Table-5-1

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
*	0	0	0	0	697 Hz + 1209 Hz	*	1	0	0	0	852 Hz + 1209 Hz
*	0	0	0	1	697 Hz + 1336 Hz	*	1	0	0	1	852 Hz + 1336 Hz
*	0	0	1	0	697 Hz + 1477 Hz	*	1	0	1	0	852 Hz + 1477 Hz
*	0	0	1	1	697 Hz + 1633 Hz	*	1	0	1	1	852 Hz + 1633 Hz
*	0	1	0	0	770 Hz + 1209 Hz	*	1	1	0	0	941 Hz + 1209 Hz
*	0	1	0	1	770 Hz + 1336 Hz	*	1	1	0	1	941 Hz + 1336 Hz
*	0	1	1	0	770 Hz + 1477 Hz	*	1	1	1	0	941 Hz + 1477 Hz
*	0	1	1	1	770 Hz + 1633 Hz	*	1	1	1	1	941 Hz + 1633 Hz

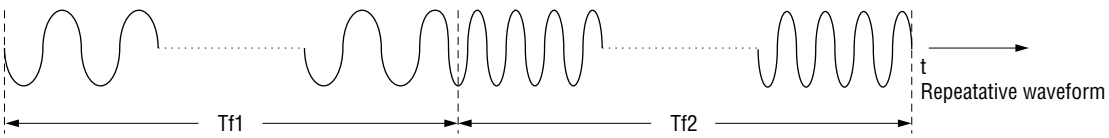
*Unrelated

(b) B7 = 0 (Other tones)

Table-5-2 Tone Generator Frequency Setting

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
0	0	0	0	0	2 k/2.48 kHz, 8 Hz wamble	1	0	0	0	0	2000 Hz
0	0	0	0	1	2 k/2.2 kHz, 8 Hz wamble	1	0	0	0	1	2042 Hz
0	0	0	1	0	2 k/2.48 kHz, 4 Hz wamble	1	0	0	1	0	2514 Hz
0	0	0	1	1	2 k/2.2 kHz, 4 Hz wamble	1	0	0	1	1	500 Hz
0	0	1	0	0	1 k/1.333 kHz, 8 Hz wamble	1	0	1	0	0	667 Hz
0	0	1	0	1	2.73 k/2.5 kHz, 8 Hz wamble	1	0	1	0	1	1333 Hz
0	0	1	1	0	1.8 k/2 kHz, 8 Hz wamble	1	0	1	1	0	2100 Hz
0	0	1	1	1	400 Hz,16 Hz wamble	1	0	1	1	1	—
0	1	0	0	0	400 Hz,20 Hz wamble	1	1	0	0	0	—
0	1	0	0	1	400 Hz	1	1	0	0	1	—
0	1	0	1	0	350 Hz + 440 Hz Mix	1	1	0	1	0	—
0	1	0	1	1	1.5kHz	1	1	0	1	1	—
0	1	1	0	0	1.8kHz	1	1	1	0	0	—
0	1	1	0	1	800 Hz	1	1	1	0	1	—
0	1	1	1	0	1000 Hz	1	1	1	1	0	—
0	1	1	1	1	1300 Hz	1	1	1	1	1	—

Wamble Tone Wave



4Hz wamble... Tf1 = Tf2 = 125 ms
8Hz wamble... Tf1 = Tf2 = 62.5 ms
16Hz wamble...Tf1 = Tf2 = 31.25 ms
20Hz wamble...Tf1 = Tf2 = 25 ms

(6) CR5 (Analog switch control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	SW7_ CONT	SW8_ CONT	SW9_ CONT	SW5&SW6_ CONT	SW4_ CONT	SW3_ CONT	SW2_ CONT	SW1_ CONT
Initial Value	0	0	0	0	0	0	0	0

B7 ... Control Analog switch SW7 between IO12 and V_{DD} :
0/SW7 OFF, 1/SW7 ON
B6 ... Control Analog switch SW8 between IO13 and V_{DD} :
0/SW8 OFF, 1/SW8 ON
B5 ... Control Analog switch SW9 between IO14 and V_{DD} :
0/SW9 OFF, 1/SW9 ON
B4 ... Control Analog switch SW5 between IO9 and IO10, and Analog switch SW6 between IO10 and IO11 :
0/SW5 OFF, SW6 ON, 1/SW5 ON, SW6 OFF
B3 ... Control Analog switch SW4 between IO7 and IO8 :
0/SW4 OFF, 1/SW4 ON
B2 ... Control Analog switch SW3 between IO5 and IO6 :
0/SW3 OFF, 1/SW3 ON
B1 ... Control Analog switch SW2 between IO3 and IO4 :
0/SW2 OFF, 1/SW2 ON
B0 ... Control Analog switch SW1 between IO1 and IO2 :
0/SW1 OFF, 1/SW1 ON

(7) CR6 (VOX function control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LEVEL SEL	RX NOISE LVL1	RX NOISE LVL0
Initial Value	0	0	0	0	0	0	0	0

B7 ... VOX function enable : 0/Disable, 1/Enable
B6, B5 ... Transmit signal energy detect (Transmit VOX) threshold
(0, 0): –30 dBm0
(0, 1): –35 dBm0
(1, 0): –40 dBm0
(1, 1): –45 dBm0
B4 ... Hang-over time (Fig. 2, $T_{VXOFF)}$: 0/160 ms, 1/320 ms
B3 ... Receive VOX function setting : 0/Background noise transmit, 1/Voice signal detect
When using this data for control, the pin VOXI should be set at a "L" level.
B2 ... Background noise amplitude setting : 0/Automatic, 1/Programmable by B1 and B0
Automatic : The noise is set at the voice signal amplitude at the time when B3 (or VOXI) changes from "1" to digital "0".
B1, B0 ... (0, 0): No noise
(0, 1): –55 dBm0
(1, 0): –45 dBm0
(1, 1): –35 dBm0

(8) CR7 (Detect register, read only)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	VOX OUT	TX NOISE LVL1	TX NOISE LVL0	—	—	—	—	—
Initial	0	0	0	*	*	*	*	*

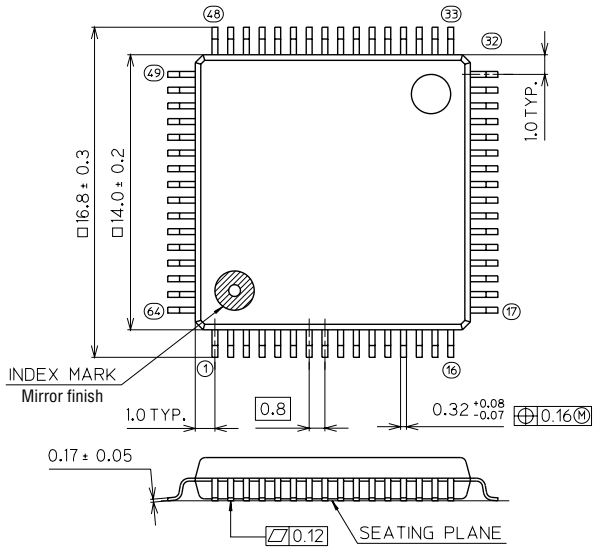
* For IC test

B7 ... Transmit VOX function result : 0/Absence, 1/Presence
B6, B5 ... Transmit voiceless level (indicator) :
(0, 0) : below –60 dBm0
(0, 1) : –50 to –60 dBm0
(1, 0) : –40 to –50 dBm0
(1, 1) : over –40 dBm0
Note) These outputs are valid only when VOX function is enabled by CR6-B7.
B4 ... Not used
B3 ... Not used
B2 ... Not used
B1 ... Not used
B0 ... Not used

PACKAGE DIMENSIONS

(Unit : mm)

QFP64-P-1414-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.87 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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