MH1M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 37748736-BIT (1048576-WORD BY 36-BIT) DYNAMIC RAM

DESCRIPTION

The MH1M365CXJ/CNXJ is 1048576-word x 36-bits dynamic RAM. This consists of two industry standard 1M x 16 dynamic RAMs in SOJ and one industry 1M x 4 dyanmic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required. This is a socket-type memory module,suitable for easy interchange or addition of modules.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
MH1M365CXJ/CNXJ-5	50	13	25	90	2120
MH1M365CXJ/CNXJ-6	60	15	30	110	1750
MH1M365CXJ/CNXJ-7	70	20	35	130	1520

- **72pin single in-line package**
- **Single 5.0V ± 10% supply**
- **Low stand-by power dissipation**
  16.5mW (Max) ---------- **CMOS Input level**
- **Low operating power dissipation**
  MH1M365CXJ/CNXJ- 5 ---------- **2.67W (Max)**
  MH1M365CXJ/CNXJ- 6 ---------- **2.20W (Max)**
  MH1M365CXJ/CNXJ- 7 ---------- **1.90W (Max)**

- **Hyper-page mode , $\overline{RAS}$-only refresh , $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities**
- **All inputs and output directly TTL compatible**
  1024 refresh cycles every 16.4ms (A_0 ~ A_9)

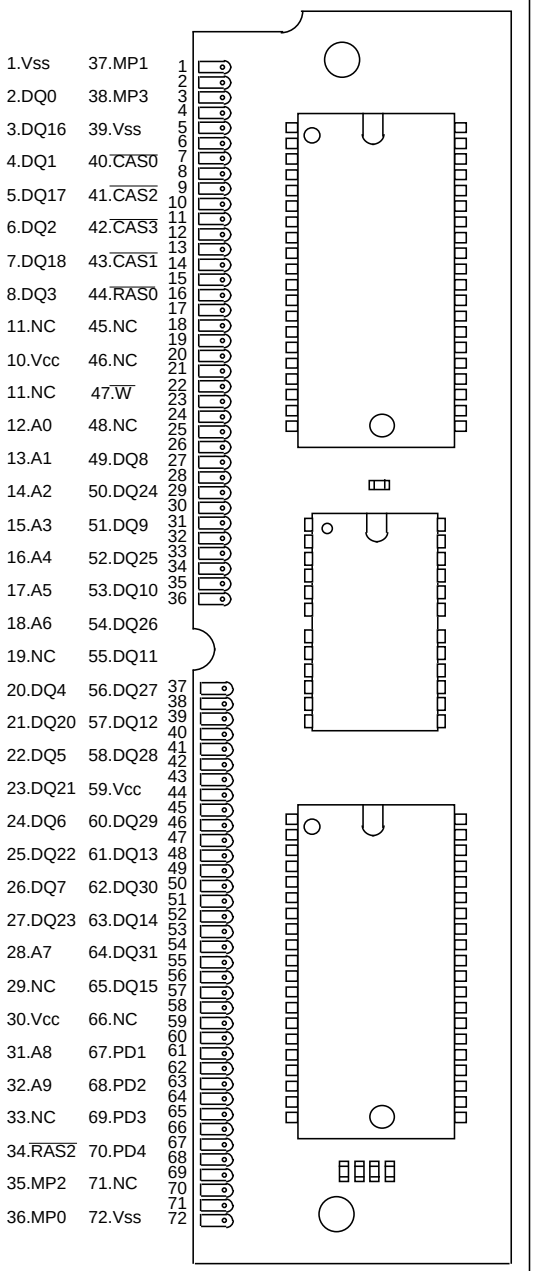
- **MH1M365CXJ** ---------- **Gold plating**
- **MH1M365CNXJ** ---------- **Nickel+solder plating**

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)

[Single side]



Outline 72N9K-C

	- 5	- 6	- 7
PD1	Vss	Vss	Vss
PD2	Vss	Vss	Vss
PD3	Vss	NC	Vss
PD4	Vss	NC	NC

NC: NO CONNECTION

FUNCTION

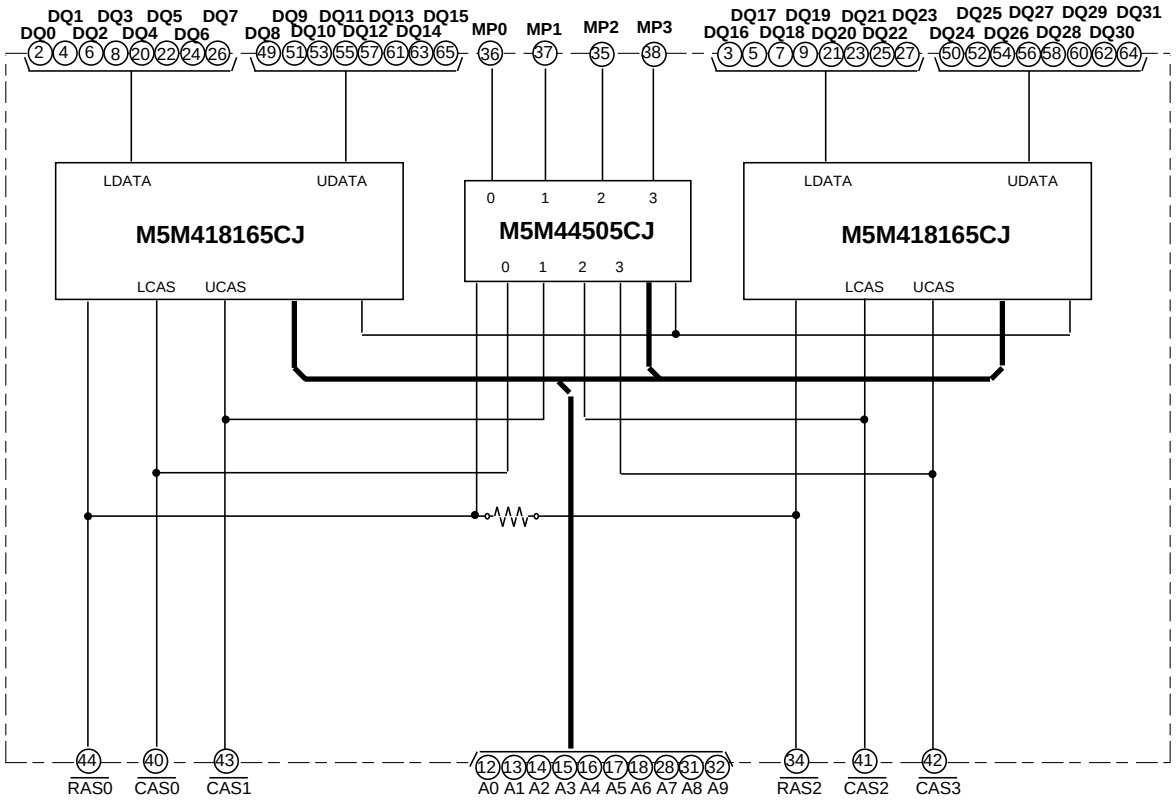
in addition to normal read, write, a number of other functions, e.g., hyper page mode, $\overline{RAS}$ only refresh, The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Row address	Column address	Input	Output
Read	ACT	ACT	NAC	APD	APD	OPN	VLD
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN
$\overline{RAS}$-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN
Hidden refresh	ACT	ACT	NAC	APD	DNC	OPN	VLD
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1 ~ 7	V
V I	Input voltage		-1 ~ 7	V
V0	Output voltage		-1 ~ 7	V
I 0	Output current		50	mA
Pd	Power dissipation	Ta=25°C	3000	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70 °C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≤ V_{OUT} ≤ 5.5V	-10		10	µA
I_I	Input current		0V ≤ V_{IN} ≤ 6 V, Other inputs pins=0V	-30		30	µA
$I_{CC1\ (AV)}$	Average supply current from Vcc operating (Note 3,4,5)	MH1M365C -5	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			485	mA
		MH1M365C -6				400	
		MH1M365C -7				345	
I_{CC2}	Supply current from Vcc , stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			6	mA
			$\overline{RAS}$= $\overline{CAS}$ ≥ Vcc - 0.2 V			3	
$I_{CC3\ (AV)}$	Average supply current from Vcc refreshing (Note 3,5)	MH1M365C -5	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			485	mA
		MH1M365C -6				400	
		MH1M365C -7				345	
$I_{CC4(AV)}$	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	MH1M365C -5	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			455	mA
		MH1M365C -6				360	
		MH1M365C -7				305	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	MH1M365C -5	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			465	mA
		MH1M365C -6				385	
		MH1M365C -7				335	

Note 2: Current flowing into an IC is positive, out is negative.

3: Icc1 (AV), Icc3 (AV) and Icc4 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS=V_{IL} and $\overline{CAS}$=V_{IH} .

CAPACITANCE (Ta=0 ~ 70 °C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I\ (A)}$	Input capacitance,address inputs	V_I=Vss f=1MHz Vi=25mVrms			30	pF
$C_{I\ (\overline{W})}$	Input capacitance, write control input				36	pF
$C_{I\ (\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				36	pF
$C_{I\ (\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				29	pF
$C_{I\ /\ O}$	Input/Output capacitance, data ports				22	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70 °C, Vcc = 5V ± 10%, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter	Limits						Unit
		MH1M365C -5		MH1M365C -6		MH1M365C -7		
		Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$ (Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 7,9)		50		60		70	ns
t_{AA}	Column address access time (Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (Note 7,11)		30		35		40	ns
t_{OHC}	Output hold time from $\overline{CAS}$	5		5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$ (Note 13)	5		5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low (Note 7)	5		5		5		ns
t_{WEZ}	Output disable time after $\overline{WE}$ high (Note 12)		13		15		20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note 12,13)		13		15		20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high (Note 12,13)		13		15		20	ns

Note 6: An initial pause of 500µs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-5mA) / VOL=0.4V(IOL=-4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq$ I ± 10 µA I) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc = 5V ± 10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		MH1M365C -5		MH1M365C -6		MH1M365C -7		
		Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time		16.4		16.4		16.4	ms
t_{RP}	$\overline{RAS}$ high pulse width	30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note16)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	8		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note17)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note18)	0	10	0	13	0	13	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	8		10		10		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low (Note19)	0		0		0		ns
t_{RDD}	Delay time, RAS high to data (Note20)	13		15		20		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data (Note20)	13		15		20		ns
t_T	Transition time (Note21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed t_T =3ns.

15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

16: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.

17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \leq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

18: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

19: t_{DZC} must be satisfied.

20: Either t_{RDD} or t_{CDD} or t_{ODD} must be satisfied.

21: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		MH1M365C -5		MH1M365C -6		MH1M365C -7		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	8	10000	10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	40		48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 22)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 22)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	25		30		35		ns
t_{CAL}	Column address to $\overline{CAS}$ hold time	13		18		23		ns

Note 22: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write)

Symbol	Parameter	Limits						Unit
		MH1M365C -5		MH1M365C -6		MH1M365C -7		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	8	10000	10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	40		48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	8		10		13		ns
t_{WP}	Write pulse width	8		10		13		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		13		ns

Hyper page Mode Cycle (Read, Early Write, Hi-Z control by $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		MH1M365C -5		MH1M365C -6		MH1M365C -7		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time	20		25		30		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low	5		5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note24)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note25)	8	13	10	16	13	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until CAS access	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

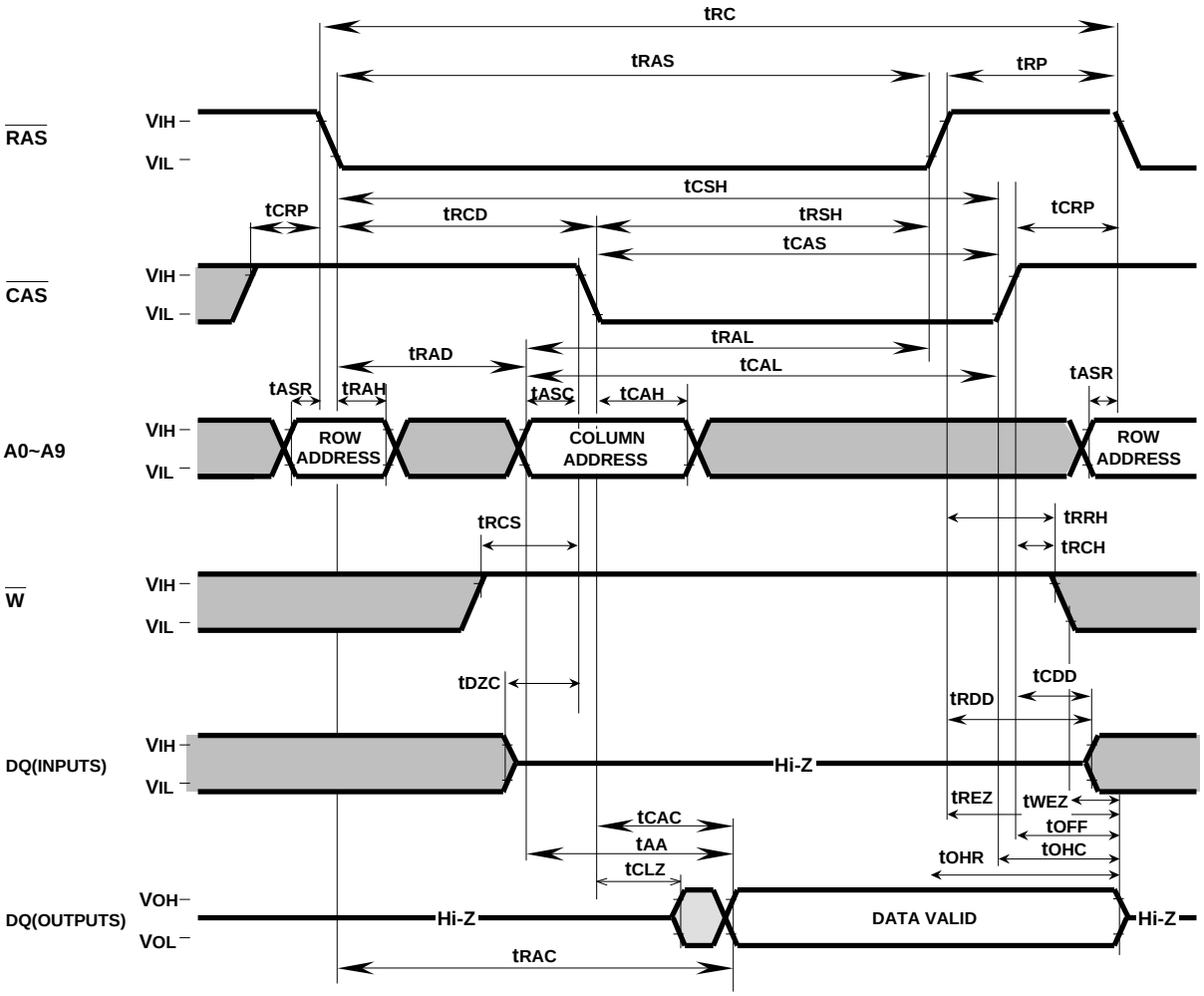
25: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		MH1M365C -5		MH1M365C -6		MH1M365C -7		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 27)
Read Cycle

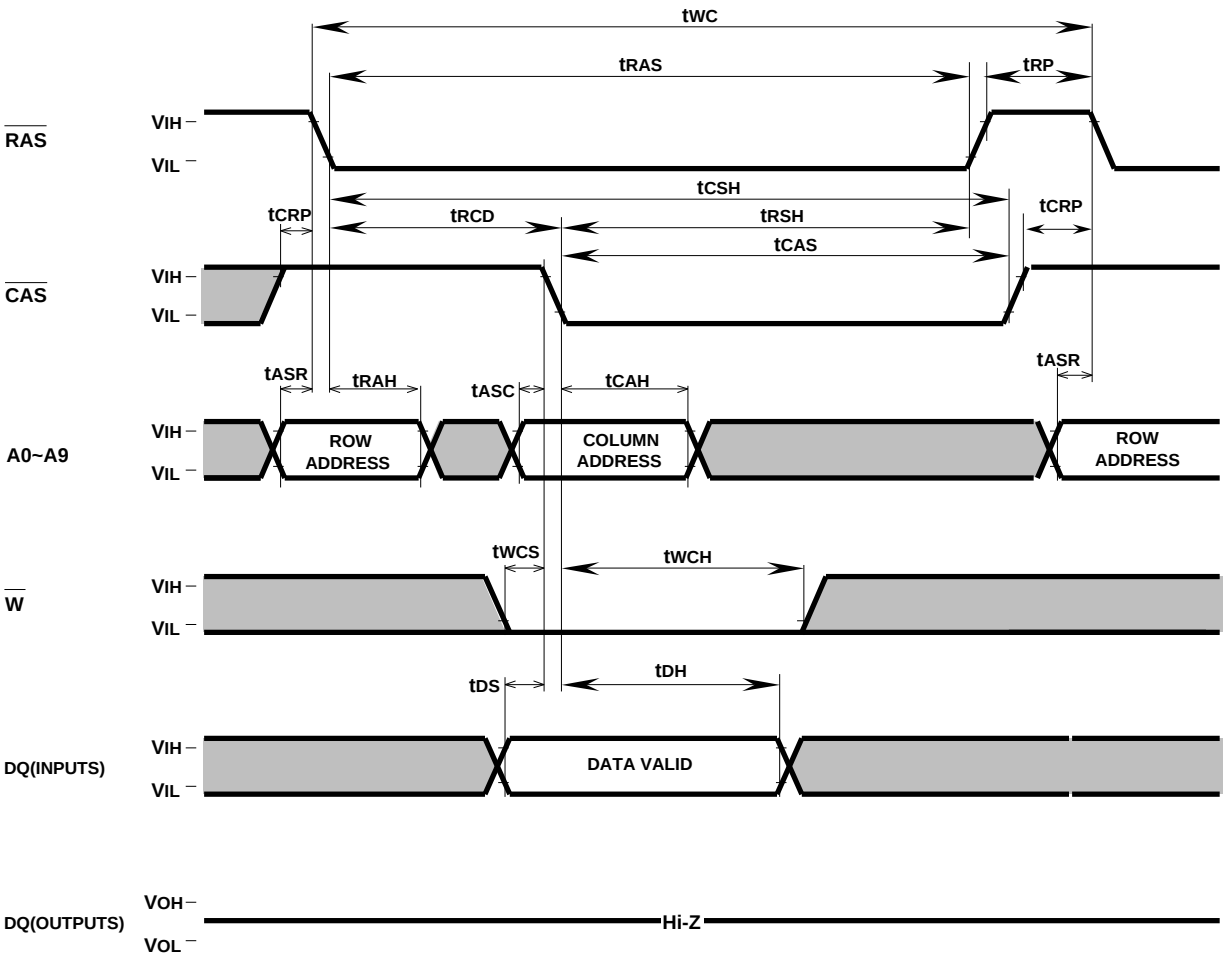


Note 27

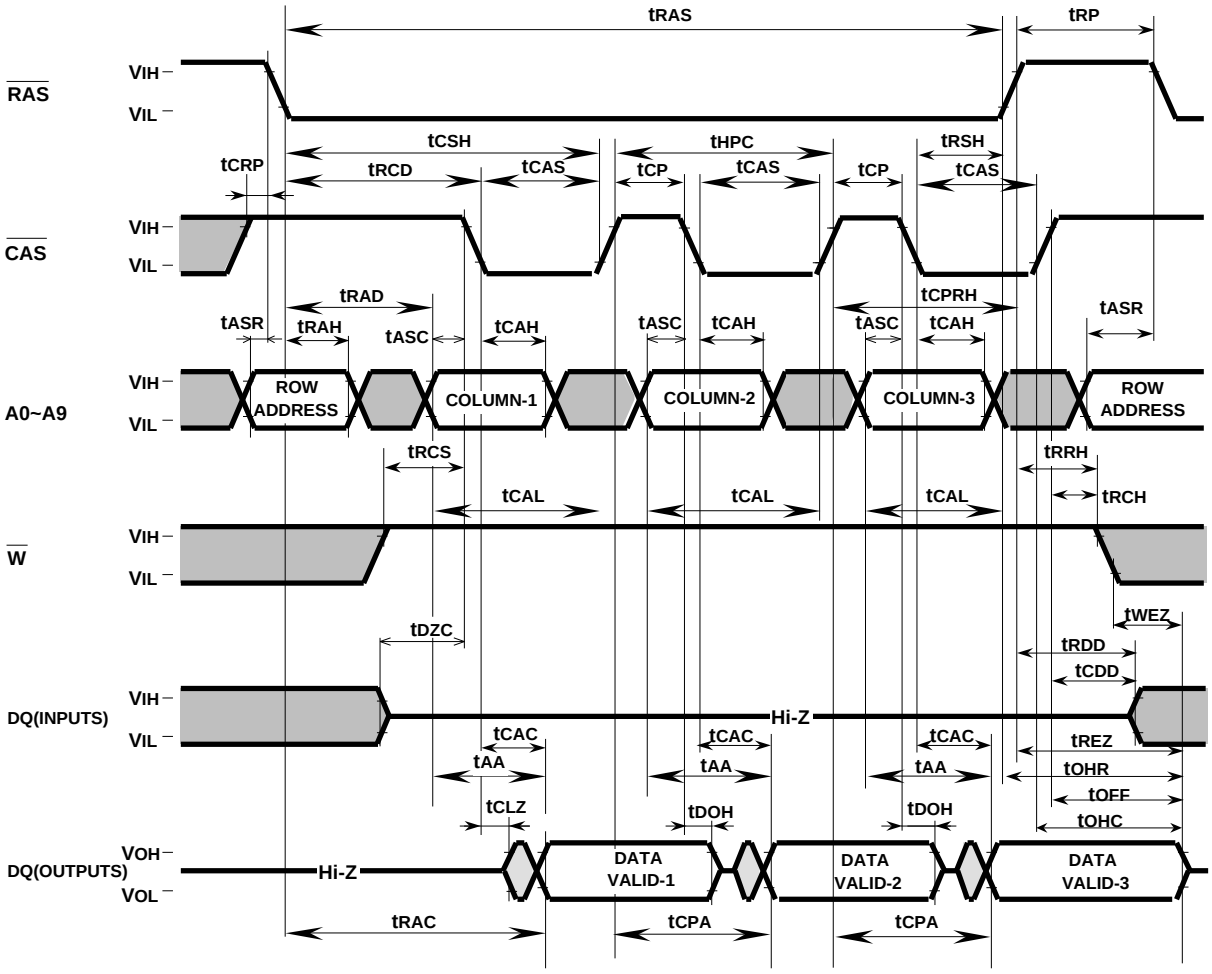
Indicates the don't care input.
VIH(min) ≤ VIN ≤ VIH(max) or
VIL(min) ≤ VIN ≤ VIL(max)

Indicates the invalid output.

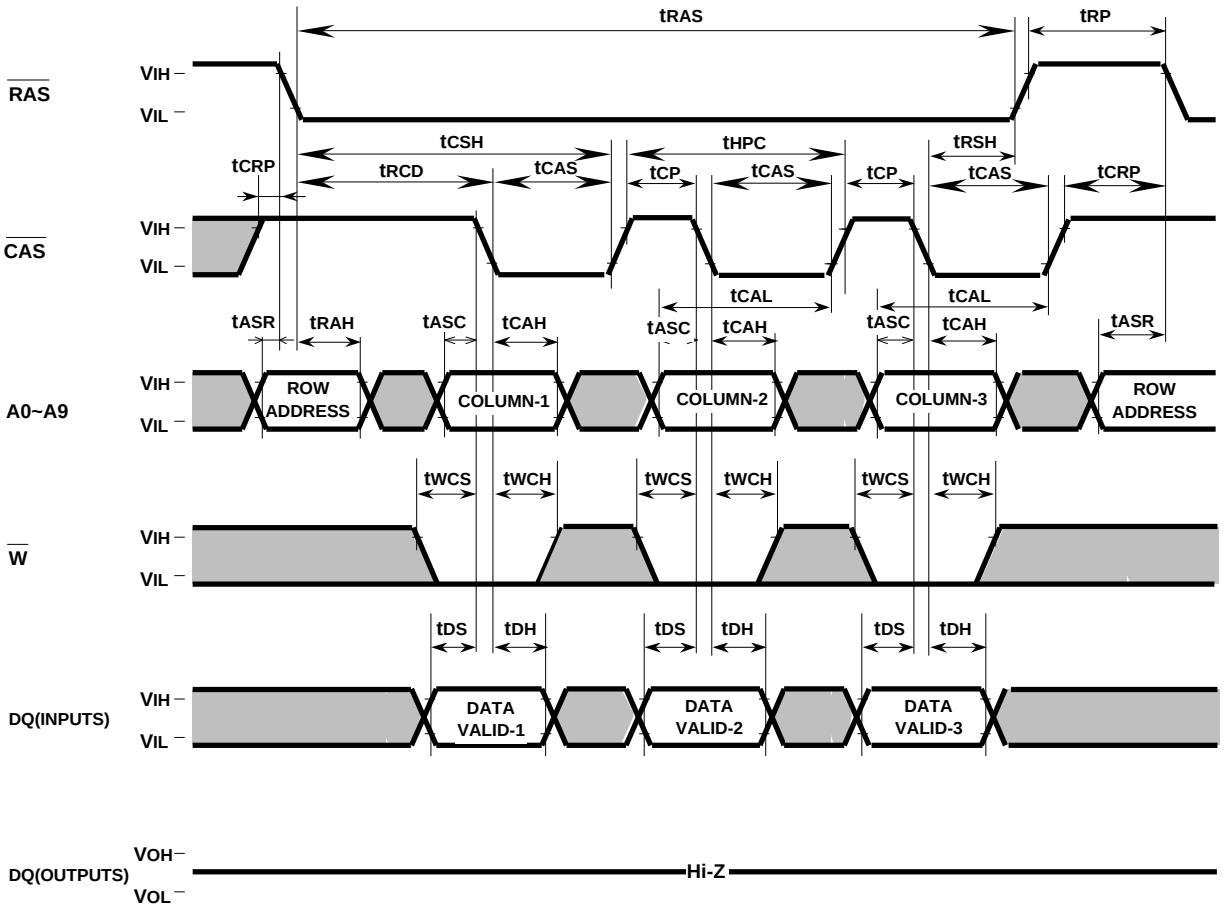
Early Write Cycle



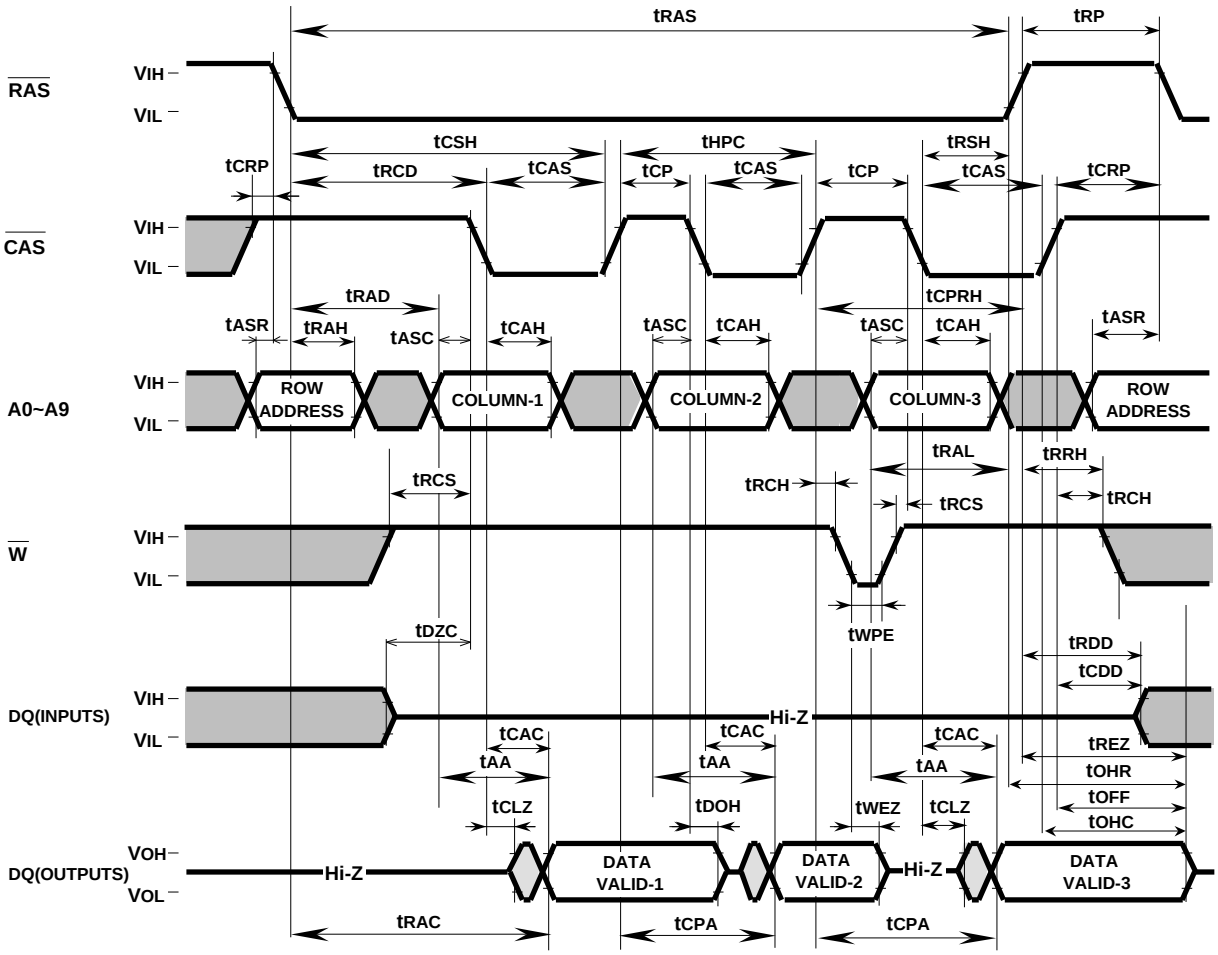
Hyper Page Mode Read Cycle



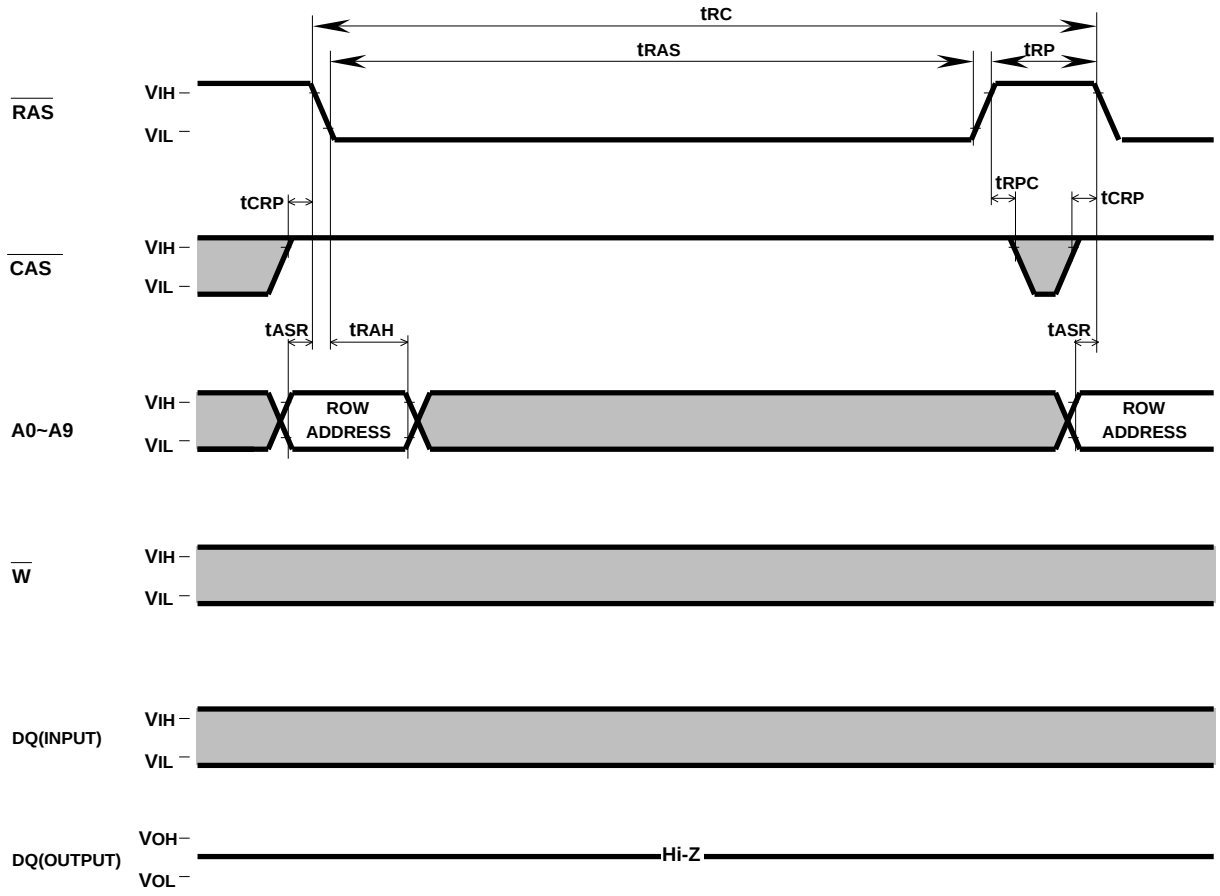
Hyper Page Mode Early Write Cycle



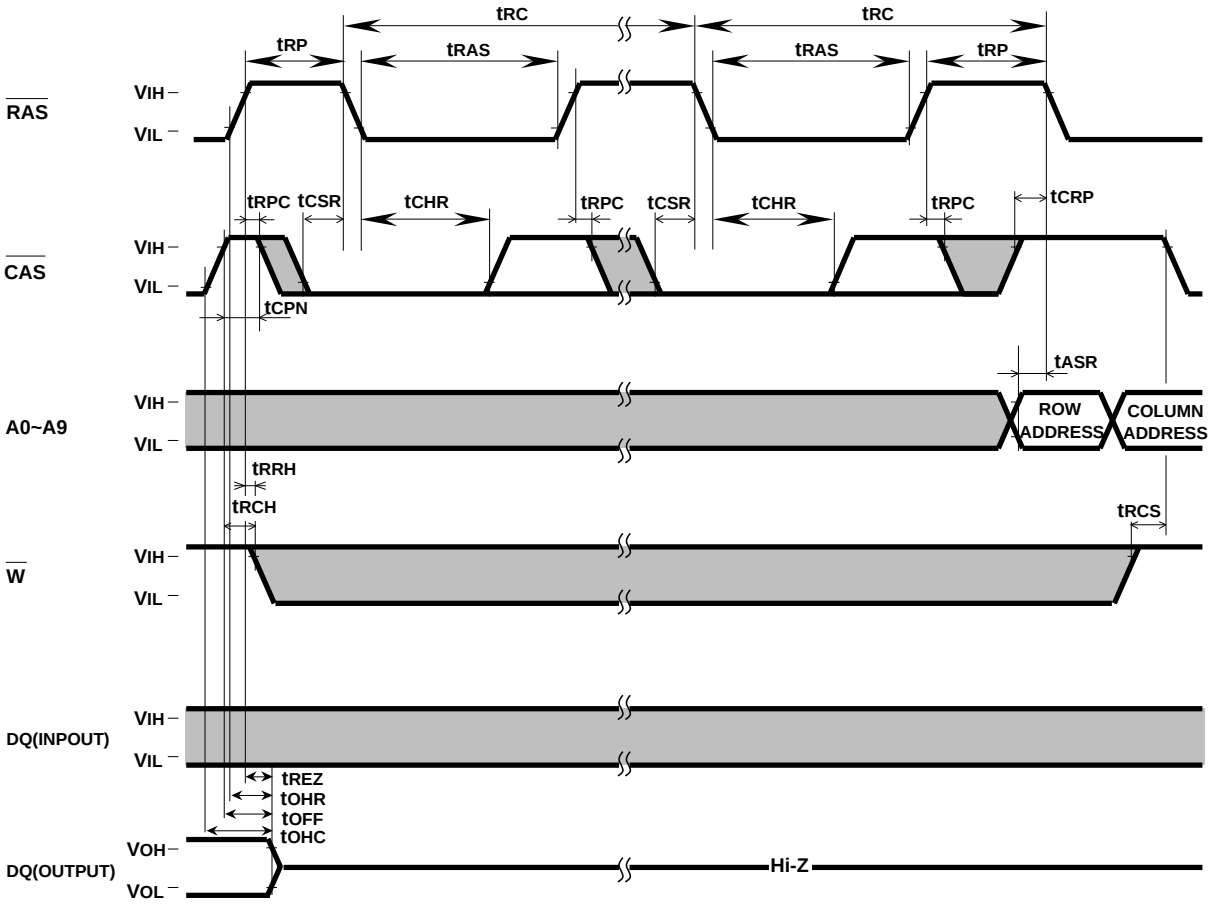
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



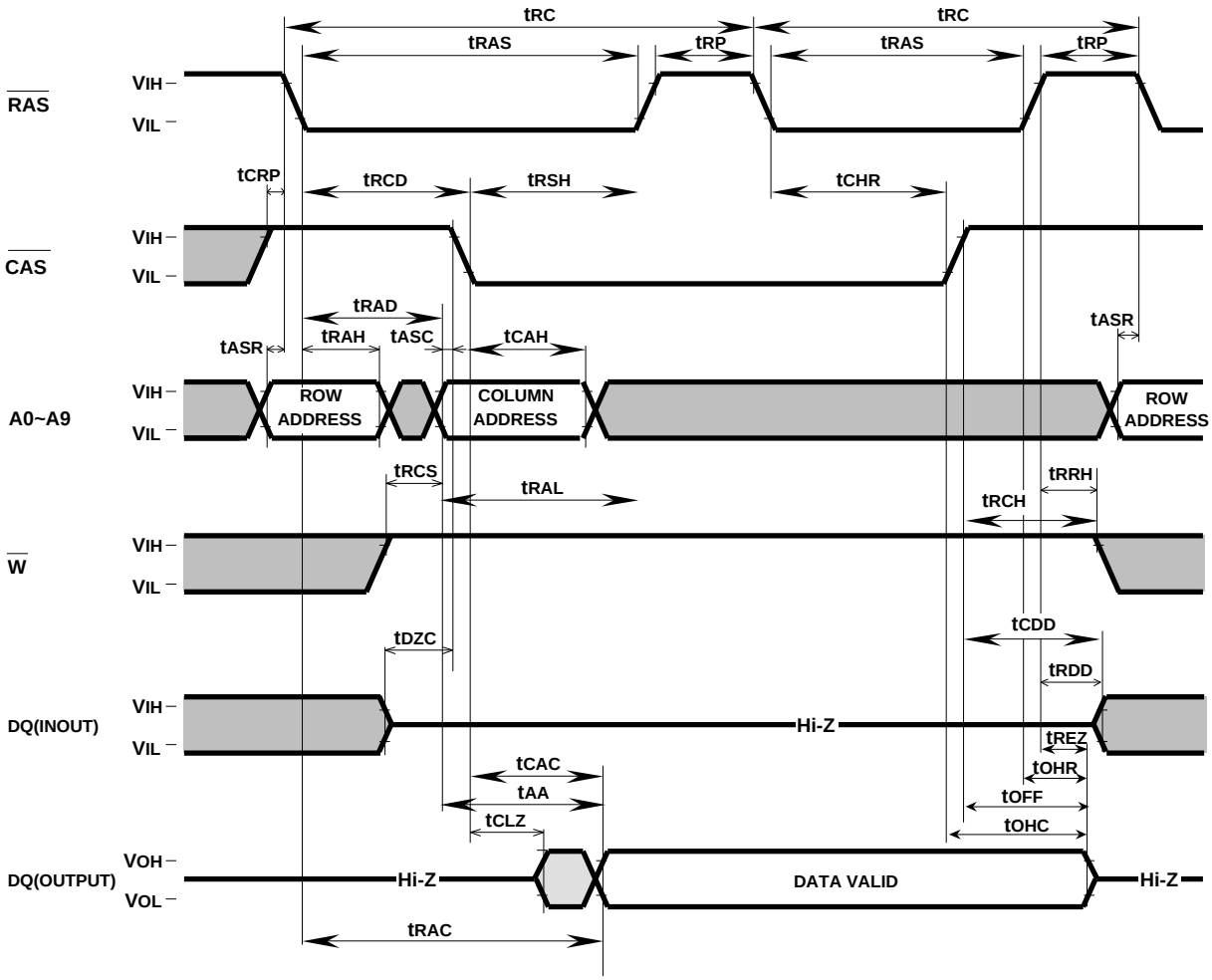
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Hidden Refresh Cycle (Read) **(Note 28)**



Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

72pin DRAM Module Outline