MF1 IC S20 05

Sawn bumped 120µm wafer addendum

1. General description

The MF1 IC S20 05 is a contactless Smart Card IC designed for card IC coils following the "Mifare card IC coil design guide" and is qualified to work properly in NXP´ reader environment, which is built according to NXP´ specification.

This specification describes electrical, physical and dimensional properties of wafers.

2. Ordering information

Table 1.   Ordering information

Type number	Package		
	Name	**Description**	**Ordering Code**
MF1ICS2005W/U7D		**Die on sawn wafer**	9352 851 56005

3. Mechanical specification

3.1 Wafer

- Diameter: 8"
- Thickness: 120 μm $\pm$ 15 μm
- Flatness: not applicable
- PGDW: 24892

3.2 Wafer backside

- Material: Si
- Treatment: ground and stress relieve

3.3 Chip dimensions

- Chip size: 1.11 x 1.06 mm
- Scribe lines: x-line: 80 μm
                           y-line: 80 μm

3.4 Passivation

- Type: sandwich structure
- Material: PSG / Nitride

- Thickness: 500 nm / 600 nm

3.5 Au bump

- Bump material: > 99.9% pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 μm
- Bump height uniformity:
  - within a die: ± 2 μm
  - within a wafer: ± 3 μm
  - wafer to wafer: ± 4 μm
- Bump flatness: ± 1.5 μm
- Bump size:
  - LA, LB, VSS[1]   104 x 104 μm
  - TESTIO[1]   89 x 104 μm
- Bump size variation: ± 5 μm
- Under bump metallization: sputtered TiW

Remark: Substrate is connected to VSS.

3.6 Fail die identification

Electronic wafer mapping covers the electrical test results and additionally the results of mechanical/ visual inspection.

No inkdots are applied.

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1. Pads VSS and TESTIO are disconnected when wafer is sawn.

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4. Limiting values

Table 2. Limiting values [1][2][3]

In accordance with the Absolute Maximum Rating System (IEC 134)

Symbol	Parameter		Min	Max	Unit
I_{IN}	Input Current		-	30	mA
P_{TOT}	Total power dissipation per package		-	200	mW
T_{STOR}	Storage temperature		-55	125	°C
T_{OP}	Operating temperature		-25	70	°C
V_{ESD}	Electrostatic discharge voltage	[4]	2	-	kV
I_{LU}	Latch-up current		± 100		mA

[1] Stresses above one or more of the limiting values may cause permanent damage to the device

[2] These are stress ratings only. Operation of the device at these or any other conditions above those given in the Characteristics section of the specification is not implied

[3] Exposure to limiting values for extended periods may affect device reliability
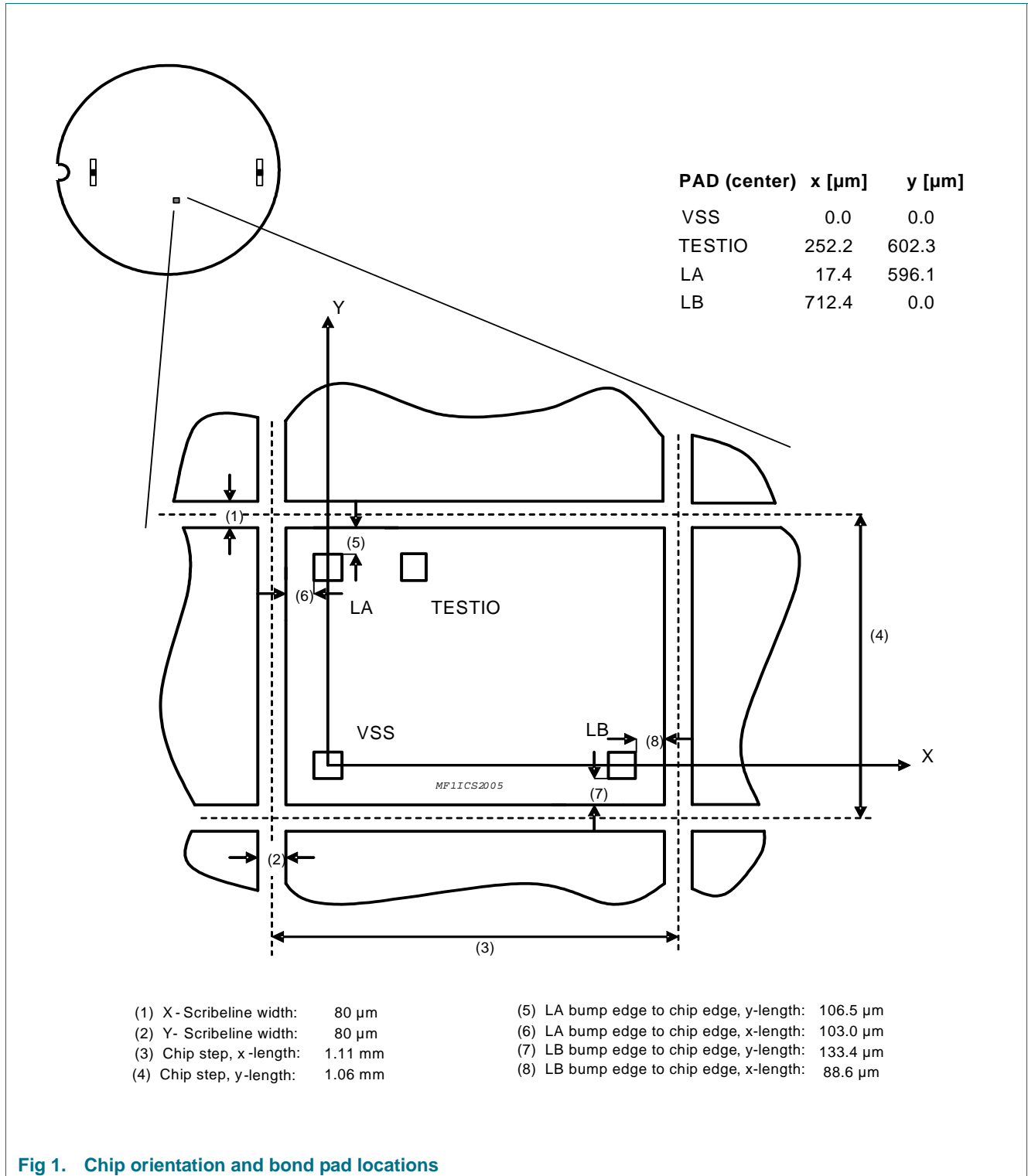
[4] MIL Standard 883-C method 3015; Human body model: C = 100 pF, R = 1.5 kW

5. Characteristics

Table 3. Electrical characteristics [1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IN}	Input frequency		-	13.56	-	MHz
C_{IN}	Input capacitance (LCR meter HP4258)	22 °C, Cp-D, 13.56 MHz, 2 V	14.4	16.1	17.4	pF
t_W	EEPROM write time		-	2.9	-	ms
t_{RET}	EEPROM data retention		10			years
N_{WE}	EEPROM write endurance		10^5			cycles

[1] Stresses above one or more of the limiting values may cause permanent damage to the device

[2] These are stress ratings only. Operation of the device at these or any other conditions above those given in the Characteristics section of the specification is not implied

[3] Exposure to limiting values for extended periods may affect device reliability

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6. Chip orientation and bond pad locations

PAD (center)	x [μm]	y [μm]
VSS	0.0	0.0
TESTIO	252.2	602.3
LA	17.4	596.1
LB	712.4	0.0

(1) X - Scribeline width: 80 μm
(2) Y - Scribeline width: 80 μm
(3) Chip step, x -length: 1.11 mm
(4) Chip step, y -length: 1.06 mm

(5) LA bump edge to chip edge, y-length: 106.5 μm
(6) LA bump edge to chip edge, x-length: 103.0 μm
(7) LB bump edge to chip edge, y-length: 133.4 μm
(8) LB bump edge to chip edge, x-length: 88.6 μm

Fig 1.   Chip orientation and bond pad locations

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7. References

- Data sheet "General wafer specification for 8" wafers"
- Data sheet "Standard card IC MF1 IC S50 memory contents after test"
- Data sheet "Standard card IC MF1 IC S50 functional Specification"
- Product qualification package "Standard card IC MF1 IC S50 05"
- Application note "Mifare, card IC coil design guide"

8. Revision history

Table 4.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
141130	July 2007	Product data sheet		
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.			
	• Legal texts have been adapted to the new company name.			

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9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1]   Please consult the most recently issued document before initiating or completing a design.

[2]   The term 'short data sheet' is explained in section "Definitions".

[3]   The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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For sales office addresses, send an email to: **salesaddresses@nxp.com**

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