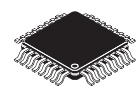
MC100ES7111

Preliminary Information

Low Voltage 1:10 Differential LVDS Clock Fanout Buffer

LOW–VOLTAGE 1:10 DIFFERENTIAL LVDS CLOCK FANOUT DRIVER



FA SUFFIX
32–LEAD LQFP PACKAGE
CASE 873A

The Motorola MC100ES7111 is a LVDS differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES7111 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

Features:

- 1:10 differential clock fanout buffer
- 50 ps maximum device skew[1]
- SiGe technology
- Supports DC to 1000 MHz operation[1] of clock or data signals
- LVDS compatible differential clock outputs
- PECL and HSTL/LVDS compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 32 lead LQFP package

Functional Description

The MC100ES7111 is designed for low skew clock distribution systems and supports clock frequencies up to 1000 MHz[1]. The device accepts two clock sources. The CLK0 input accepts LVDS or HSTL compatible signals and CLK1 accepts PECL compatible signals. The selected input signal is distributed to 10 identical, differential LVDS compatible outputs.

The output enable control is synchronized internally preventing output runt pulse generation. Outputs are only disabled or enabled when the outputs are already in logic low state (true outputs logic low, inverted outputs logic high). The internal synchronizer eliminates the setup and hold time requirements for the external clock enable signal. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

1. AC specifications are design targets and subject to change

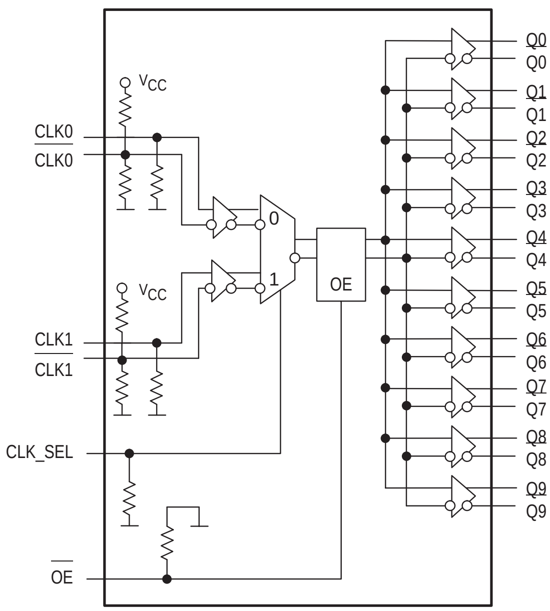


Figure 1. MC100ES7111 Logic Diagram

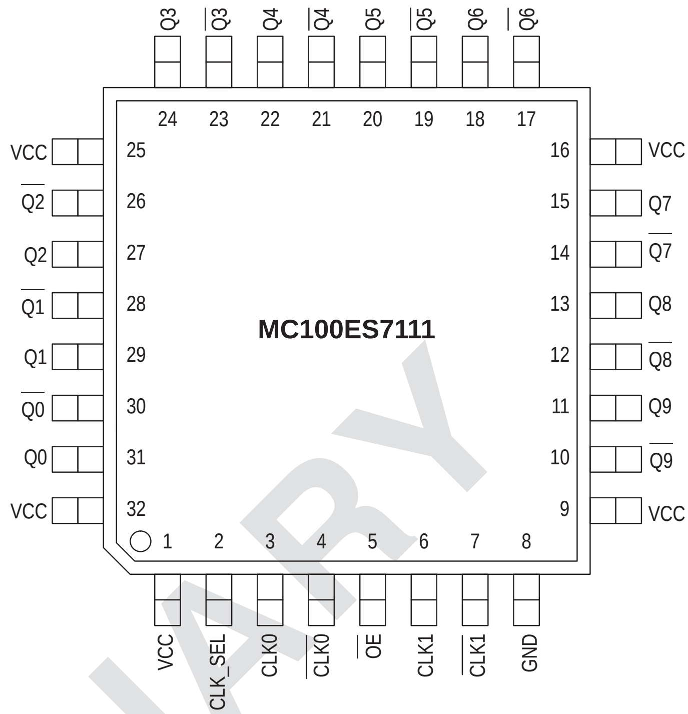


Figure 2. 32–Lead Package Pinout (Top View)

Table 1. PIN CONFIGURATION

Pin	I/O	Type	Function
CLK0, $\overline{CLK0}$	Input	HSTL/LVDS	Differential HSTL or LVDS reference clock signal input
CLK1, $\overline{CLK1}$	Input	PECL	Differential PECL reference clock signal input
CLK_SEL	Input	LVCMOS	Reference clock input select
OE	Input	LVCMOS	Output enable/disable. OE is synchronous to the input reference clock which eliminates possible output runt pulses when the OE state is changed.
Q[0–9], $\overline{Q[0–9]}$	Output	LVDS	Differential clock outputs
GND	Supply		Negative power supply
V_{CC}	Supply		Positive power supply of the device (3.3V)

Table 2. FUNCTION TABLE

Control	Default	0	1
CLK_SEL	0	CLK0, $\overline{CLK0}$ (HSTL/LVDS) is the active differential clock input	CLK1, $\overline{CLK1}$ (PECL) is the active differential clock input
$\overline{OE}$	0	Q[0-9], $\overline{Q[0-9]}$ are active. Deassertion of $\overline{OE}$ can be asynchronous to the reference clock without generation of output runt pulses.	Q[0-9] = L, $\overline{Q[0-9]}$ =H (outputs disabled). Assertion of OE can be asynchronous to the reference clock without generation of output runt pulses.

Table 3. Absolute Maximum Ratings[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-65	125	°C	
T_{Func}	Functional temperature range	T_A = -40	T_J = +110	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating junction temperature[a] (continuous operation) MTBF = 9.1 years			110	°C	

a. Operating junction temperature impacts device life time. Maximum continues operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this datasheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES7111 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES7111 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. DC Characteristics (V_{CC} = 3.3V±5%, T_J = 0°C to + 110°C)[a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$ (HSTL/LVDS differential signals)						
V_{DIF}	Differential input voltage[b]	0.2			V	
$V_{X, IN}$	Differential cross point voltage[c]	0.25	0.68 - 0.9	V_{CC}-1.3	V	
V_{IH}	Input high voltage	V_X+0.1			V	
V_{IL}	Input low voltage			V_X-0.1	V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_X \pm 0.1V$
Clock input pair CLK1, $\overline{CLK1}$ (PECL differential signals)						
V_{PP}	Differential input voltage[d]	0.15		1.0	V	Differential operation
V_{CMR}	Differential cross point voltage[e]	1.0		V_{CC}-0.6	V	Differential operation
V_{IH}	Input voltage high	V_{CC}-1.165		V_{CC}-0.880	V	
V_{IL}	Input voltage low	V_{CC}-1.810		V_{CC}-1.475	V	
I_{IN}	Input Current[a]			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
LVCMOS control inputs $\overline{OE}$, CLK_SEL						
V_{IL}	Input voltage low			0.8	V	
V_{IH}	Input voltage high	2.0			V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
LVDS clock outputs (Q[0-9], $\overline{Q[0-9]}$)						
V_{PP}	Output Differential Voltage (peak–to–peak)	250			mV	LVDS
V_{OS}	Output Offset Voltage	1125		1275	mV	LVDS
Supply current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)

a. DC characteristics are design targets and pending characterization.
b. V_{DIF} (DC) is the minimum differential HSTL/LVDS input voltage swing required for device functionality.
c. V_X (DC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
d. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
e. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics (V_{CC} = 3.3V±5%, T_J = 0°C to + 110°C) [a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$ (HSTL/LVDS differential signals)						
V_{DIF}	Differential input voltage[c] (peak-to-peak)	0.4			V	
$V_{X, IN}$	Differential cross point voltage[d]	0.68		1.275	V	
f_{CLK}	Input Frequency		1000	TBD	MHz	
t_{PD}	Propagation Delay CLK0 to Q[0-9]			TBD	ps	
Clock input pair CLK1, $\overline{CLK1}$ (PECL differential signals)						
V_{PP}	Differential input voltage[e] (peak-to-peak)	0.2		1.0	V	
V_{CMR}	Differential input crosspoint voltage[f]	1		V_{CC}-0.6	V	
f_{CLK}	Input Frequency		1000		MHz	Differential
t_{PD}	Propagation Delay CLK1 to Q[0-9]			TBD	ps	Differential
LVDS clock outputs (Q[0-9], $\overline{Q[0-9]}$)						
$t_{sk(O)}$	Output-to-output skew			50	ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter			TBD		
DC_O	Output duty cycle	TBD	50	TBD	%	DC_{fref}= 50%
t_r, t_f	Output Rise/Fall Time	0.05		TBD	ns	20% to 80%
t_{PDL}[g]	Output disable time	2.5·T + t_{PD}		3.5·T + t_{PD}	ns	T=CLK period
t_{PLD}[h]	Output enable time	3·T + t_{PD}		4·T + t_{PD}	ns	T=CLK period

a. AC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
c. V_{DIF} (DC) is the minimum differential HSTL/LVDS input voltage swing required for device functionality.
d. V_X (DC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{DIF} (DC) specification.
e. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
f. V_{CMR} (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
g. Propagation delay OE deassertion to differential output disabled (differential low: true output low, complementary output high).
h. Propagation delay OE assertion to output enabled (active).

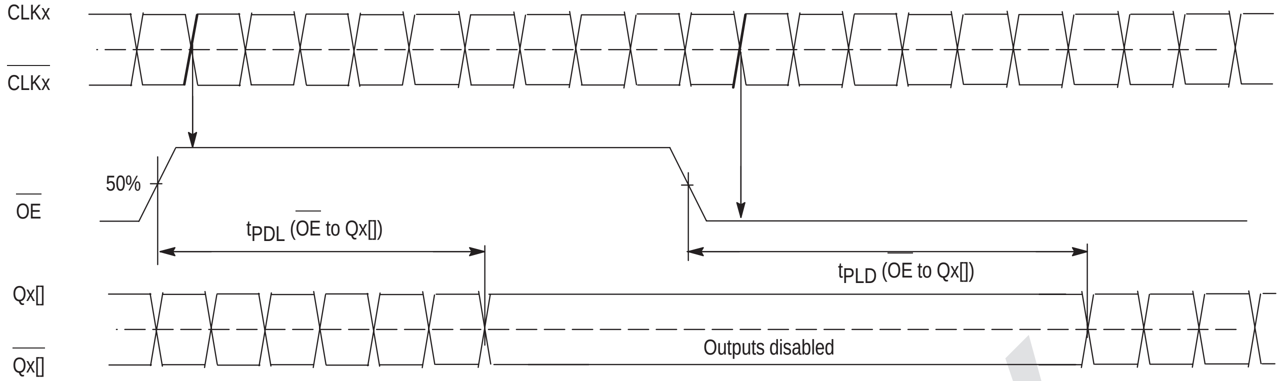


Figure 3. MC100ES7111 AC test reference

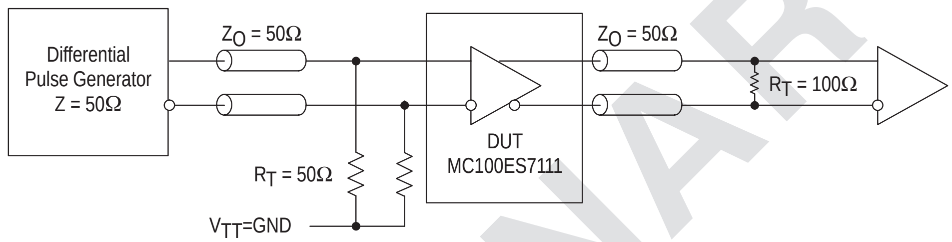


Figure 4. MC100ES7111 AC test reference

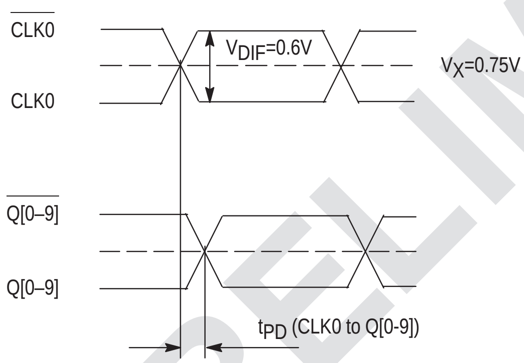


Figure 5. MC100ES7111 AC reference measurement waveform (HSTL input)

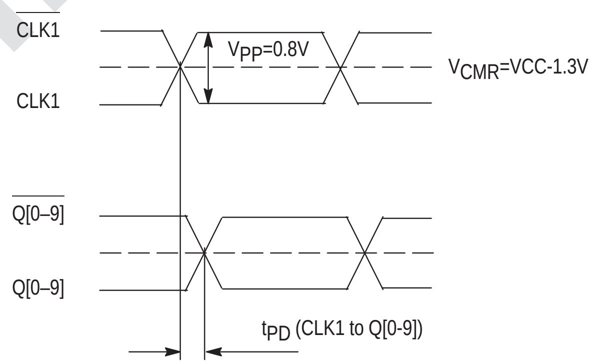


Figure 6. MC100ES7111 AC reference measurement waveform (PECL input)

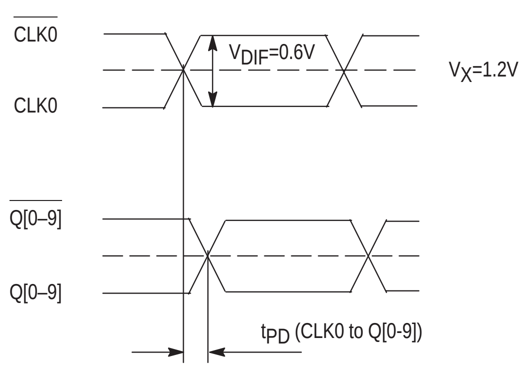
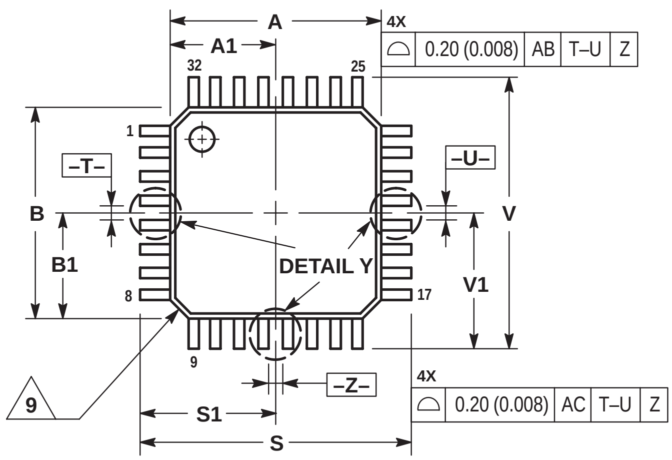
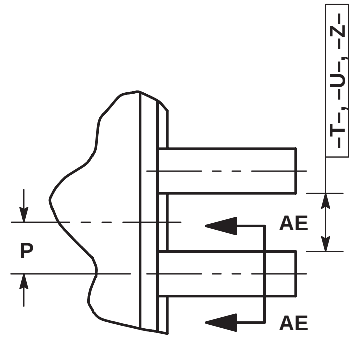


Figure 7. MC100ES7111 AC reference measurement waveform (LVDS input)

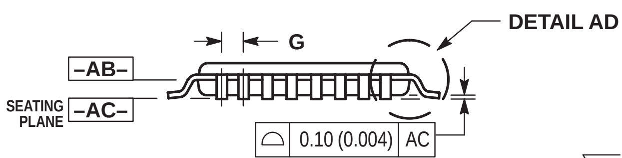
OUTLINE DIMENSIONS

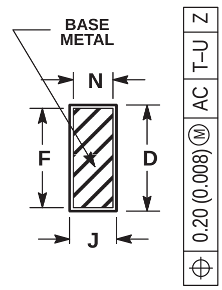
FA SUFFIX
LQFP PACKAGE
CASE 873A-02
ISSUE A



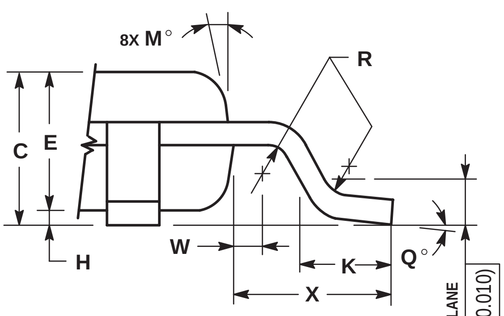


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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