19-3754; Rev 0; 8/05

Constant-Frequency, Half-Bridge CCFL Inverter Controller

General Description

The MAX8729 cold-cathode-fluorescent lamp (CCFL) inverter controller is designed to drive multiple CCFLs using the half-bridge inverter consisting of two external n-channel power MOSFETs. The half-bridge topology minimizes the component count, while providing near sinusoidal drive waveforms. The MAX8729 operates in resonant mode during striking and switches over to constant-frequency operation after all the lamps are lit. This unique feature ensures reliable striking under all conditions and reduces the transformer stress.

The MAX8729 provides accurate lamp-current regulation (±2.5%). The lamp current is adjustable with an external resistor. The MAX8729 changes the brightness by turning the CCFL on and off using a digital pulse-width modulation (DPWM) method, while maintaining the lamp current constant. The brightness can be adjusted with an analog voltage on the CNTL pin, or with an external PWM signal.

The MAX8729 is capable of synchronizing and adjusting the phase of the gate drivers and DPWM oscillator. These features allow multiple MAX8729 ICs to be connected in a daisy-chain configuration. The switching frequency and DPWM frequency of the master IC can be easily adjusted using external resistors, or synchronized with system signals. If the controller loses the external sync signals, it switches over to the internal oscillators and keeps operating. Phase-shift select pins PS1 and PS2 can be used to program four different phase shifts, allowing up to five MAX8729s to be used together.

The MAX8729 protects the inverter from lamp-out, secondary overvoltage, and secondary short-circuit faults. The MAX8729 can drive large-power MOSFETs typically used in applications where one power stage drives four or more CCFL tubes in parallel. An internal 5.35V linear regulator powers the MOSFET drivers and most of the internal circuitry. The MAX8729 is available in a low-cost, 28-pin QSOP package and operates over the -40°C to +85°C extended temperature range.

Applications

LCD Monitors	Notebook Computers
LCD TVs	Automotive Infotainment

Ordering Information

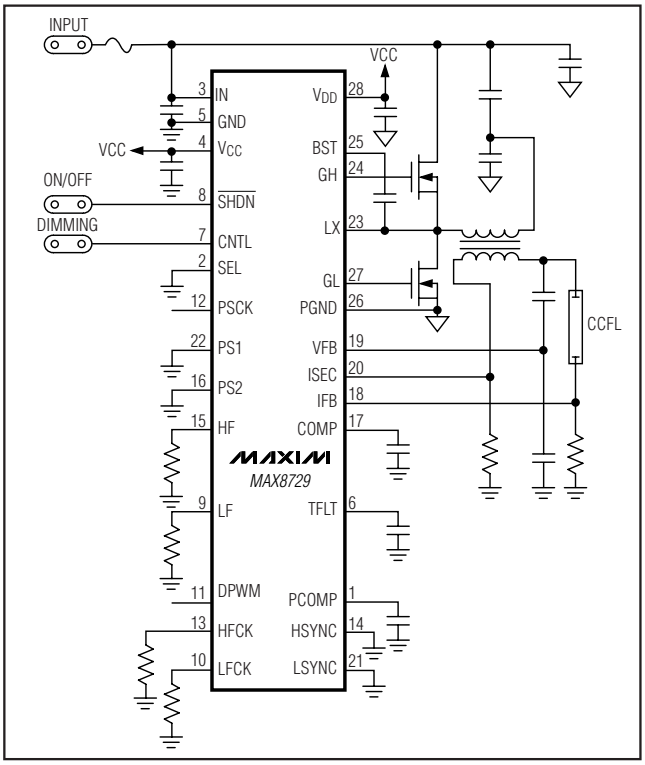
PART	TEMP RANGE	PIN-PACKAGE
MAX8729EEI	-40°C to +85°C	28 QSOP

Pin Configuration appears at end of data sheet.

Features

- **Low-Cost, Half-Bridge Inverter Topology**
- **Resonant Mode Striking Ensures Startup**
- **Constant-Frequency Operation After Lamp Ignition**
- **Drives Large External MOSFETs**
- **Supports Multilamp Applications**
- **Sync and Phase-Shift Controls Allow Daisy-Chained Operation**
- **Adjustable Switching Frequency and DPWM Frequency**
- **±2.5% Lamp-Current Regulation**
- **10:1 Dimming Range**
- **Accurate Analog-Dimming Control**
- **Lamp-Out Detection with Adjustable Timeout**
- **Secondary Current and Voltage Limiting**
- **Primary Current Limit with $R_{DS(ON)}$ Sensing**
- **Adjustable DPWM Rise and Fall Time**
- **Low-Cost, 28-Pin QSOP Package**

Simplified Operating Circuit



Constant-Frequency, Half-Bridge CCFL Inverter Controller

ABSOLUTE MAXIMUM RATINGS

IN, LX to GND .....-0.3V to +30V
BST to GND .....-0.3V to +36V
BST to LX .....-0.3V to +6V
V_{CC}, V_{DD} to GND .....-0.3V to +6V
GH to LX .....-0.3V to V_{BST} + 0.3V
CNTL, COMP, GL, DPWM, HF, LF, HFCK, LFCK, HSYNC, LSYNC, PS1, PS2, PSCK, TFLT, PCOMP, SEL .....-0.3V to V_{CC} + 0.3V
IFB, ISEC, VFB to GND .....-6V to +6V
$\overline{SHDN}$ to GND .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 10.8mW/°C above +70°C) 860.2mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{DD} = 5.3V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input Voltage Range		6		28	V
IN Quiescent Current	$V_{\overline{SHDN}}$ = 5.3V, V_{IN} = 28V		3.2	6	mA
IN Quiescent Current, Shutdown	$\overline{SHDN}$ = GND		6	20	µA
V_{CC} Output Voltage, Normal Operation	$V_{\overline{SHDN}}$ = 5.3V, 6V < V_{IN} < 28V, 0 < I_{LOAD} < 10mA	5.20	5.35	5.50	V
V_{CC} Output Voltage, Shutdown	$\overline{SHDN}$ = GND, no load	3.5	4.6	5.5	V
V_{CC} Undervoltage Lockout Threshold	V_{CC} rising (leaving lockout)			4.5	V
	V_{CC} falling (entering lockout)	4.0			
V_{CC} Undervoltage-Lockout Hysteresis			200		mV
GH, GL On-Resistance, Low State	I_{TEST} = 10mA		1	2	Ω
GH, GL On-Resistance, High State	I_{TEST} = 10mA		4	6	Ω
BST Leakage Current	V_{BST} = 17V, V_{LX} = 12V			5	µA
Resonant Frequency Range	Not tested	30		80	kHz
Minimum Off-Time		330	416	560	ns
Maximum Off-Time (LX-GND)		24.0	30.7	42.0	µs
Low-Side MOSFET Maximum Current-Limit Threshold (LX-GND)		370	400	470	mV
High-Side MOSFET Maximum Current-Limit Threshold (IN – LX)		370	400	470	mV
Low-Side MOSFET Zero-Current-Crossing Threshold (GND – LX)		0	10	18	mV
High-Side MOSFET Zero-Current-Crossing Threshold (LX – IN)		-16	+6	+28	mV
Current-Limit Leading Edge Blanking		310	410	560	ns
IFB Regulation Point	Internally full-wave rectified	770	790	810	mV
IFB Maximum AC Voltage			±3		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{DD} = 5.3V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IFB Input Bias Current	$0 < V_{IFB} < 2V$	-3		+3	µA
	$-2V < V_{IFB} < 0$	-150			
IFB Lamp-Out Threshold	Reject 1µs glitches	760	790	820	mV
IFB-to-COMP Transconductance	$0.5V < V_{COMP} < 2.4V$		100		µS
COMP Output Impedance			10		MΩ
COMP Discharge Current During Overvoltage or Overcurrent Fault	V_{IFB} = 800mV, V_{ISEC} = 2.5V		1200		µA
COMP Discharge Current During DPWM Off-Time	CNTL = GND, V_{COMP} = 1.5V		100		µA
ISEC Input Voltage Range		-3		+3	V
ISEC Input Bias Current		-0.3		+0.3	µA
ISEC Overcurrent Threshold		1.18	1.21	1.26	V
VFB Input-Voltage Range		-4		+4	V
VFB Input Bias Current	$-4V < V_{VFB} < 4V$	-25		+25	µA
VFB Overvoltage Threshold		2.15	2.25	2.35	V
Main Oscillator Frequency	R_{HF} = 100kΩ	51.7	53.8	55.9	kHz
Main Oscillator Frequency Range		20		100	kHz
HF, HFCK, LF, LFCK Input-Low Voltage	Slave mode, $V_{CNTL} = V_{CC}$			0.8	V
HF, HFCK, LF, LFCK Input-High Voltage	Slave mode, $V_{CNTL} = V_{CC}$	2.1			V
HF, HFCK, LF, LFCK Input Hysteresis	Slave mode, $V_{CNTL} = V_{CC}$		200		mV
HF, HFCK, LF, LFCK Input Bias Current	Slave mode, $V_{CNTL} = V_{CC}$	-1		+1	µA
HF, HFCK, LF, LFCK Input Rise and Fall Time	Slave mode, $V_{CNTL} = V_{CC}$			200	ns
HF Input Frequency Range	Slave mode, $V_{CNTL} = V_{CC}$	20		100	kHz
HFCK Input Frequency Range	Slave mode, $V_{CNTL} = V_{CC}$	120		600	kHz
HSYNC Input Frequency Range	R_{HF} = 100kΩ	190		460	kHz
LF Input Frequency Range	Slave mode, $V_{CNTL} = V_{CC}$	80		300	Hz
LFCK Input Frequency Range	Slave mode, $V_{CNTL} = V_{CC}$	10.24		38.40	kHz
LSYNC Input Frequency Range	R_{LF} = 150kΩ	120		280	Hz
DPWM Chopping Frequency	R_{LF} = 150kΩ	199	207	215	Hz
DPWM Frequency Range	R_{LF} = 300kΩ	80		300	Hz

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{DD} = 5.3V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PS1, PS2, LSYNC, HSYNC, SEL Input Low Voltage				0.8	V
PS1, PS2, LSYNC, HSYNC, SEL Input High Voltage		2.1			V
PS1, PS2, LSYNC, HSYNC, SEL Input Hysteresis			200		mV
PS1, PS2, LSYNC, HSYNC, SEL Input Bias Current		-1		+1	µA
HFCK, LFCK, PSCK, DPWM Output On-Resistance	I_{TEST} = 1mA			2.5	kΩ
CNTL Minimum Duty-Cycle Threshold		0.21	0.23	0.26	V
CNTL Maximum Duty-Cycle Threshold		1.9	2.0	2.1	V
CNTL Input Current	0 < V_{CNTL} < 2V	-0.1		+0.1	µA
CNTL Input Threshold	Slave mode	4.2	4.5	4.8	V
DPWM A/D Converter Resolution	Guaranteed monotonic		5		Bits
$\overline{SHDN}$ Input Low Voltage				0.8	V
$\overline{SHDN}$ Input High Voltage		2.1			V
$\overline{SHDN}$ Input Bias Current		-1		+1	µA
TFLT Charging Current	V_{ISEC} < 1.25 and V_{IFB} < 790mV; V_{FLT} = 2.0V	0.95	1.00	1.05	µA
	V_{ISEC} < 1.25 and V_{IFB} > 790mV; V_{FLT} = 2.0V		-1		
	V_{ISEC} > 1.25 and V_{IFB} < 790mV; V_{FLT} = 2.0V		126		
TFLT Trip Threshold		3.9	4.0	4.1	V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{DD} = 5.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input-Voltage Range		6		28	V
IN Quiescent Current	$V_{\overline{SHDN}}$ = 5.3V, V_{IN} = 28V			6	mA
IN Quiescent Current, Shutdown	$\overline{SHDN}$ = GND			20	µA
V_{CC} Output Voltage, Normal Operation	$V_{\overline{SHDN}}$ = 5.3V, 6V < V_{IN} < 28V, 0 < I_{LOAD} < 10mA	5.20		5.50	V
V_{CC} Output Voltage, Shutdown	$\overline{SHDN}$ = GND, no load	3.5		5.5	V
V_{CC} Undervoltage Lockout Threshold	V_{CC} rising (leaving lockout)			4.5	V
	V_{CC} falling (entering lockout)	4.0			
GH, GL On-Resistance, Low State	I_{TEST} = 10mA			3	Ω
GH, GL On-Resistance, High State	I_{TEST} = 10mA			7	Ω
Minimum Off-Time		330		560	ns
Maximum Off-Time		24.0		42.0	µs
Low-Side MOSFET Maximum Current-Limit Threshold (LX – GND)		350		500	mV
High-Side MOSFET Maximum Current-Limit Threshold (IN – LX)		350		500	mV
Low-Side MOSFET Zero-Current Crossing Threshold (GND – LX)		0		18	mV
High-Side MOSFET Zero-Current Crossing Threshold (LX – IN)		-16		+28	mV
Current-Limit Leading-Edge Blanking		310		560	ns
IFB Regulation Point	Internally full-wave rectified	770		810	mV
IFB Maximum AC Voltage			±3		V
IFB Input Bias Current	0 < V_{IFB} < 2V	-3		+3	µA
	-2V < V_{IFB} < 0	-150			
IFB Lamp-Out Threshold	Reject 1µs glitches	760		820	mV
ISEC Input Voltage Range		-3		+3	V
ISEC Overcurrent Threshold		1.18		1.26	V
VFB Input Voltage Range		-4		+4	V
VFB Overvoltage Threshold		2.15		2.35	V
Main Oscillator Frequency	R_{HF} = 100kΩ	50.0		57.6	kHz
Main Oscillator Frequency Range		20		100	kHz

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{DD} = 5.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

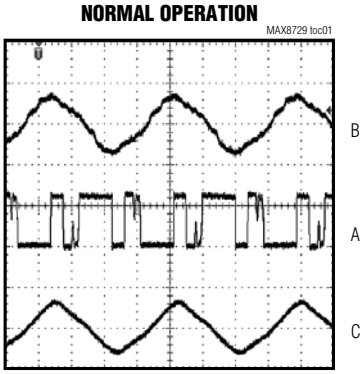
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
HF, HFCK, LF, LFCK Input Low Voltage	Slave mode, V_{CNTL} = V_{CC}			0.8	V
HF, HFCK, LF, LFCK Input High Voltage	Slave mode, V_{CNTL} = V_{CC}	2.1			V
HF, HFCK, LF, LFCK Input Rise and Fall Time	Slave mode, V_{CNTL} = V_{CC}			200	ns
HF Input Frequency Range	Slave mode, V_{CNTL} = V_{CC}	20		100	kHz
HFCK Input Frequency Range	Slave mode, V_{CNTL} = V_{CC}	120		600	kHz
HSYNC Input Frequency Range	R_{HF} = 100kΩ	190		460	kHz
LF Input Frequency Range	Slave mode, V_{CNTL} = V_{CC}	80		300	Hz
LFCK Input Frequency Range	Slave mode, V_{CNTL} = V_{CC}	10.24		38.40	kHz
LSYNC Input Frequency Range	R_{LF} = 150kΩ	120		280	Hz
DPWM Chopping Frequency	R_{LF} = 150kΩ	197		217	Hz
DPWM Input Frequency Range		80		300	Hz
PS1, PS2, LSYNC, HSYNC, SEL Input Low Voltage				0.8	V
PS1, PS2, LSYNC, HSYNC, SEL Input High Voltage		2.1			V
HFCK, LFCK, PSCK, DPWM Output On-Resistance	I_{TEST} = 1mA			2.5	kΩ
CNTL Minimum Duty-Cycle Threshold		0.21		0.26	V
CNTL Maximum Duty-Cycle Threshold		1.9		2.1	V
CNTL Input Threshold	Slave mode	4.2		4.8	V
$\overline{SHDN}$ Input Low Voltage				0.8	V
$\overline{SHDN}$ Input High Voltage		2.1			V
TFLT Charging Current	V_{ISEC} < 1.25 and V_{IFB} < 600mV, V_{FLT} = 2.0V	0.93		1.07	µA
TFLT Trip Threshold		3.9		4.1	V

Note 1: Specifications to -40°C are guaranteed by design, based on final characterization results.

Typical Operating Characteristics

(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD}, T_A = +25°C, unless otherwise noted.)

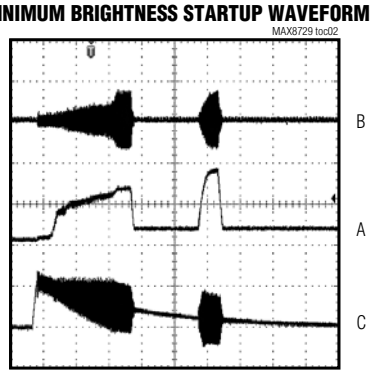
NORMAL OPERATION



4ms/div

A: LX, 10V/div
B: IFB, 2V/div
C: VFB, 2V/div

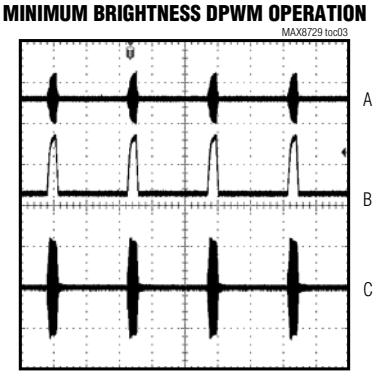
MINIMUM BRIGHTNESS STARTUP WAVEFORM



1ms/div

A: COMP, 1V/div
B: IFB, 2V/div
C: VFB, 2V/div

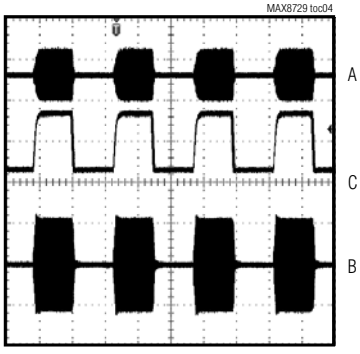
MINIMUM BRIGHTNESS DPWM OPERATION



2ms/div

A: IFB, 2V/div
B: VFB, 1V/div
C: COMP, 1V/div

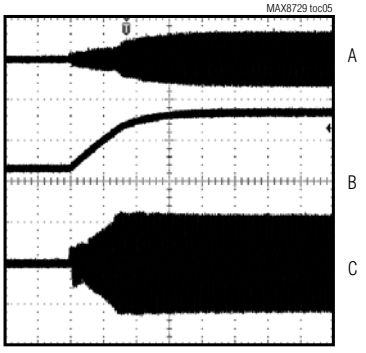
50% BRIGHTNESS DPWM OPERATION



2ms/div

A: IFB, 2V/div
B: VFB, 1V/div
C: COMP, 1V/div

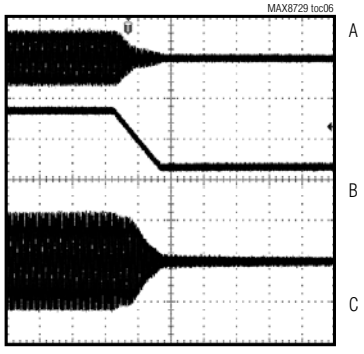
DPWM SOFT-START



100ms/div

A: IFB, 2V/div
B: VFB, 1V/div
C: COMP, 1V/div

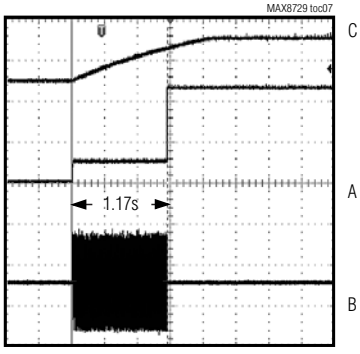
DPWM SOFT-STOP



100ms/div

A: IFB, 2V/div
B: VFB, 1V/div
C: COMP, 1V/div

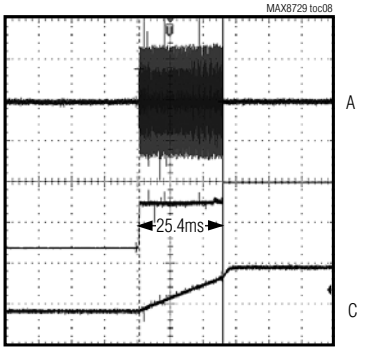
LAMP-OUT VOLTAGE LIMITING AND TIMEOUT



400ms/div

A: COMP, 2V/div
B: VFB, 2V/div
C: TFLT, 5V/div

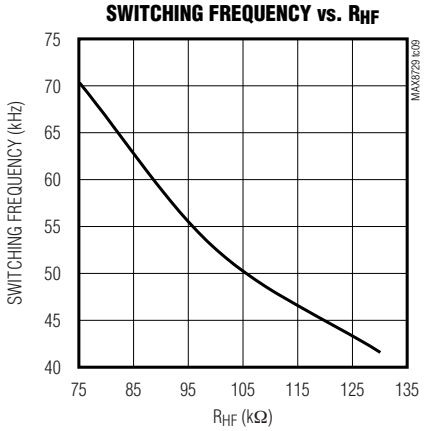
SECONDARY SHORT-CIRCUIT PROTECTION AND TIMEOUT



10ms/div

A: ISEC, 1V/div
B: COMP, 2V/div
C: TFLT, 5V/div

SWITCHING FREQUENCY vs. R_{HF}

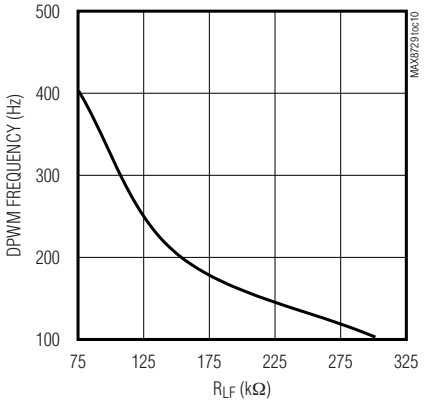


Constant-Frequency, Half-Bridge CCFL Inverter Controller

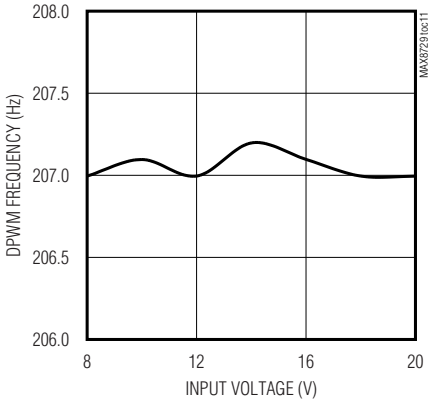
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD}, T_A = +25°C, unless otherwise noted.)

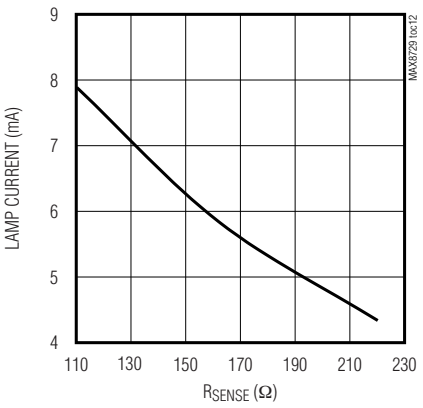
DPWM FREQUENCY vs. R_{LF}



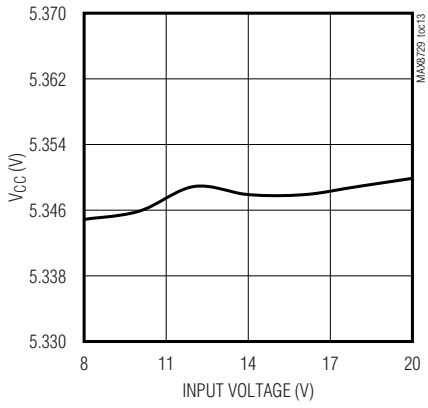
DPWM FREQUENCY vs. INPUT VOLTAGE



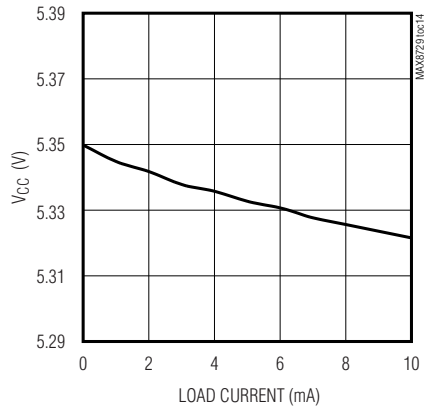
LAMP CURRENT vs. R_{SENSE}



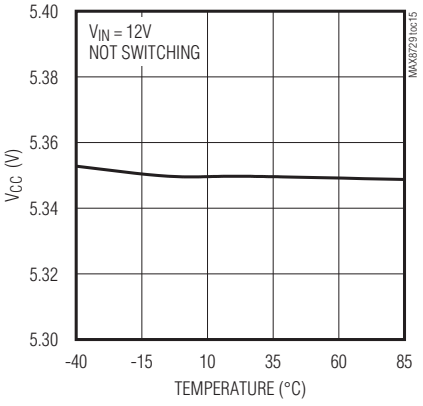
V_{CC} LINE REGULATION



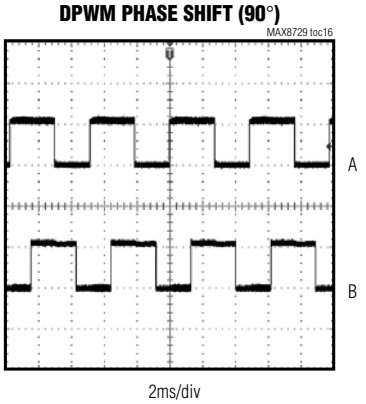
V_{CC} LOAD REGULATION



V_{CC} vs. TEMPERATURE



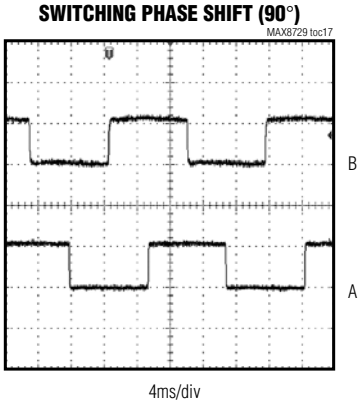
DPWM PHASE SHIFT (90°)



2ms/div

A: SLAVE DPWM 5V/div
B: MASTER DPWM 5V/div

SWITCHING PHASE SHIFT (90°)



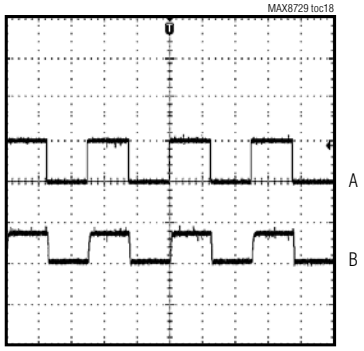
4ms/div

A: SLAVE DPWM
B: MASTER DPWM

Typical Operating Characteristics (continued)

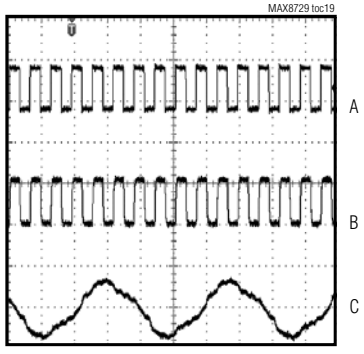
(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD}, T_A = +25°C, unless otherwise noted.)

LF SYNCHRONIZATION



A: LSYNC 5/div
B: COMP 2V/div

HF SYNCHRONIZATION



A: HSYNC, 5/div
B: HFCK, 5/div
C: IFB, 2V/div

Constant-Frequency, Half-Bridge CCFL Inverter Controller

Pin Description

PIN	NAME	FUNCTION
1	PCOMP	Compensation Node of the Phase-Lock Loop. Connect a 0.1µF capacitor between PCOMP and GND to compensate the phase-lock loop.
2	SEL	Brightness-Control Select Input. Brightness can be adjusted with an analog voltage or with an external sync signal. Connecting SEL to GND enables analog control at the CNTL pin. Connecting SEL to V_{CC} enables brightness control using an external sync signal at the LSYNC pin.
3	IN	Supply Input. Input to the internal 5.35V linear regulator that powers the device. Bypass IN to GND with a 0.1µF ceramic capacitor.
4	V_{CC}	5.35V/10mA Linear-Regulator Output. V_{CC} powers most of the control circuitry in the MAX8729. Bypass V_{CC} to GND with a 1µF ceramic capacitor.
5	GND	System Ground
6	TFLT	Fault-Timer Set Pin. Connect a 0.22µF capacitor from TFLT to GND to set the open-lamp fault delay period to approximately 1.2s and the secondary short-circuit fault-delay period to approximately 10ms. See the *Setting the Fault-Delay Time* section for details.
7	CNTL	Brightness Control Input. The usable brightness control range is from 0 to 2V. V_{CNTL} = 0 represents the minimum brightness (10% DPWM duty cycle); 2V ≤ V_{CNTL} < 4.2V represents the full brightness (100% DPWM duty cycle). The MAX8729 enters into slave mode when CNTL is connected to V_{CC}. See the *Digital PWM Dimming Control* section for details.
8	$\overline{SHDN}$	Shutdown Control Input. The MAX8729 shuts down when $\overline{SHDN}$ is pulled to GND.
9	LF	DPWM Frequency Adjustment Pin. Connect a resistor from LF to GND to set the DPWM oscillator frequency. LF is a logic input when CNTL is connected to V_{CC}.
10	LFCK	DPWM Oscillator Clock Output. LFCK is a logic input when CNTL is connected to V_{CC}.
11	DPWM	DPWM Signal Output. The DPWM output is used to control the DPWM frequency of the slave IC in master-slave operation. See the *Slave Operation* section for details.
12	PSCK	Phase-Shift Clock Output. PSCK is a logic input when CNTL is connected to V_{CC}.
13	HFCK	Main Switching Oscillator Clock Output. HFCK is a logic input when CNTL is connected to V_{CC}.
14	HSYNC	Main Switching-Frequency Sync Input. Switching frequency can be synchronized with an external signal on HSYNC. HSYNC has a Schmitt trigger input.
15	HF	Switching-Frequency Adjustment Pin. Connect a resistor from HF to GND to set the main oscillator frequency. HF is a logic input when CNTL is connected to V_{CC}.
16	PS2	Phase-Shift Select Input. The PS1 and PS2 logic inputs select between four programmable phase shifts (60°, 90°, 120°, and 180°) in master-slave operation. PS1 and PS2 should be in identical states in each slave. See the *Phase Shift* section for details.
17	COMP	Transconductance Error-Amplifier Output. A 0.01µF capacitor connected between COMP and GND sets the rise and fall time of the lamp-current envelope during DPWM operation. See the *COMP Capacitor Selection* section for details.

Pin Description (continued)

PIN	NAME	FUNCTION
18	IFB	Lamp-Current Feedback Input. The IFB sense signal is internally full-wave rectified. The average value of the rectified signal is regulated to 790mV (typ) by controlling the on-time of the high-side MOSFET. An open-lamp fault is generated if the IFB is continuously below 790mV (typ) for a period set by TFLT. See the *Lamp-Out Protection* and *Setting the Fault-Delay Time* sections for details.
19	VFB	Transformer Secondary-Voltage Feedback Input. When the peak voltage on VFB exceeds the 2.3V (typ) overvoltage threshold, the controller turns on an internal 1.2mA current sink, discharging the COMP capacitor. A capacitive voltage-divider between the high-voltage terminal of the CCFL tube and GND determines the maximum lamp output voltage during startup and lamp-out fault. See the *Setting the Secondary Voltage Limit* section for details.
20	ISEC	Transformer Secondary-Current Feedback Input. When the peak voltage on ISEC exceeds the internal overcurrent threshold, the controller turns on an internal 1.2mA current sink, discharging the COMP capacitor. A current-sense resistor connected between the low-voltage end of the transformer secondary and the ground determines the maximum secondary current during short-circuit fault. See the *Setting the Secondary Current Limit* section for details.
21	LSYNC	DPWM Sync Input. DPWM frequency can be synchronized with an external signal on LSYNC. When SEL is connected to V_{CC}, the duty cycle of the LSYNC signal determines the brightness. LSYNC has a Schmitt trigger input.
22	PS1	Phase-Shift-Select Input. The PS1 and PS2 logic inputs select between four programmable phase shifts (60°, 90°, 120°, and 180°) in master-slave operation. PS1 and PS2 should be in identical states in each slave. See the *Phase Shift* section for details.
23	LX	Switching Node. LX is the return of the high-side gate driver. LX is also the input to the primary current-limit and zero-crossing comparators. The controller senses the voltage across the high-side MOSFET (IN - LX) and low-side MOSFET (LX - GND) to detect primary overcurrent condition and zero crossing.
24	GH	High-Side MOSFET Gate-Driver Output
25	BST	High-Side Gate-Driver Supply Input. The MAX8729 includes an integrated boost diode. Connect a 0.1µF capacitor between LX and BST to complete the bootstrap circuit.
26	PGND	Power Ground. PGND is the return for the low-side gate driver.
27	GL	Low-Side MOSFET Gate-Driver Output
28	V_{DD}	Low-Side MOSFET Gate-Driver Supply Input

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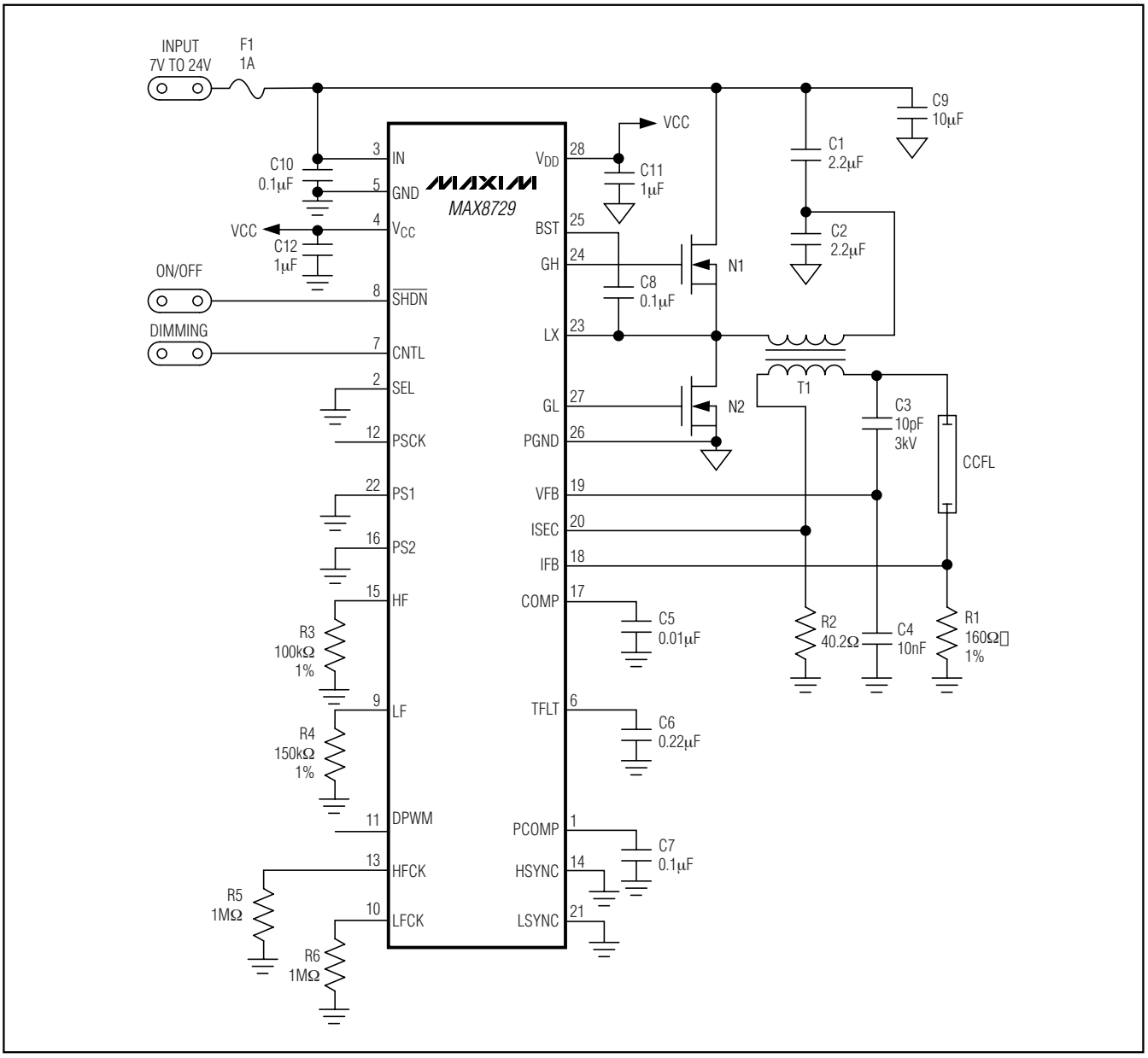

Figure 1. Typical Stand-Alone Operating Circuit

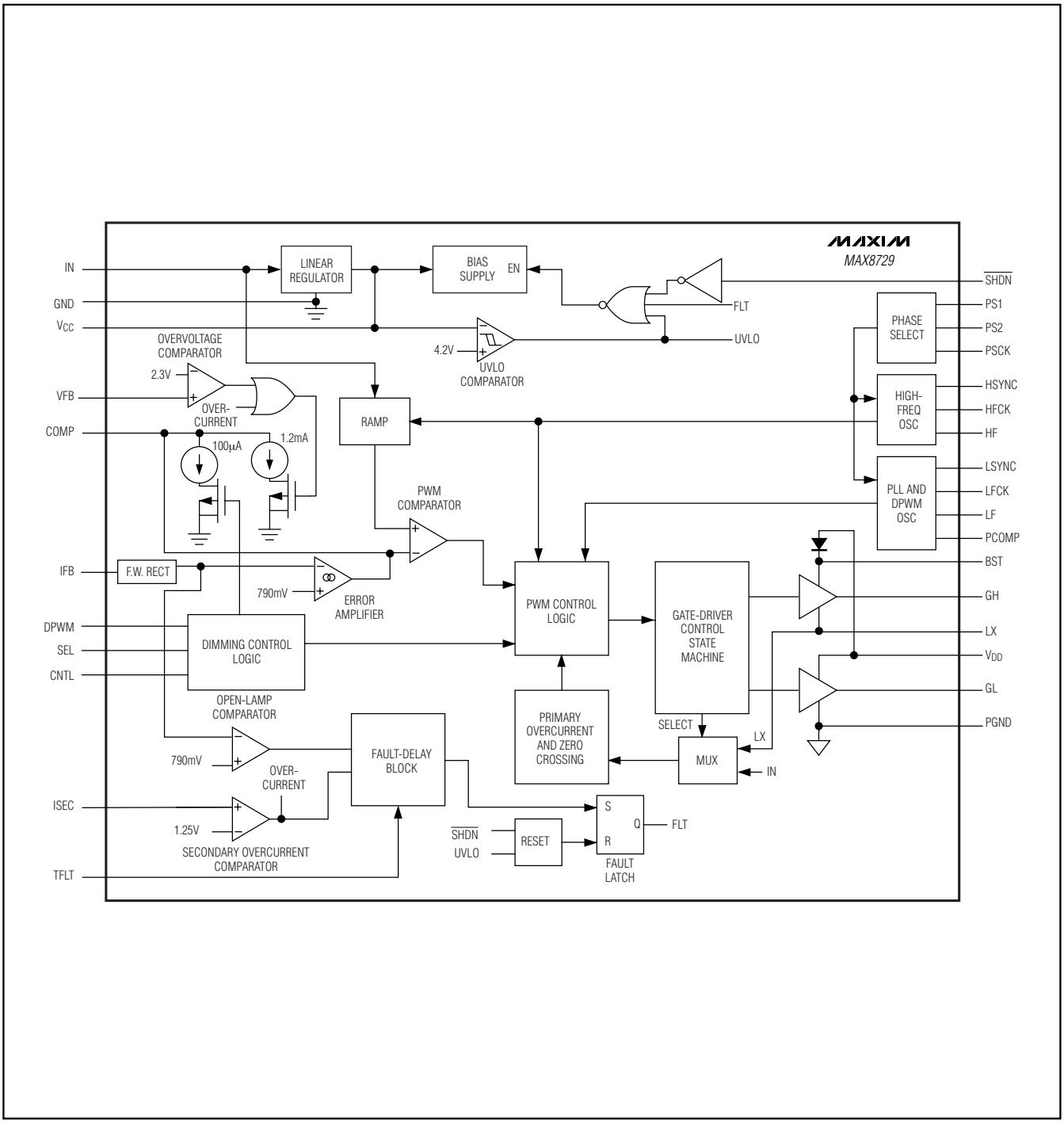

Figure 2. Functional Diagram

Constant-Frequency, Half-Bridge CCFL Inverter Controller

Detailed Description

Figure 1 shows the Stand-Alone Typical Operating Circuit. Figure 2 shows the Functional Diagram of the MAX8729. The circuit architecture consists of a half-bridge inverter, which converts unregulated DC into a nearly sinusoidal, high-frequency, AC output for powering CCFLs. The MAX8729 is biased from an internal 5.35V linear regulator with UVLO comparator that ensures stable operation and clean startup characteristics. There are several layers of fault-protection circuitry, consisting of comparators for detecting primary-side current limit, secondary-side overvoltage, secondary short circuit, and open-lamp faults. A logic block arbitrates the comparator outputs by making sure that a given fault persists for a minimum duration before registering the fault condition. A separate block provides dimming control based upon analog or DPWM inputs. Finally, a dedicated logic circuit provides synchronization and phase control functions for daisy chaining up to five MAX8729s without phase overlap.

The inverter operates in resonant mode during striking and switches over to constant-frequency operation after all the lamps are lit. This unique feature ensures reliable striking under all conditions and reduces the transformer stress. The constant-frequency architecture can be synchronized and phase shifted for daisy-chained applications. Multiple lamps can also be driven in parallel within a single stage. The MAX8729's gate drivers are strong enough to drive the large-power MOSFETs needed when one power stage drives four or more CCFL lamps in parallel.

The MAX8729 provides accurate lamp-current regulation (±2.5%). A primary-side current sense provides cycle-by-cycle current limit and zero-crossing detection, while the secondary current is sensed with a separate loop that provides fine adjustment of the lamp current with an external resistor. The MAX8729 controls lamp brightness by turning the CCFL on and off using a DPWM method, while maintaining approximately constant lamp current. The brightness set point can be adjusted with an analog voltage on the CNTL pin, or with an external PWM signal.

The MAX8729 has a single compensation input (COMP), which also establishes the soft-start and soft-stop timing characteristics. Control logic changes the available drive current at COMP based on the operating mode to adjust the inverter's dynamic behavior.

Constant-Frequency Operation

The MAX8729 operates in constant-frequency mode in normal operation. There are two ways to set the switching frequency:

1) The switching frequency can be set with an external resistor connected between HF and GND. The switching frequency is given by the following equation:

$$f_{SW} = 54kHz \times \frac{100k\Omega}{R_{HF}}$$

The adjustable range of the switching frequency is between 20kHz and 100kHz (R_{HF} is between 270kΩ and 54kΩ).

2) The switching frequency can be synchronized by an external high-frequency signal. Connect HF to GND through a 100kΩ resistor, and connect HSYNC to the external high-frequency signal. The resulting synchronized switching frequency (f_{SW}) is 1/6th the frequency of the external signal (f_{EXT}):

$$f_{SW} = \frac{f_{EXT}}{6}$$

The frequency range of the external signal should be between 190kHz and 460kHz, with R_{HF} + 100kΩ resulting in a switching frequency range between 32kHz and 77kHz.

Figure 3 illustrates the constant-frequency operation, with timing diagrams that show the primary current, clock signal, and gate-drive signals. At the beginning of the positive half cycle, the high-side switch is on and the primary current ramps up. The controller turns off the high-side switch at t_1. The primary current continues to flow in the same direction, which forward biases the body diode of the low-side switch after the high-side switch is off. When the controller turns on the low-side switch, the voltage drop across the switch is nearly zero. This zero-voltage switching (ZVS) operation results in lower switching losses. With DL on, the primary current ramps down. If the primary current reaches zero (t_2) before the falling edge of the oscillator clock arrives (t_3), as shown in Figure 3(A), the controller turns off the low-side switch at t_2. Both the high-side switch and low-side switch stay off until t_3. The controller turns on the low-side switch at the falling edge of the clock (t_3). The primary current ramps up in the other direction, starting the negative half cycle. If the clock falling edge comes before the zero crossing as shown in Figure 3(B), the low-side switch stays on, which allows the primary current to reach zero and then

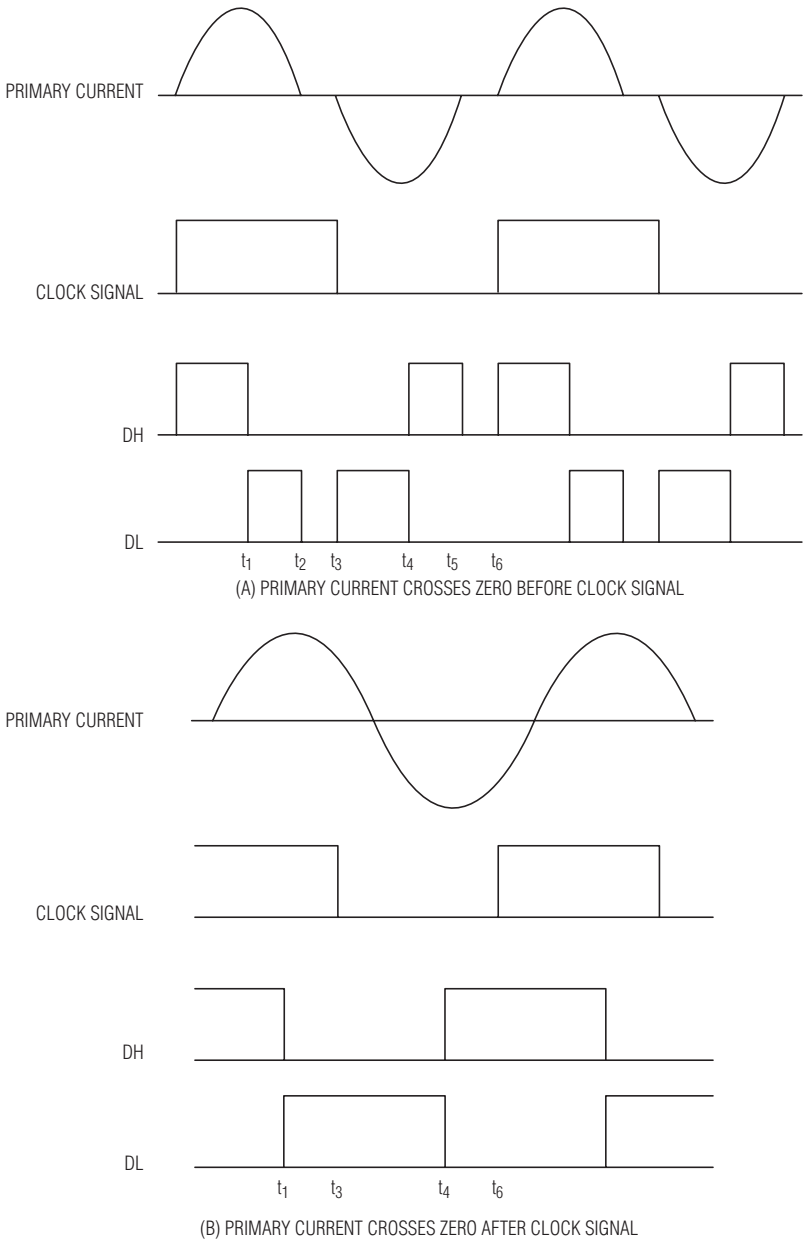

Figure 3. Constant-Frequency-Operation Timing Diagram

Constant-Frequency, Half-Bridge CCFL Inverter Controller

continues below ground to start the negative cycle. During the negative half cycle, the controller turns off the low-side switch at t_4. After which, the controller turns on the high-side switch under ZVS conditions and a new cycle begins. In both cases, A and B, ZVS operation reduces the turn-on switching losses of both power switches, resulting in better efficiency.

Resonant Startup

The MAX8729 operates in resonant mode during startup. In resonant operation, the inverter keeps increasing the secondary voltage until either the lamp is struck or the controller activates overvoltage protection. In resonant mode, the switching frequency is synchronized with the natural resonant frequency of the resonant tank circuit composed of: transformer leakage inductance, primary capacitive divider, and secondary resonant capacitor. The synchronization and phase-shift functions are disabled during startup. Figure 4 demonstrates the resonant operation, with a timing diagram of the primary current and gate signals. In the resonant mode, the high side turns on at the beginning of the positive half cycle. The primary current ramps up. The controller turns off the high-side switch at t_1 to regulate the lamp current. The primary current continues to flow in the same direction, which forward biases the body diode of the low-side switch after the high-side switch is off. When the controller turns on the low-side switch, the voltage drop across the switch is nearly zero. This ZVS operation results in lower switching losses. With DL on, the primary current ramps down through zero until t_2, when the controller turns off the low-side switch. After which, the controller turns on the high-side switch with ZVS condition and a new cycle begins. The ZVS operation of this architecture reduces the turn-on switching losses of both power switches, resulting in better efficiency.

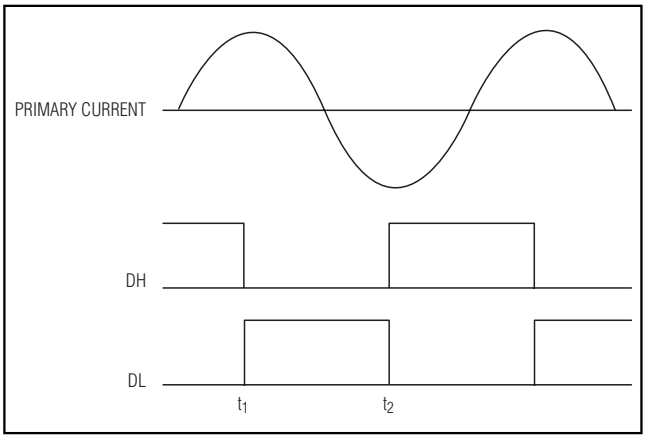

Figure 4. Resonant-Operation Timing Diagram

Lamp-Current Regulation

The MAX8729 uses a lamp-current control loop to regulate the current delivered to the CCFL. The heart of the control loop is a transconductance error amplifier in Figure 2. The AC lamp current is sensed with a sense resistor connected in series with the low-voltage terminal of the lamp. The voltage across this resistor is fed to the IFB input and is internally full-wave rectified. The transconductance error amplifier compares the rectified IFB voltage with a 790mV (typ) internal reference to generate an error current. The error current charges and discharges a capacitor connected between the error amplifier's output (COMP) and ground to create an error voltage (V_{COMP}). V_{COMP} is then compared with an internal ramp signal to control the high-side MOSFET switch on-time (t_{ON}).

Transformer Secondary Voltage Limiting

The MAX8729 reduces the voltage stress on the transformer's secondary winding by limiting the secondary voltage during startup and open-lamp fault. The AC voltage across the transformer secondary winding is sensed through a capacitive voltage-divider. The voltage across the low-side capacitor of the divider is fed to the VFB input and is internally half-wave rectified. An overvoltage comparator compares the VFB voltage with a 2.3V (typ) internal threshold. Once the sense voltage exceeds the overvoltage threshold, the MAX8729 turns on a 1.2mA current source that discharges the COMP capacitor. As the COMP voltage decreases, the high-side MOSFET's on-time shortens, which reduces the transformer secondary peak voltage. The MAX8729 stops discharging the COMP capacitor after the secondary peak voltage is below the threshold set by the capacitive voltage-divider. This mechanism effectively limits the secondary voltage.

Lamp Startup

A CCFL is a gas-discharge lamp that is normally driven in the avalanche mode. To start ionization in a nonionized lamp, the applied voltage (striking voltage) must be increased to the level required to start ionization in the lamp. For example, the normal running voltage of a typical CCFL is around $650V_{RMS}$, but the striking voltage can be as high as $1800V_{RMS}$.

The MAX8729's unique resonant startup method ensures reliable striking. Before the lamp is ionized, the lamp impedance is infinite. The transformer secondary leakage inductance and the high-voltage parallel capacitor determine the unloaded resonant frequency. Since the unloaded resonant circuit has a high Q, the inverter keeps increasing the secondary voltage until either the lamp is struck or the controller activates the secondary overvoltage protection.

Upon power-up, V_{COMP} slowly rises, increasing the duty cycle of the high-side MOSFET switches and providing a measure of soft-start. In addition, the MAX8729 charges V_{FB} to the overvoltage threshold (2.3V, typ) immediately after the device is enabled. The DC voltage on V_{FB} is gradually discharged through an internal resistor during startup. This feature is equivalent to slowly raising the overvoltage threshold during startup, so it further improves the soft-start behavior. The MAX8729 automatically switches over to the constant-frequency operation after the lamp current reaches regulation.

Feed-Forward Control and Dropout Operation

The MAX8729 is designed to maintain tight control of the lamp current when a line transient occurs. The feed-forward control instantaneously adjusts the on-time for changes in input voltage (V_{IN}). This feature provides immunity to input-voltage variations and simplifies loop compensation over wide-input voltage ranges. The feed-forward control also improves the line regulation for short DPWM on-times and makes startup transients less dependent on the input voltage.

Feed-forward control is implemented by increasing the internal voltage ramp rate for higher V_{IN}. This has the effect of varying t_{ON} as a function of the input voltage while maintaining about the same signal levels at V_{COMP}. Since the required voltage change across the compensation capacitor is minimal, the controller's response to input voltage changes is essentially instantaneous.

DPWM Dimming Control

The MAX8729 controls the brightness of the CCFL by "chopping" the lamp current on and off using a low-frequency (between 100Hz and 350Hz) DPWM signal either from the internal oscillator or from an external signal source. In DPWM operation, COMP controls the dynamics of the lamp-current envelope. At the beginning of the DPWM ON cycle, the average value of the lamp-current feedback signal is below the regulation point, so the transconductance error amplifier sources current into the COMP capacitor. The switch on-time (t_{ON}) gradually increases as V_{COMP} rises, which provides soft-start. At the end of the DPWM ON cycle, the MAX8729 turns on a 100µA internal current source. The current source linearly discharges the COMP capacitor, gradually decreasing t_{ON}, and providing soft-stop.

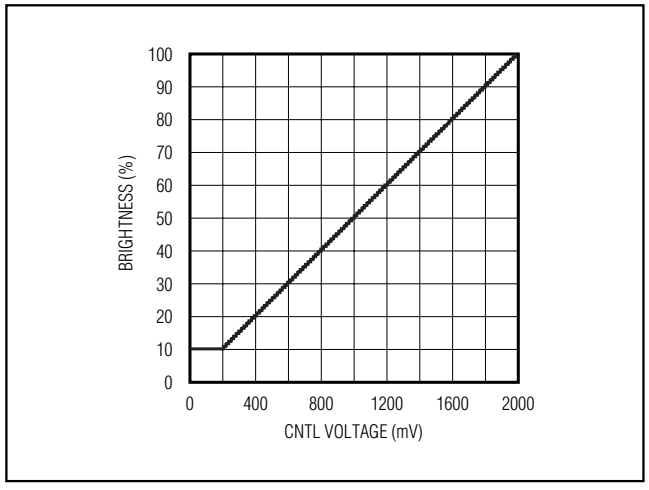

Figure 5. Theoretical Brightness vs. Control Voltage

Using the Internal Oscillator

When the SEL pin is connected to ground, the MAX8729 uses the internal oscillator to generate the DPWM signal. The frequency of the internal DPWM oscillator is adjustable through a resistor connected between LF and GND. The DPWM frequency is given by the following equation:

$$f_{DPWM} = \frac{207Hz \times 150k\Omega}{R_{LF}}$$

The adjustable range of the DPWM frequency is between 100Hz and 300Hz (R_{LF} is between 217kΩ and 103kΩ).

The CCFL brightness is proportional to the DPWM duty cycle, which can be adjusted from 10% to 100% through the CNTL pin. CNTL is an analog input with a usable input voltage range between 0 and 2V, which is digitized to select one of 128 brightness levels. As shown in Figure 5, the MAX8729 ignores the first 13 steps, so the first 13 steps all represent the same brightness. When V_{CNTL} is between 0 and 203mV, the DPWM duty cycle is always 10%. When V_{CNTL} is above 203mV, a 15.625mV change on CNTL results in a 0.78% change in the DPWM duty cycle. When V_{CNTL} is equal to or above 2V, the DPWM duty cycle is always 100%.

Using the External PWM Signal

To use the external DPWM signal to control the brightness, connect SEL to V_{CC} and connect LSYNC to the external signal source. The frequency range of the external signal is between 100Hz and 300Hz with R_{LF} = 150kΩ. In this mode, the brightness control input CNTL is disabled, and the brightness is proportional to the duty cycle of the external signal. When the duty cycle of the external signal is 100%, the CCFL reaches full brightness. If the duty cycle of the external signal is less than 10%, the CCFL brightness is adjusted accordingly.

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Lamp-Out Protection

For safety, the MAX8729 monitors the lamp-current feedback (IFB) to detect faulty or open CCFL lamps and shorted IFB sense resistor. As described in the *Lamp-Current Regulation* section, the voltage on IFB is internally full-wave rectified. If the rectified IFB voltage is below 790mV, the MAX8729 charges the TFLT capacitor with 1µA. The MAX8729 latches off if the voltage on TFLT exceeds 4V. Unlike the normal shutdown mode, the linear regulator output (V_{CC}) remains at 5.3V. Toggling $\overline{SHDN}$ or cycling the input power reactivates the device.

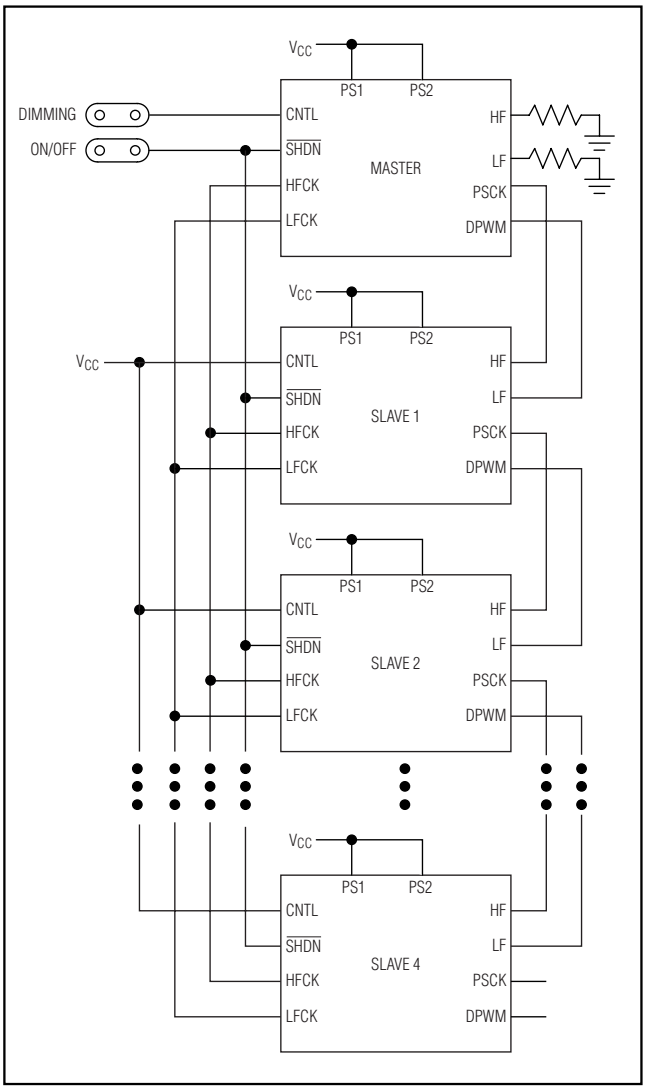

Figure 6. Daisy-Chain Operation of Five Controllers

During the delay period, the current-control loop tries to maintain the lamp-current regulation by increasing the high-side MOSFET on-time. Because the lamp impedance is very high when it is open, the transformer secondary rises as a result of the high-Q factor of the resonant tank. Once the secondary voltage exceeds the overvoltage threshold, the MAX8729 turns on a 1.2mA current source that discharges the COMP capacitor. The on-time of the high-side MOSFET is reduced, lowering the secondary voltage, as the COMP voltage decreases. Therefore, the peak voltage of the transformer secondary winding never exceeds the limit during the lamp-out delay period.

Primary Overcurrent Protection

The MAX8729 provides cycle-by-cycle primary overcurrent protection. A current-sense amplifier monitors the drain-to-source voltages of both the high-side and low-side switches when the switches are conducting. If the voltage exceeds the internal current-limit threshold (400mV typ), the regulator turns off the high-side switch at the opposite side of the primary to prevent the transformer primary current from increasing further.

Secondary Current Limit (ISEC)

The secondary current limit provides fail-safe protection in case of short-circuit or leakage from the transformer's high-voltage terminal to ground. ISEC monitors the voltage across a sense resistor placed between the transformer's low-voltage secondary terminal and ground. The ISEC voltage is internally half-wave rectified and continuously compared to the ISEC regulation threshold (1.25V, typ). Any time the ISEC voltage exceeds the threshold, a controlled current is drawn from COMP to reduce the on-time of the bridge's high-side switches. At the same time, the MAX8729 charges the TFLT capacitor with a 126µA current. The MAX8729 latches off when the voltage on TFLT exceeds 4V. Unlike the normal shutdown mode, the linear regulator output (V_{CC}) remains at 5.3V. Toggling $\overline{SHDN}$ or cycling the input power reactivates the device.

Synchronization in Daisy-Chain Operation (HFCK, LFCK, PSCK, DPWM)

The MAX8729 supports daisy-chain operation to allow synchronization and phase shift of multiple MAX8729s. Up to five MAX8729s can be connected in a daisy-chain configuration shown in Figure 6. Connecting CNTL to V_{CC} enables the daisy-chain operation and puts the IC in slave mode.

To synchronize the switching frequency, connect the HFCK pins of the slave IC and master IC together, and connect the PSCK pin of the master IC to the HF pin of

Table 1 Phase Shift Setting

PIN SETTING		PHASE SHIFT IN DEGREES					NO. OF PHASES
PS2	PS1	MASTER	SLAVE 1	SLAVE 2	SLAVE 3	SLAVE 4	
X	X	0	N/A	N/A	N/A	N/A	1
GND	GND	0	180	N/A	N/A	NA	2
GND	V_{CC}	0	120	240	N/A	N/A	3
V_{CC}	GND	0	90	180	270	N/A	4
V_{CC}	V_{CC}	0	72	144	216	288	5

X = Don't care.

the slave IC. To synchronize the DPWM frequency, connect the LFCK pins of the slave IC and master IC together, and connect the DPWM pin of the master IC to the LF pin of the slave IC. The CNTL brightness control is disabled in the slave mode. The master directly controls the brightness setting of the slave by providing a dimming signal on its DPWM pin.

Phase Shift in Daisy-Chain Operation (PS1, PS2)

The MAX8729 has the capability to adjust the phase of the gate drivers and the DPWM oscillator. The phase-shift function significantly reduces the input RMS ripple current and lowers the input capacitor requirement. The phase shift can be easily programmed using two logic input pins (PS1 and PS2). These two pins combined together give four choices of phase shift: 72°, 90°, 120°, and 180°. The selection of the phase shift is based on the number of MAX8729s used in the daisy-chain.

Table 1 gives the suggested selection of phase shift for 1, 2, 3, 4, and 5 phases. For a given multiphase circuit, all master and slave ICs should use the same setting for PS1, PS2.

Table 2 summarizes the MAX8729's operation in all modes.

Linear Regulator Output (V_{CC})

The internal linear regulator steps down the DC input voltage to 5.35V (typ). The linear regulator supplies power to the internal control circuitry of the MAX8729. V_{CC} can be used to power the MOSFET gate drivers by connecting it to V_{DD}. V_{DD} can also be driven from an external supply. The V_{CC} voltage drops to 4.5V in shutdown.

UVLO

The MAX8729 includes an undervoltage lockout (UVLO) circuit. The UVLO circuit monitors the V_{CC} voltage. When V_{CC} is below 4.2V (typ), the MAX8729 disables both high-side and low-side gate drivers and resets the fault latch.

Low-Power Shutdown

When the MAX8729 is placed in shutdown, all functions of the IC are turned off except for the 5.3V linear regulator. In shutdown, the linear regulator output voltage drops to about 4.5V and the supply current is 6µA (typ). While in shutdown, the fault latch is reset. The device can be placed into shutdown by pulling $\overline{SHDN}$ to its logic low level.

Table 2. Operation Summary

PIN NAME	MASTER MODE USING INTERNAL OSCILLATORS	MASTER MODE USING EXTERNAL SYNC SIGNAL (SYNC ONLY)	MASTER MODE USING EXTERNAL SYNC SIGNAL (SYNC AND DIMMING)	SLAVE MODE
CNTL	An analog voltage on CNTL sets the brightness.	An analog voltage on CNTL sets the brightness.	CNTL control is disabled. The external signal controls the brightness. Connect CNTL to an analog voltage in case the external sync signal is lost.	Connect CNTL to V_{CC}. Brightness is controlled by the master.
SEL	Connect SEL to GND.	Connect SEL to GND.	Connect SEL to V_{CC}.	Don't care.
HF	Connect a resistor to GND to set the switching frequency.	Switching frequency is controlled by the external sync signal. Connect a resistor to GND in case the external sync signal is lost.	Switching frequency is controlled by the external sync signal. Connect a resistor to GND in case the external sync signal is lost.	Connect to the PSCK pin of its master controller.
LF	Connect a resistor to GND to set DPWM frequency.	DPWM frequency is determined by the external sync signal. Connect a resistor to GND in case the external sync signal is lost.	DPWM frequency is determined by the external sync signal. Connect a resistor to GND in case the external sync signal is lost.	Connect to the DPWM pin of its master controller.
HFCK	Connect to the HFCK pin of its slave controller.	Connect to the HFCK pin of its slave controller.	Connect to the HFCK pin of its slave controller.	Connect to the HFCK pin of its master controller. Connect a 1MΩ resistor to GND.
LFCK	Connect to the LFCK pin of its slave controller.	Connect to the LFCK pin of its slave controller.	Connect to the LFCK pin of its slave controller.	Connect to the LFCK pin of its master controller. Connect a 1MΩ resistor to GND.
HSYNC	Not used. Connect to GND.	Connect to a high-frequency external signal to sync the switching frequency.	Connect to a high-frequency external signal to sync the switching frequency.	Not used. Connect to GND.
LSYNC	Not used. Connect to GND.	Connect a low-frequency external signal to sync the digital PWM frequency.	Connect a low-frequency external signal to sync the digital PWM frequency. The duty cycle of the external signal determines the brightness.	Not used. Connect to GND.
PSCK	Connect to the HF pin of its slave controller.	Connect to the HF pin of its slave controller.	Connect to the HF pin of its slave controller.	Connect to the HF pin of its slave controller.
DPWM	Connect to the LF pin of its slave controller.	Connect to the LF pin of its slave controller.	Connect to the LF pin of its slave controller.	Connect to the LF pin of its slave controller.

Applications Information

MOSFETs

The MAX8729 requires two external n-channel power MOSFETs to form a half-bridge inverter circuit to drive the transformer primary. Since the positive half-cycle and negative half-cycle are symmetrical, the same type of MOSFET should be used for the high-side and low-side switches. When selecting the MOSFET, focus on the voltage rating, current rating, on-resistance ($R_{DS(ON)}$), total gate charge, and power dissipation.

Select a MOSFET with a voltage rating at least 25% higher than the maximum input voltage of the inverter. For example, if the maximum input voltage is 24V, the voltage rating of the MOSFET should be 30V or higher. The current rating of the MOSFET should be higher than the peak primary current at the minimum input voltage and full brightness. Use the following equation to estimate the primary peak current I_{PEAK_PRI}:

$$I_{PEAK\_PI} = \frac{\sqrt{2} \times P_{OUT\_MAX}}{V_{IN\_MIN} \times \eta}$$

where P_{OUT_MAX} is the maximum output power, V_{IN_MIN} is the minimum input voltage, and is the estimated efficiency at the minimum input voltage. Assuming the half bridge drives four CCFLs and the maximum output power of each lamp is 4.5W, the total maximum output power is 18W. If the minimum input voltage is 8V and the estimated efficiency is 75% at that input, the peak primary current is approximately 4.3A. Therefore, power MOSFETs with a DC current rating of 5A or greater are sufficient.

Since the regulator senses the on-state, drain-to-source voltage of both MOSFETs to detect the transformer primary current, the lower the MOSFET $R_{DS(ON)}$, the higher the current limit is. Therefore, the user should select n-channel MOSFETs with low $R_{DS(ON)}$ to minimize conduction loss, and keep the primary current limit at a reasonable level. Use the following equation to estimate the maximum and minimum values of the primary current limit:

$$I_{LIM\_MIN} = \frac{320mV}{R_{DS(ON)\_MAX}}$$

$$I_{LIM\_MAX} = \frac{480mV}{R_{DS(ON)\_MIN}}$$

Both MOSFETs must be able to dissipate the conduction losses plus the switching losses at both V_{IN_MIN} and V_{IN_MAX}. Calculate both terms. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of the MOSFETs. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider choosing MOSFETs with lower parasitic capacitance. If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the conduction losses equal the switching losses.

Calculate the total conduction power dissipation of the two MOSFETs using the following equation:

$$PD_{CONDUCT} = I_{PRI}^2 \times R_{DS(ON)}$$

where I_{PRI} is the primary current calculated using the following equation:

$$I_{PRI} = \frac{P_{OUT\_MAX}}{\eta \times V_{IN}}$$

Both MOSFETs turn on with ZVS condition, so there is no switching power dissipation associated with the MOSFET. However, the current is at peak when the MOSFET is turned off. Calculate the total turn-off switching power dissipation of the two MOSFETs using the following equation:

$$PD_{SWITCH} = \frac{\sqrt{2} \times C_{RSS} \times V_{IN}^2 \times f_{SW} \times I_{PRI}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of the MOSFETs and I_{GATE} is the peak gate-drive sink current when the MOSFET is being turned off.

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Setting the Lamp Current

The MAX8729 senses the lamp current flowing through resistor R1 (Figure 1) connected between the low-voltage terminal of the lamp and ground. The voltage across R1 is fed to IFB and is internally full-wave rectified. The MAX8729 controls the desired lamp current by regulating the average of the rectified IFB voltage. To set the RMS lamp current, determine R1 as follows:

$$R1 = \frac{\pi \times 790mV}{2\sqrt{2} \times I_{LAMP(RMS)}}$$

where $I_{LAMP(RMS)}$ is the desired RMS lamp current and 790mV is the typical value of the IFB regulation point specified in the *Electrical Characteristics* table. To set the RMS lamp current to 6mA, the value of R1 should be 148Ω. The closest standard 1% resistors are 147Ω and 150Ω. The precise shape of the lamp-current waveform depends on lamp parasitics. The resulting waveform is an imperfect sinusoid waveform, which has an RMS value that is not easy to predict. A high-frequency true RMS current meter (such as Yokogawa 2016) should be used to measure the RMS current and make final adjustments to R1. Insert this meter between the sense resistor and the lamp's low-voltage terminal to measure the actual RMS current.

Setting the Secondary Voltage Limit

The MAX8729 limits the transformer secondary voltage during startup and lamp-out faults. The secondary voltage is sensed through the capacitive voltage-divider formed by C3 and C4 (Figure 1). The voltage of VFB is proportional to the CCFL voltage. The selection of parallel resonant capacitor C3 is described in the *Transformer Design and Resonant-Component Selection* section. Smaller values for C3 result in higher efficiency due to lower circulating current. If C3 is too small, the resonant operation is affected by the panel parasitic capacitance. Therefore, C3 is usually chosen to be between 10pF and 18pF. After the value of C3 is set, select C4 based on the desired maximum RMS secondary voltage $V_{LAMP(RMS)\_MAX}$:

$$C4 = \frac{\sqrt{2} \times V_{LAMP(RMS)\_MAX}}{2.34V} \times C3$$

where the 2.34V is the typical value of the VFB peak-voltage when the lamp is open. To set the maximum RMS secondary voltage to 1800V with C3 selected to be 12pF, C4 must be less than or equal to 13nF.

Setting the Secondary Current Limit

The MAX8729 limits the secondary current even if the IFB sense resistor is shorted or transformer secondary current finds its way to ground without passing through R1. ISEC monitors the voltage across the sense resistor R2 connected between the low-voltage terminal of the transformer secondary winding and ground. Determine the value of R2 using the following equation:

$$R2 = \frac{1.28V}{\sqrt{2} \times I_{SEC(RMS)\_MAX}}$$

where $I_{SEC(RMS)\_MAX}$ is the desired maximum RMS transformer secondary current during fault conditions, and 1.28V is the typical value of the ISEC peak voltage when the secondary is shorted. To set the maximum RMS secondary current in the circuit of Figure 1 to 22mA, set R3 = 40.2Ω.

Transformer Design and Resonant-Component Selection

The transformer is the most important component of the resonant tank circuit. The first step in designing the transformer is to determine the transformer turns ratio. The ratio must be high enough to support the CCFL operating voltage at the minimum supply voltage. The transformer turns ratio N can be calculated as follows:

$$N \geq \frac{V_{LAMP(RMS)}}{0.45 \times V_{IN(MIN)}}$$

where $V_{LAMP(RMS)}$ is the maximum RMS lamp voltage in normal operation, and $V_{IN(MIN)}$ is the minimum DC input voltage. If the maximum RMS lamp voltage in normal operation is 800V and the minimum DC input voltage is 10V, the turns ratio should be greater than 178.

The next step in the procedure is to design the resonant tank so the resonant frequency is close to the switching frequency set by the HF resistor. The lamp current is closer to sine wave when the switching frequency is close to the resonant frequency The resonant frequency is determined by: the primary capacitive voltage-divider C_{S1} and C_{S2}, the secondary parallel capacitor C_P, the transformer secondary leakage inductance L, and the CCFL lamp. The simplified CCFL inverter circuit is shown in Figure 7a. The half-bridge power stage is simplified and represented as a square-wave AC source. The resonant tank circuit can be further simplified to Figure 7b by removing the transformer. C_S' is the capacitance of the primary capacitive divider reflected to the secondary and N is the transformer turns ratio.

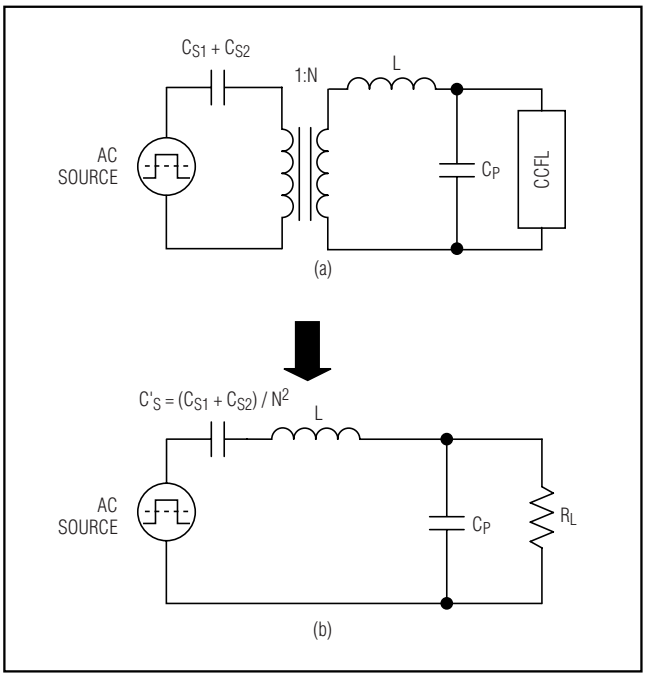

Figure 7. Simplified CCFL Inverter Circuit

Figure 8 shows the frequency response of the resonant tank's voltage gain under different load conditions. The primary series capacitor is 1µF, the secondary parallel capacitor is 15pF, the transformer turns ratio is 1:78, and the secondary leakage inductance is 260mH. Notice that there are two peaks, f_S and f_P, in the frequency response. The first peak, f_S, is the series resonant peak determined by the secondary leakage inductance (L) and the series capacitor reflected to the secondary (C'_S):

$$f_S = \frac{1}{2\pi\sqrt{LC'_S}}$$

The second peak, f_P, is the parallel resonant peak determined by the secondary leakage inductance (L), the parallel capacitor (C_P), and the series capacitor reflected to the secondary (C'_S):

$$f_P = \frac{1}{2\pi\sqrt{L\frac{C'_S C_P}{C'_S + C_P}}}$$

The actual resonant frequency is between these two resonant peaks. When the lamp is off, the operating point of the resonant tank is close to the parallel resonant peak due to the lamp's infinite impedance. The circuit displays the characteristics of a parallel-loaded resonant converter. While in parallel-loaded resonant operation, the inverter behaves like a voltage source to generate the necessary striking voltage. Theoretically, the output voltage of the resonant converter increases until the lamp is ionized or until it reaches the IC's secondary voltage limit. Once the lamp is ionized, the equivalent-load resistance decreases rapidly and the operating point moves toward the series-resonant peak. While in series-resonant operation, the inverter behaves like a current source.

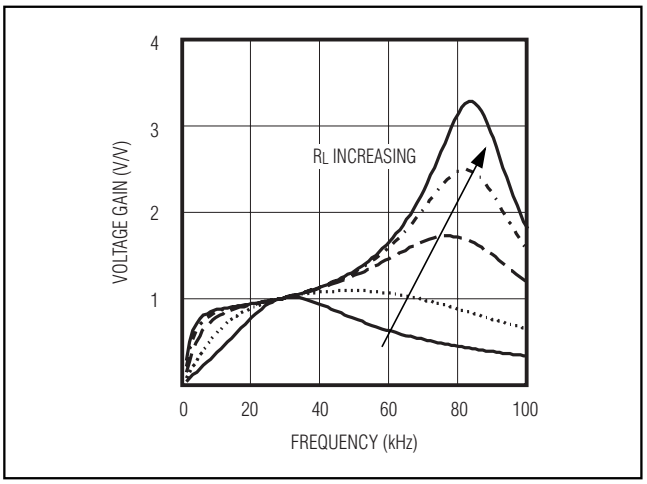

Figure 8. Frequency Response of the Resonant Tank

The leakage inductance of the CCFL transformer is an important parameter in the resonant tank design. The leakage inductance values can have large tolerance and significant variations among different batches. It is best to work directly with transformer vendors on leakage inductance requirements. The MAX8729 works best when the secondary leakage inductance is between 200mH and 350mH. The primary capacitive dividers C1 and C2 set the minimum operating frequency, which is approximately two times the series-resonant peak frequency. Choose:

$$C1 = C2 \le \frac{N^2}{8\pi^2 \times f^2_{MIN} \times L}$$

where f_{MIN} is the minimum operating frequency range. In the circuit of Figure 1, the transformer's turns ratio is 178 and its secondary leakage inductance is about 300mH. To set the minimum resonant frequency to 40kHz, use a capacitor of 2.2µF or less for C1 and C2.

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Parallel capacitor C3 sets the maximum operating frequency, which is also the parallel-resonant peak frequency. Choose:

$$C3 \le \frac{C1 + C2}{4\pi^2 \times f^2_{MAX} \times L \times C_S - N^2}$$

In the circuit of Figure 1, the maximum resonant frequency is 70kHz, C1 and C2 are 2.2µF, and the secondary leakage inductance is 300mH. Therefore, use a capacitor of 12pF or greater for C3.

The transformer core saturation should also be considered when selecting the operating frequency. The primary winding should have enough turns to prevent transformer saturation under all operating conditions. Use the following expression to calculate the minimum number of turns N1 of the primary winding:

$$N1 > \frac{D_{MAX} \times V_{IN(MAX)}}{B_S \times A \times f_{MIN}}$$

where D_{MAX} is the maximum duty cycle (approximately 0.8) of the high-side switch, $V_{IN(MAX)}$ is the maximum DC input voltage, B_S is the saturation flux density of the core, and A is the minimal cross-section area of the core.

COMP Capacitor Selection

The COMP capacitor sets the speed of the current-regulation loop that is used during startup, maintaining lamp-current regulation, and during transients caused by changing the input voltage. To maintain stable operation, the COMP capacitor (C_{COMP}) needs to be at least 3.3nF.

As discussed in the *Digital PWM Dimming Control* section, the COMP capacitor also limits the dynamics of the lamp-current envelope in digital PWM operation. At the end of the digital PWM ON cycle, the MAX8729 turns on a 100µA internal current source to linearly discharge the COMP capacitor. Use the following equation to set the fall time:

$$C_{COMP} = \frac{100\mu A \times t_{FALL}}{1.5V}$$

where t_{FALL} is the fall time of the lamp-current envelope and 1.5V is the dynamic range of the COMP voltage. At the beginning of the digital PWM ON cycle, the COMP capacitor is charged by transconductance error amplifier, so the charge current is not constant. Because the average charge current is around 30µA, the rise time is about three times longer than the fall time.

Setting the Fault-Delay Time

The TFLT capacitor determines the delay time for both the open-lamp fault and secondary short-circuit fault. The MAX8729 charges the TFLT capacitor with a 1µA current source during an open-lamp fault and charges the TFLT capacitor with a 126µA current source during a secondary short-circuit fault. Therefore, the secondary short-circuit fault-delay time is approximately 100 times shorter than that of the pen-lamp fault. The MAX8729 sets the fault latch when the TFLT voltage reaches 4V. Use the following equations to calculate the open-lamp fault delay (T_{OPEN_LAMP}) and secondary short-circuit fault delay (T_{SEC_SHORT}):

$$T_{OPEN\_LAMP} = \frac{C_{TFLT} \times 4V}{1\mu A}$$

$$T_{SEC\_SHORT} = \frac{C_{TFLT} \times 4V}{126\mu A}$$

Bootstrap Capacitor

The high-side gate driver is powered using a bootstrap circuit. The MAX8729 integrates the bootstrap diode so only one 0.1µF bootstrap capacitor is needed. Connect the capacitor between LX and BST to complete the bootstrap circuit.

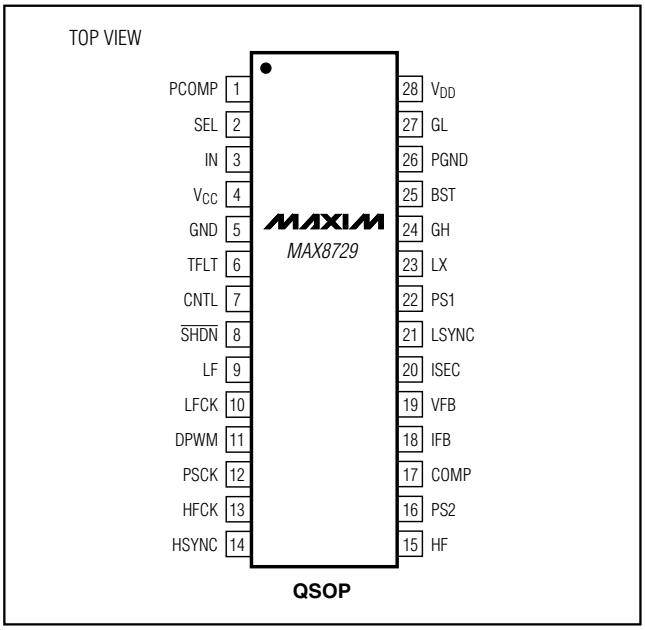
Layout Guidelines

Careful PC board layout is important to achieve stable operation. The high-voltage section and the switching section of the circuit require particular attention. The high-voltage sections of the layout need to be well separated from the control circuit. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short and wide, especially at the ground terminals. This is essential for stable, jitter-free operation and high efficiency.
2) Use a star-ground configuration for power and analog grounds. The power and analog grounds should be completely isolated—meeting only at the center of the star. The center should be placed at the analog ground pin (GND). Using separate copper islands for these grounds can simplify this task. Quiet analog ground is used for V_{CC}, COMP, HF, LF, and TFLT.

3) Route high-speed switching nodes away from sensitive analog areas (V_{CC}, COMP, HF, LF, and TFLT). Make all pin-strap control input connections to analog ground or V_{CC} rather than power ground or V_{DD}.
4) Mount the decoupling capacitor from V_{CC} to GND as close as possible to the IC with dedicated traces that are not shared with other signal paths.
5) The current-sense paths for LX to GND and IN to LX must be made using Kelvin-sense connections to guarantee the current-limit accuracy. With 8-pin SO MOSFETs, this is best done by routing power to the MOSFETs from the outside using the top copper layer, while connecting GND and LX inside (underneath) the 8-pin SO package.
6) Ensure the feedback connections are short and direct. To the extent possible, IFB, VFB, and ISEC connections should be far away from the high-voltage traces and the transformer.
7) To the extent possible, high-voltage trace clearance on the transformer's secondary should be widely separated. The high-voltage traces should also be separated from adjacent ground planes to prevent lossy capacitive coupling.
8) The traces to the capacitive voltage-divider on the transformer's secondary need to be widely separated to prevent arcing. Moving these traces to opposite sides of the board can be beneficial in some cases.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 7531

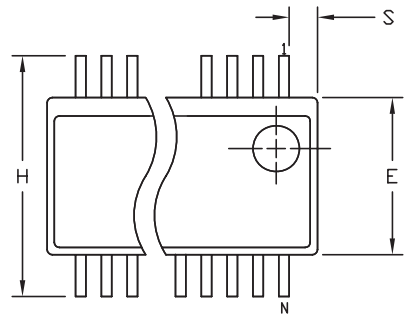
PROCESS: BiCMOS

Constant-Frequency, Half-Bridge CCFL Inverter Controller

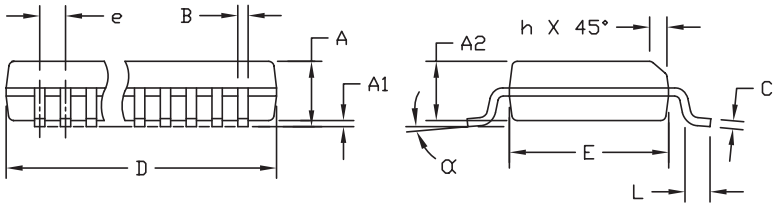
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1