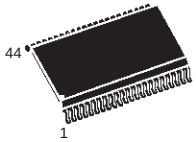
M68AW256DL

4 Mbit (256K x16) 3.0V Asynchronous SRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE: 2.7 to 3.6V
- 256K x 16 bits SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIME: 55ns
- SINGLE BYTE READ/WRITE
- LOW STANDBY CURRENT
- LOW V_{CC} DATA RETENTION: 1.5V
- TRI-STATE COMMON I/O
- AUTOMATIC POWER DOWN
- DUAL CHIP ENABLE for EASY DEPTH EXPANSION

Figure 1. Packages



TSOP44 Type II (ND)

TFBGA48 (ZB)
7 x 8 mm

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SUMMARY DESCRIPTION

The M68AW256DL is a 4 Mbit (4,194,304 bit) CMOS SRAM, organized as 262,144 words by 16 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 2.7 to 3.6V supply. This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68AW256DL is available in TFBGA48 (0.75 mm pitch) and in TSOP44 Type II packages.

Figure 2. Logic Diagram

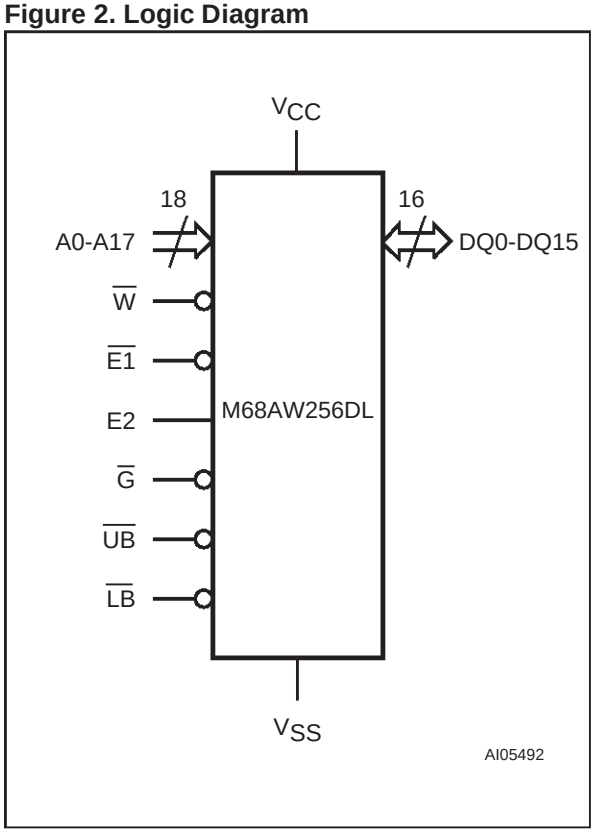


Table 1. Signal Names

A0-A17	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{E1}$, E2	Chip Enables
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Don't Use as Internally Connected

Figure 3. TSOP Connections

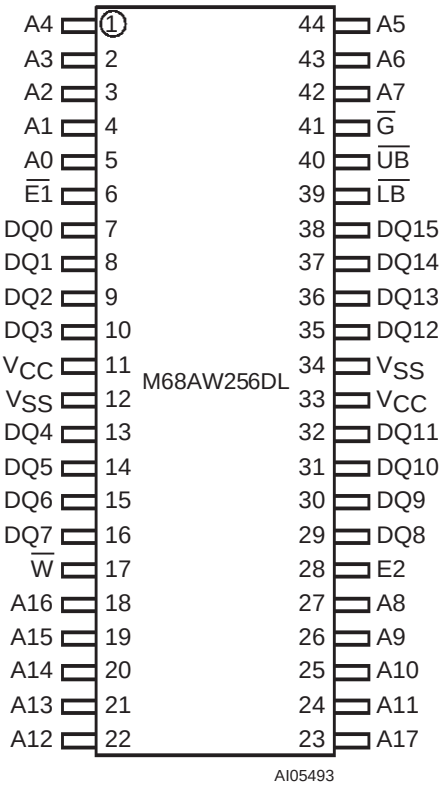


Figure 4. TFBGA Connections (Top view through package)

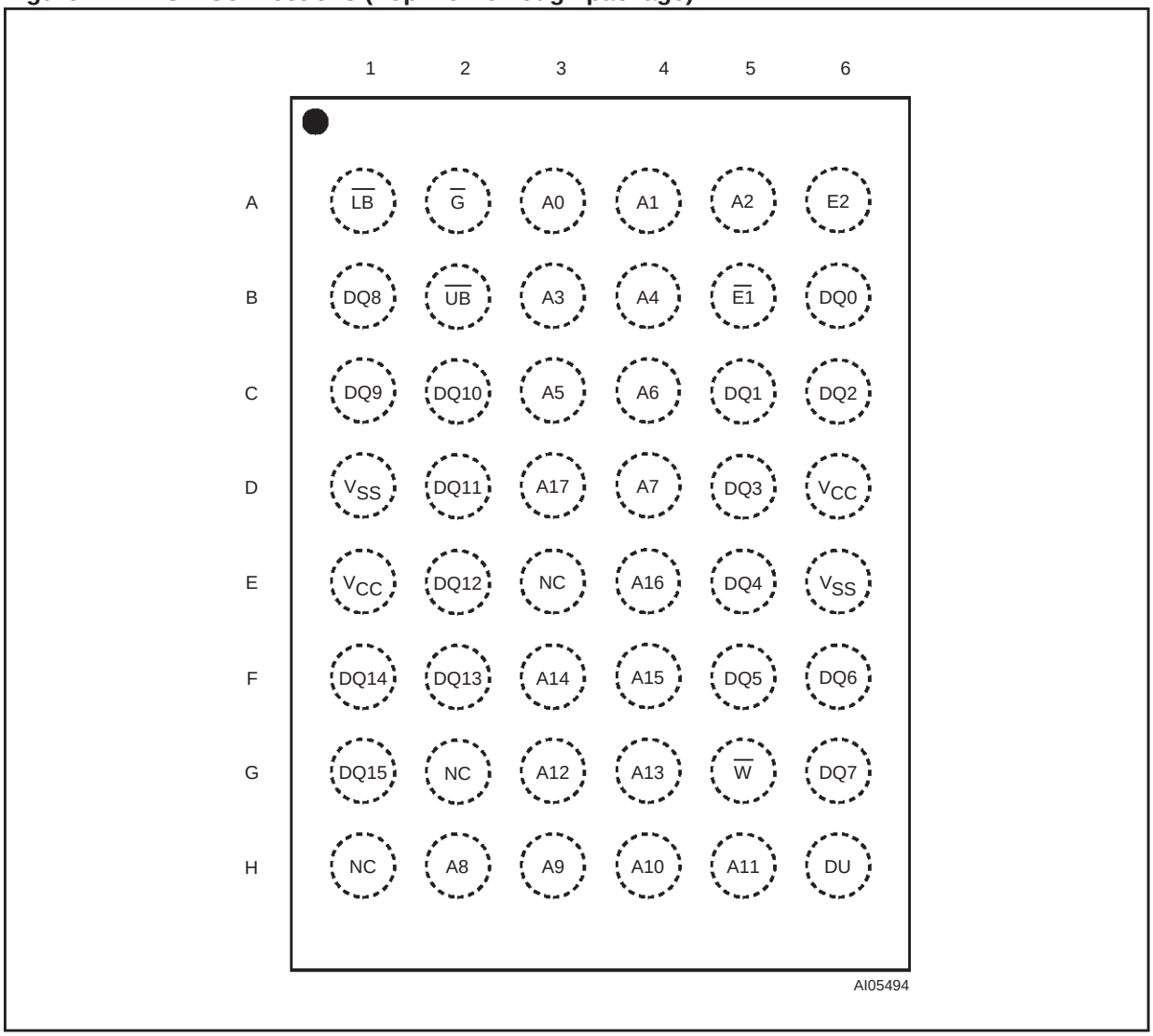
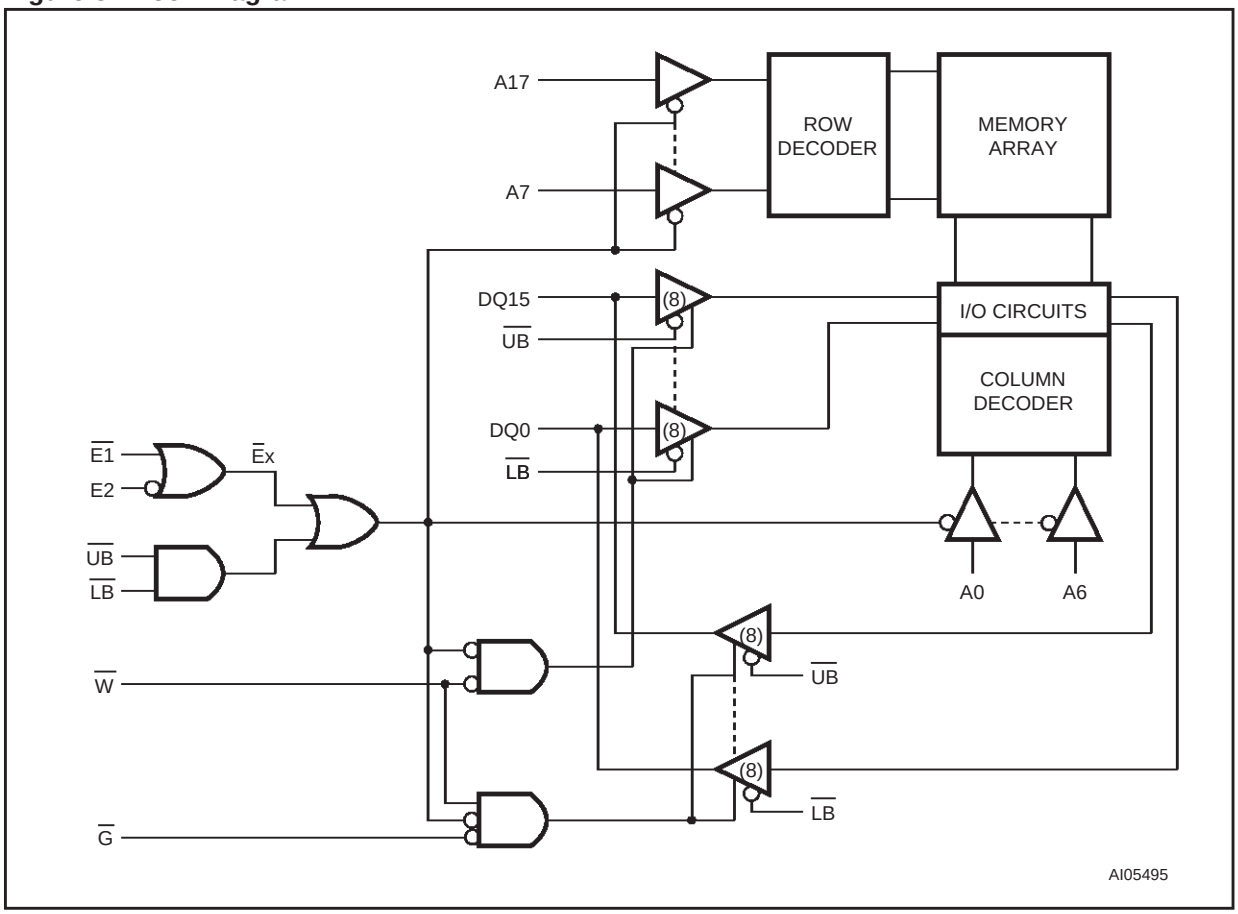


Figure 5. Block Diagram



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
I_O (1)	Output Current	20	mA
T_A	Ambient Operating Temperature	–55 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{CC}	Supply Voltage	–0.5 to 4.6	V
V_{IO} (2)	Input or Output Voltage	–0.5 to V_{CC} +0.5	V
P_D	Power Dissipation	1	W

Note: 1. One output at a time, not to exceed 1 second duration.
2. Up to a maximum operating V_{CC} of 3.6V only.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. Operating and AC Measurement Conditions

Parameter		M68AW256ML
V_{CC} Supply Voltage		2.7 to 3.6V
Ambient Operating Temperature	Range 1	0 to 70°C
	Range 6	–40 to 85°C
Load Capacitance (C_L)		30pF
Output Circuit Protection Resistance (R_1)		3.0kΩ
Load Resistance (R_2)		3.1kΩ
Input Rise and Fall Times		1ns/V
Input Pulse Voltages		0 to V_{CC}
Input and Output Timing Ref. Voltages		$V_{CC}/2$
Output Transition Timing Ref. Voltages		$V_{RL} = 0.3V_{CC}$; $V_{RH} = 0.7V_{CC}$

Figure 6. AC Measurement I/O Waveform

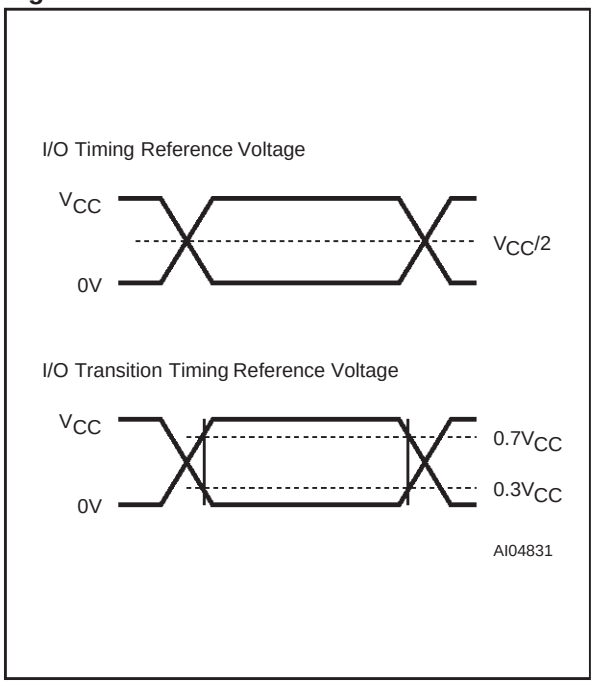


Figure 7. AC Measurement Load Circuit

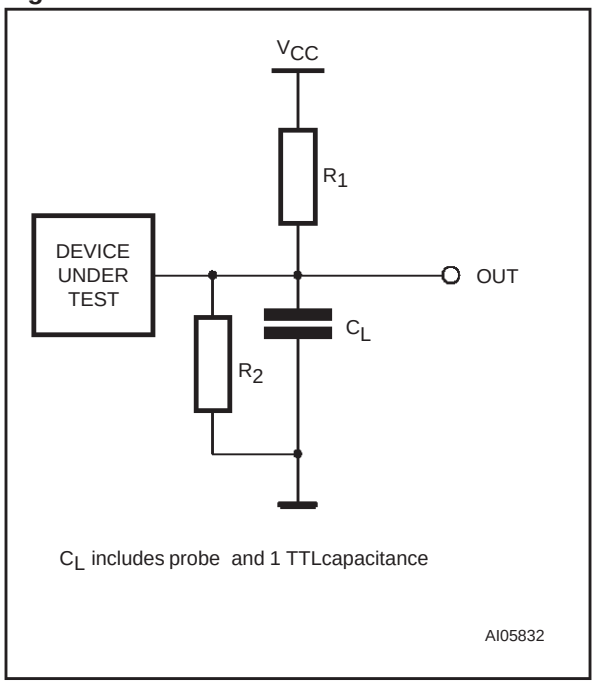


Table 4. Capacitance

Symbol	Parameter[1,2]	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		8	pF
C_{OUT}[3]	Output Capacitance	V_{OUT} = 0V		10	pF

Note: 1. Sampled only, not 100% tested.
2. At T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V.
3. Outputs deselected.

Table 5. DC Characteristics

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
I_{CC1} (1,2)	Operating Supply Current	V_{CC} = 3.6V, f = $1/t_{AVAV}$, I_{OUT} = 0mA	70ns			20	mA
			55ns			26	mA
I_{CC2} (3)	Operating Supply Current	V_{CC} = 3.6V, f = 1MHz, I_{OUT} = 0mA				2	mA
I_{SB}	Standby Supply Current CMOS	V_{CC} = 3.6V, f = 0, $\overline{E1} \geq V_{CC}$ –0.2V or E2 ≤ 0.2V or $\overline{LB}$=$\overline{UB} \geq V_{CC}$ –0.2V			5	10	µA
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		–1		1	µA
I_{LO} (4)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		–1		1	µA
V_{IH}	Input High Voltage			2.2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			–0.3		0.6	V
V_{OH}	Output High Voltage	I_{OH} = –1.0mA		2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA				0.4	V

Note: 1. Average AC current, cycling at t_{AVAV} minimum.
2. $\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{LB}$ or/and $\overline{UB}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH}.
3. $\overline{E1} \leq$ 0.2V or E2 ≥ V_{CC} –0.2V, $\overline{LB}$ or/and $\overline{UB} \leq$ 0.2V, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ –0.2V.
4. Output disabled.

OPERATION

The M68AW256DL has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E1}$ = High) or Chip Select is asserted (E2 = Low), or $\overline{UB}$/$\overline{LB}$ are de-asserted ($\overline{UB}$/$\overline{LB}$ = High). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{E1}$, $\overline{LB}$ and $\overline{UB}$ as summarized in the Operating Modes table (see Table 6).

Table 6. Operating Modes

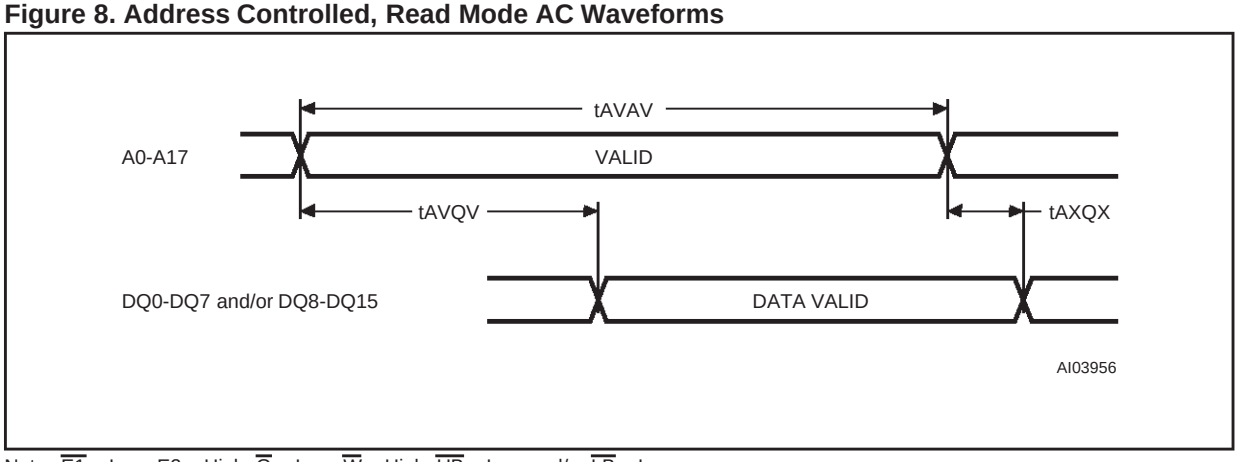
Operation	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	DQ0-DQ7	DQ8-DQ15	Power
Deselected	V_{IH}	X	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
Deselected	X	V_{IL}	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
Deselected	X	X	X	X	V_{IH}	V_{IH}	Hi-Z	Hi-Z	Standby (I_{SB})
Lower Byte Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Output	Hi-Z	Active (I_{CC})
Lower Byte Write	V_{IL}	V_{IH}	V_{IL}	X	V_{IL}	V_{IH}	Data Input	Hi-Z	Active (I_{CC})
Output Disabled	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z	Hi-Z	Active (I_{CC})
Upper Byte Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Hi-Z	Data Output	Active (I_{CC})
Upper Byte Write	V_{IL}	V_{IH}	V_{IL}	X	V_{IH}	V_{IL}	Hi-Z	Data Input	Active (I_{CC})
Word Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Data Output	Data Output	Active (I_{CC})
Word Write	V_{IL}	V_{IH}	V_{IL}	X	V_{IL}	V_{IL}	Data Input	Data Input	Active (I_{CC})

Note: X = V_{IH} or V_{IL}.

Read Mode

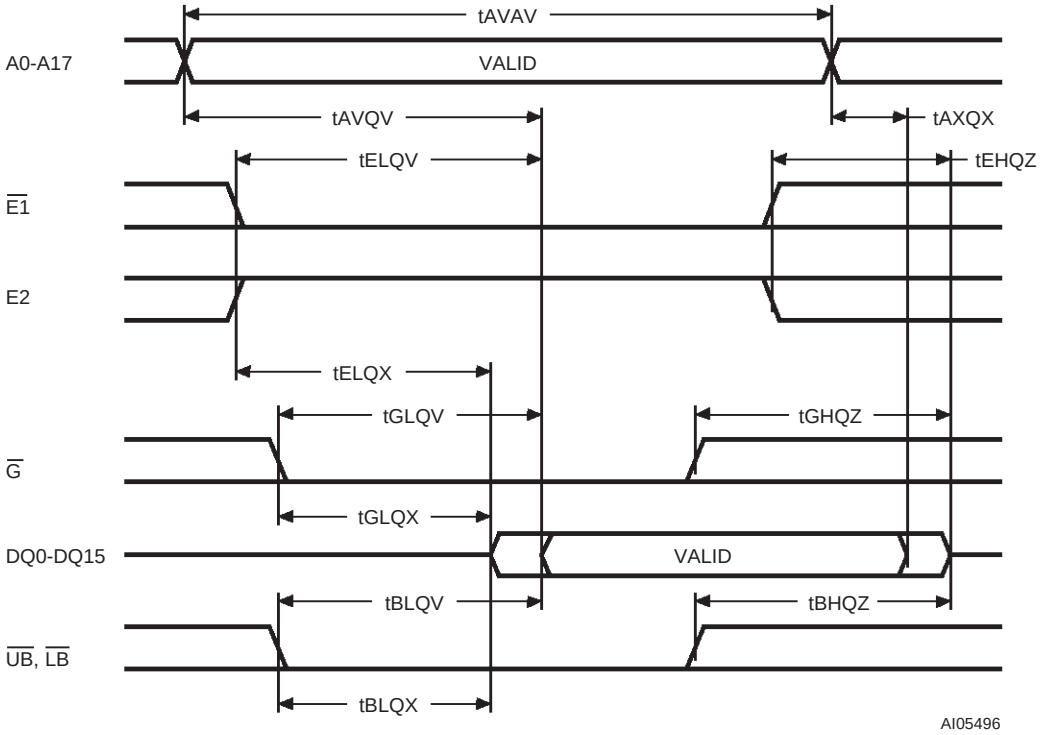
The M68AW256DL, when Chip Select (E2) is High, is in the read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and Chip Enable ($\overline{E1}$) is asserted. This provides access to data from eight or sixteen, depending on the status of the signal $\overline{UB}$ and $\overline{LB}$, of the 4,194,304 locations in the static memory array, specified by the 18 address inputs. Valid data will be available at the eight or sixteen output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low and $\overline{E1}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV}, t_{GLQV} or t_{BLQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, t_{GLQX} and t_{BLQX}, but data lines will always be valid at t_{AVQV}.

Figure 8. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E1}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{W}$ = High, $\overline{UB}$ = Low and/or $\overline{LB}$ = Low.

Figure 9. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms.



Note: Write Enable ($\overline{W}$) = High.

Figure 10. Chip Enable or $\overline{UB}$/$\overline{LB}$ Controlled, Standby Mode AC Waveforms

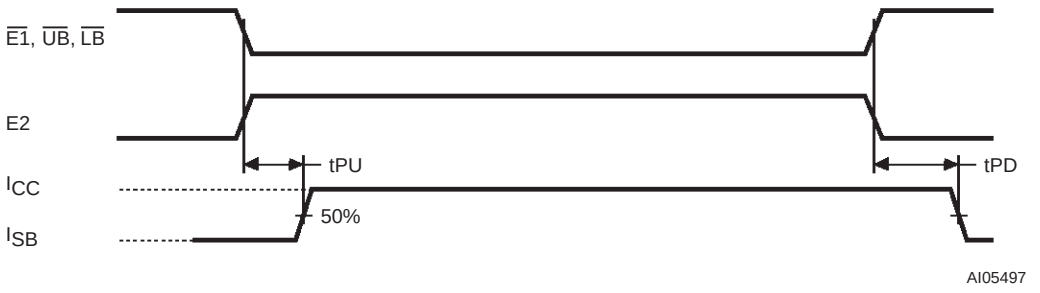


Table 7. Read and Standby Mode AC Characteristics

Symbol	Parameter		M68AW256DL		Unit
			55	70	
t_{AVAV}	Read Cycle Time	Min	55	70	ns
t_{AVQV}	Address Valid to Output Valid	Max	55	70	ns
t_{AXQX} (1)	Data hold from address change	Min	5	5	ns
t_{BHQZ} (2,3)	Upper/Lower Byte Enable High to Output Hi-Z	Max	20	25	ns
t_{BLQV}	Upper/Lower Byte Enable Low to Output Valid	Max	55	70	ns
t_{BLQX} (1)	Upper/Lower Byte Enable Low to Output Transition	Min	5	5	ns
t_{EHQZ} (2,3)	Chip Enable High to Output Hi-Z	Max	20	25	ns
t_{ELQV}	Chip Enable Low to Output Valid	Max	55	70	ns
t_{ELQX} (1)	Chip Enable Low to Output Transition	Min	5	5	ns
t_{GHQZ} (2,3)	Output Enable High to Output Hi-Z	Max	20	25	ns
t_{GLQV}	Output Enable Low to Output Valid	Max	25	35	ns
t_{GLQX} (2)	Output Enable Low to Output Transition	Min	5	5	ns
t_{PD} (4)	Chip Enable or $\overline{UB}$/$\overline{LB}$ High to Power Down	Max	0	0	ns
t_{PU} (4)	Chip Enable or $\overline{UB}$/$\overline{LB}$ Low to Power Up	Min	55	70	ns

Note: 1. Test conditions assume transition timing reference level = $0.3V_{CC}$ or $0.7V_{CC}$.
2. At any given temperature and voltage condition, t_{GHQZ} is less than t_{GLQX}, t_{BHQZ} is less than t_{BLQX} and t_{EHQZ} is less than t_{ELQX} for any given device.
3. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
4. Tested initially and after any design or process changes that may affect these parameters.

Write Mode

The M68AW256DL, when Chip Select (E2) is High, is in the Write Mode whenever the $\overline{W}$ and $\overline{E1}$ are Low. Either the Chip Enable Input ($\overline{E1}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. When $\overline{E1}$ or $\overline{W}$ is Low, and $\overline{UB}$ or $\overline{LB}$ is Low, write cycle begins on the $\overline{W}$ or $\overline{E1}$ falling edge. When $\overline{E1}$ and $\overline{W}$ are Low, and $\overline{UB}$ = $\overline{LB}$ = High, write cycle begins on the first falling edge of $\overline{UB}$ or $\overline{LB}$. Therefore, address setup time is referenced to Write Enable, Chip Enables and $\overline{UB}$/$\overline{LB}$ as t_{AVWL}, t_{AVEL} and t_{AVBL} respectively, and is determined by the latter occurring falling edge.

The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$, $\overline{W}$, $\overline{UB}$ and $\overline{LB}$.

If the Output is enabled ($\overline{E1}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{LB}$ or $\overline{UB}$ = Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E1}$ or for t_{DVBH} before the rising edge of $\overline{UB}$/$\overline{LB}$, whichever occurs first, and remain valid for t_{WHDX}, t_{EHDX} and t_{BHDX} respectively.

Figure 11. Write Enable Controlled, Write AC Waveforms

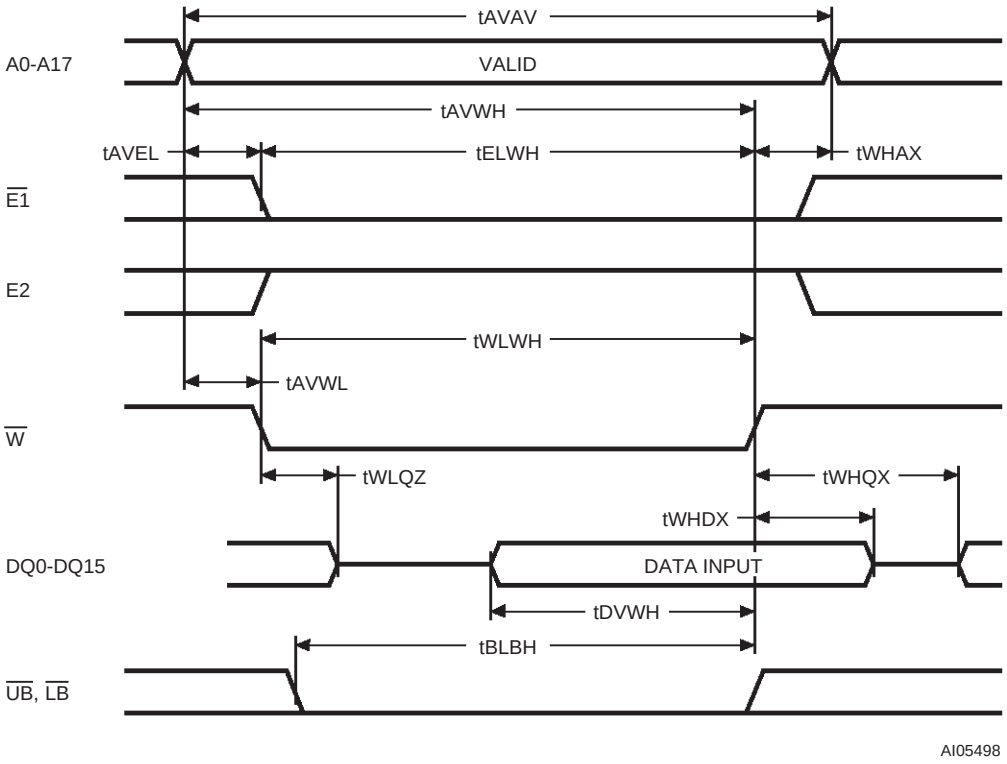


Figure 12. Chip Enable Controlled, Write AC Waveforms

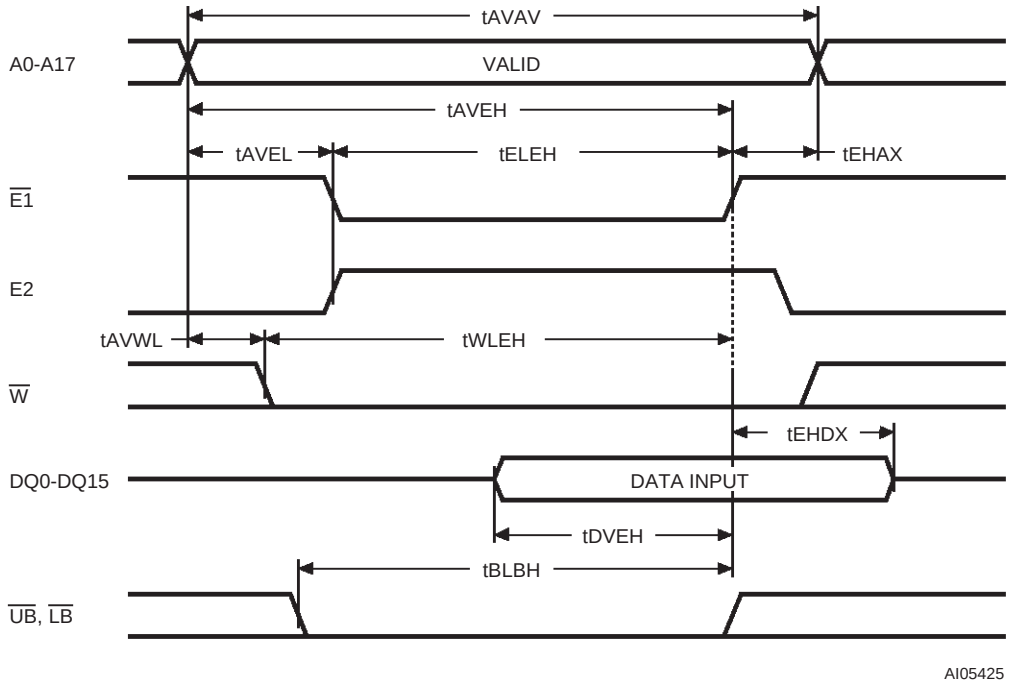
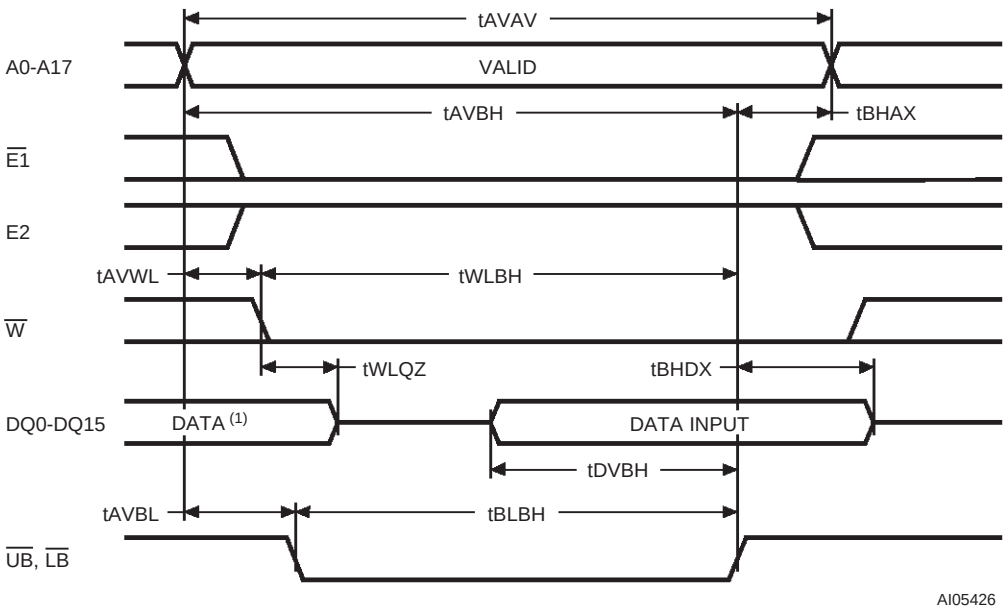


Figure 13. $\overline{UB}$/$\overline{LB}$ Controlled, Write AC Waveforms



Note: 1. During this period DQ0-DQ15 are in output state and input signals should not be applied.

Table 8. Write Mode AC Characteristics

Symbol	Parameter		M68AW256DL		Unit
			55	70	
t_{AVAV}	Write Cycle Time	Min	55	70	ns
t_{AVBH}	Address Valid to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns
t_{AVBL}	Addess Valid to $\overline{LB}$, $\overline{UB}$ Low	Min	0	0	ns
t_{AVEH}	Address Valid to Chip Enable High	Min	45	60	ns
t_{AVEL}	Address valid to Chip Enable Low	Min	0	0	ns
t_{AVWH}	Address Valid to Write Enable High	Min	45	60	ns
t_{AVWL}	Address Valid to Write Enable Low	Min	0	0	ns
t_{BHAX}	$\overline{LB}$, $\overline{UB}$ High to Address Transition	Min	0	0	ns
t_{BHDX}	$\overline{LB}$, $\overline{UB}$ High to Input Transition	Min	0	0	ns
t_{BLBH}	$\overline{LB}$, $\overline{UB}$ Low to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns
t_{BLEH}	$\overline{LB}$, $\overline{UB}$ Low to Chip Enable High	Min	45	60	ns
t_{BLWH}	$\overline{LB}$, $\overline{UB}$ Low to Write Enable High	Min	45	60	ns
t_{DVBH}	Input Valid to $\overline{LB}$, $\overline{UB}$ High	Min	25	30	ns
t_{DVEH}	Input Valid to Chip Enable High	Min	25	30	ns
t_{DVWH}	Input Valid to Write Enable High	Min	25	30	ns
t_{EHAX}	Chip Enable High to Address Transition	Min	0	0	ns
t_{EHDX}	Chip enable High to Input Transition	Min	0	0	ns
t_{ELBH}	Chip Enable Low to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns
t_{ELEH}	Chip Enable Low to Chip Enable High	Min	45	60	ns
t_{ELWH}	Chip Enable Low to Write Enable High	Min	45	60	ns
t_{WHAX}	Write Enable High to Address Transition	Min	0	0	ns
t_{WHDX}	Write Enable High to Input Transition	Min	0	0	ns
t_{WHQX} (1)	Write Enable High to Output Transition	Min	5	5	ns
t_{WLBH}	Write Enable Low to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns
t_{WLEH}	Write Enable Low to Chip Enable High	Min	45	60	ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z	Max	20	20	ns
t_{WLWH}	Write Enable Low to Write Enable High	Min	45	60	ns

Note: 1. At any given temperature and voltage condition, t_{WLQZ} is less than t_{WHQX} for any given device.
2. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 14. $\overline{E1}$ Controlled, Low V_{CC} Data Retention AC Waveforms

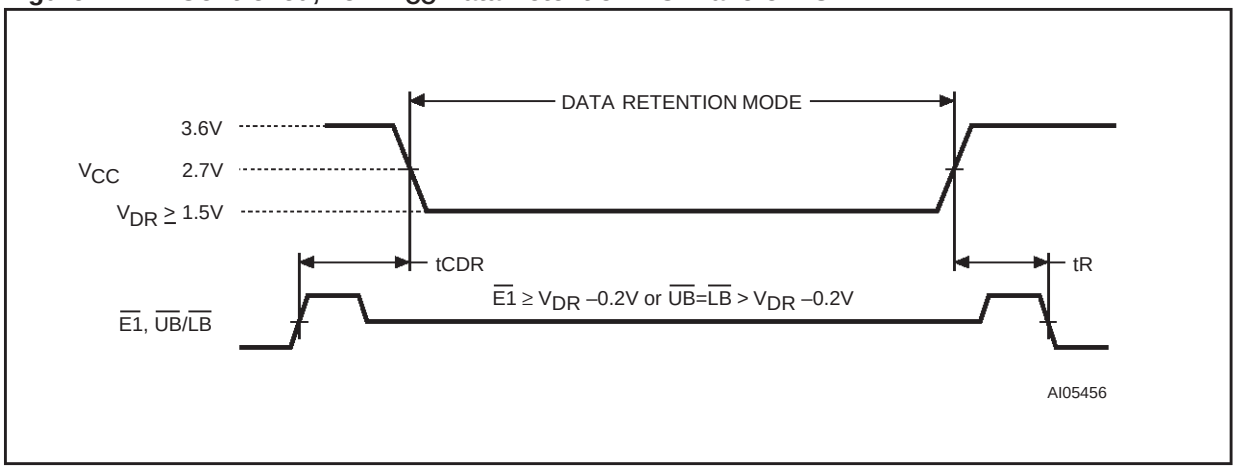


Figure 15. E2 Controlled, Low V_{CC} Data Retention AC Waveforms

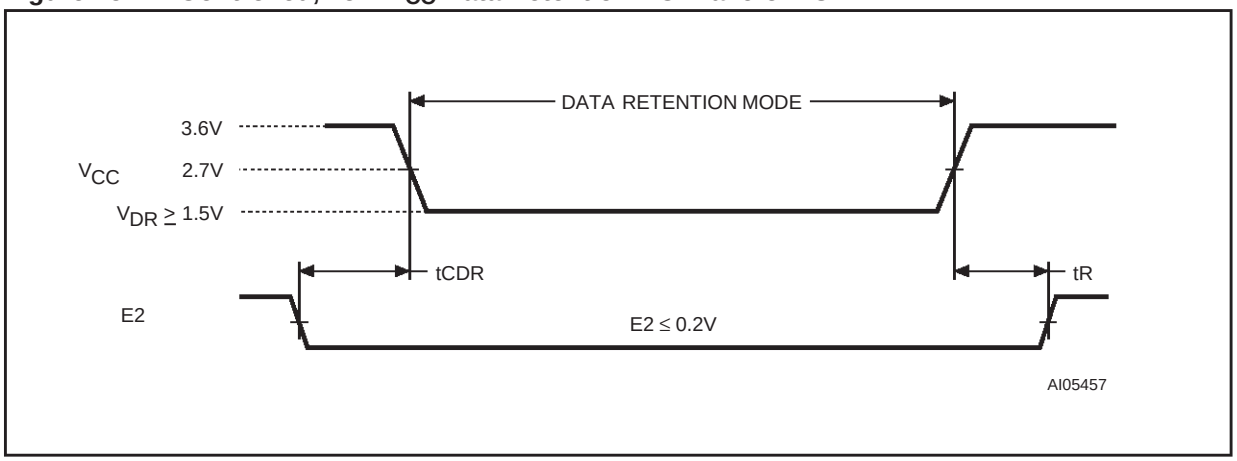


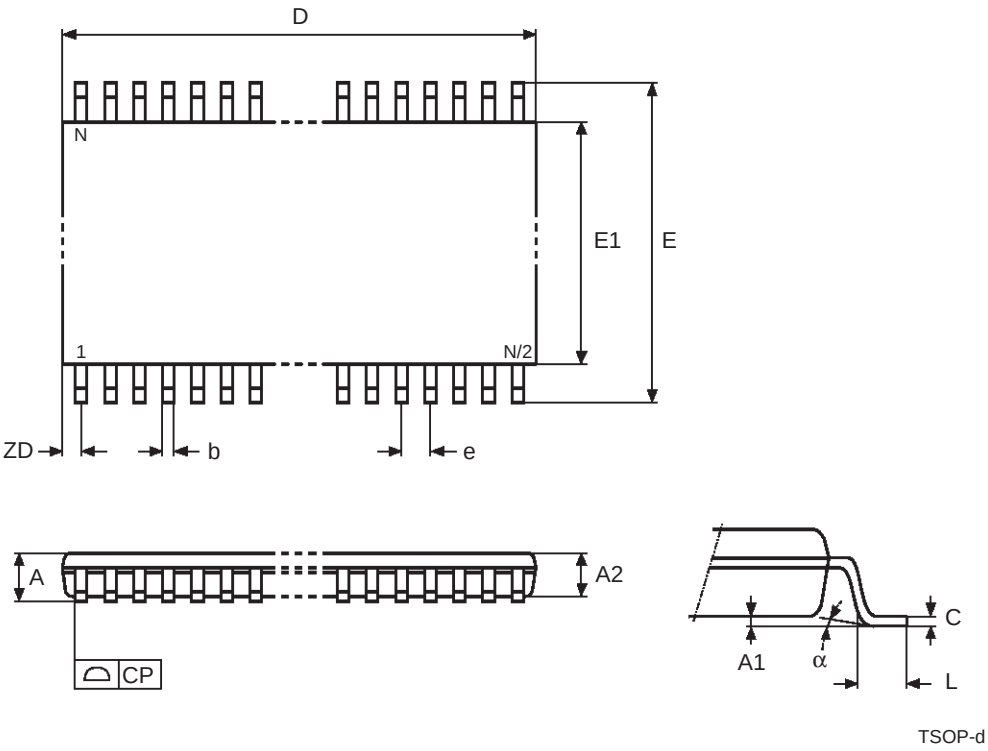
Table 9. Low V_{CC} Data Retention Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{CCDR} (1)	Supply Current (Data Retention)	V_{CC} = 1.5V, $\overline{E1} \geq V_{CC}$ –0.2V or E2 ≤ 0.2V or $\overline{UB}$ = $\overline{LB} \geq V_{CC}$ –0.2V, f = 0		4.5	9	µA
t_{CDR} (1,2)	Chip Deselected to Data Retention Time		0			ns
t_R (2)	Operation Recovery Time		t_{AVAV}			ns
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E1} \geq V_{CC}$ –0.2V or E2 ≤ 0.2V or $\overline{UB}$ = $\overline{LB} \geq V_{CC}$ –0.2V, f = 0	1.5			V

Note: 1. All other Inputs at $V_{IH} \geq V_{CC}$ –0.2V or $V_{IL} \leq$ 0.2V.
2. Tested initially and after any design or process changes that may affect these parameters. t_{AVAV} is Read cycle time.
3. No input may exceed V_{CC} +0.2V.

PACKAGE MECHANICAL

Figure 16. TSOP44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Outline

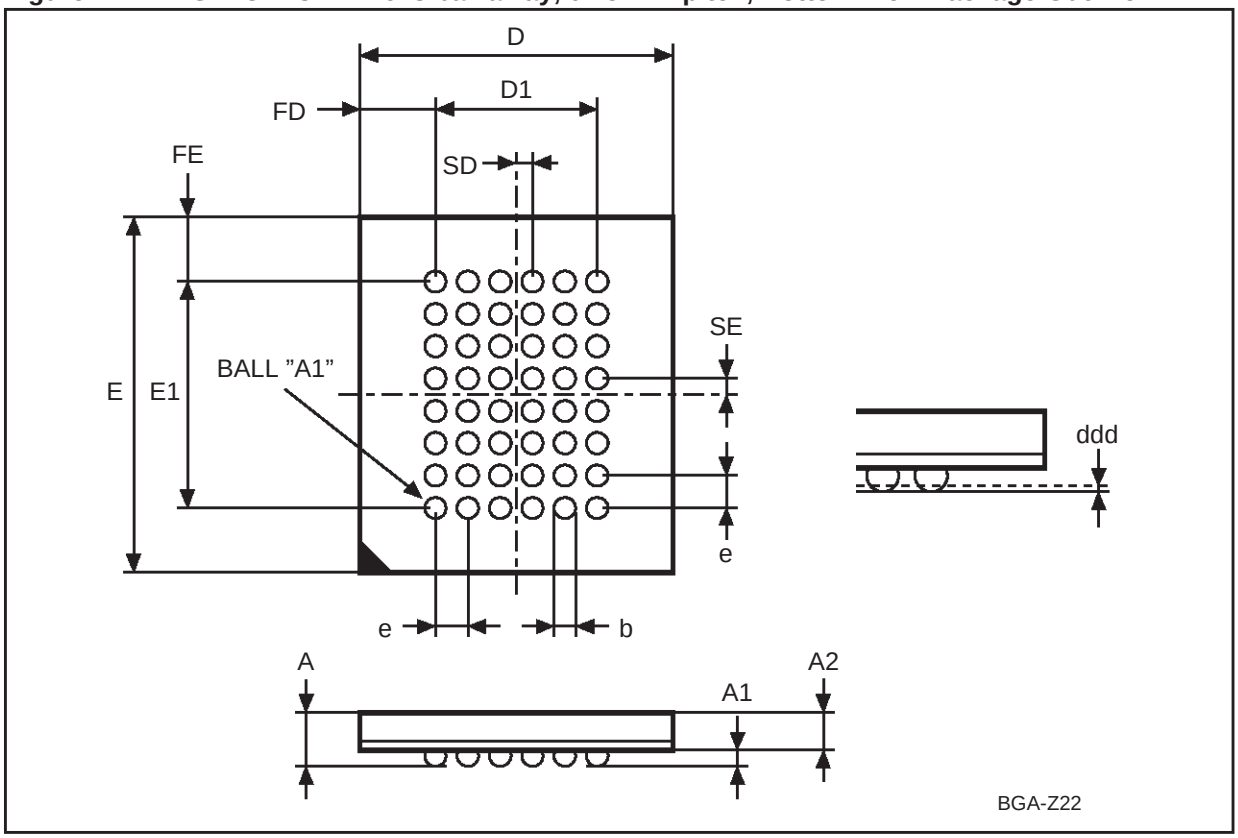


Note: Drawing is not to scale.

Table 10. TSOP 44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
b	0.350			0.0138		
c		0.120	0.210		0.0047	0.0083
D	18.410	–	–	0.7248	–	–
E	11.760	–	–	0.4630	–	–
E1	10.160	–	–	0.4000	–	–
e	0.800	–	–	0.0315	–	–
L	0.500	0.400	0.600	0.0197	0.0157	0.0236
ZD	0.805	–	–	0.0317	–	–
alfa		0	5		0	5
CP			0.100			0.0039
N	44			44		

Figure 17. TFBGA48 7x8mm - 6x8 ball array, 0.75 mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 11. TFBGA48 7x8mm - 6x8 ball array, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.010	1.200		0.0398	0.0472
A1		0.260			0.0102	
A2			0.950			0.0374
b	0.400	0.300	0.500	0.0157	0.0118	0.0197
D	7.000	6.900	7.100	0.2756	0.2717	0.2795
D1	3.750	–	–	0.1476	–	–
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.250	–	–	0.2067	–	–
e	0.750	–	–	0.0295	–	–
FD	1.625	–	–	0.0640	–	–
FE	1.375	–	–	0.0541	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

PART NUMBERING

Table 12. Ordering Information Scheme

Example: M68AW256 D L 55 ZB 6 T

Device Type
M68

Mode
A = Asynchronous

Operating Voltage
W = 2.7 to 3.6V

Array Organization
256 = 4 Mbit (256K x16)

Option 1
D = 2 Chip Enable; Write and Standby from $\overline{UB}$ and $\overline{LB}$

Option 2
L = Low Leakage

Speed Class
55 = 55 ns
70 = 70 ns

Package
ND = TSOP 44 Type II
ZB = TFBGA48: 0.75 mm pitch

Operative Temperature
1 = 0 to 70 °C
6 = –40 to 85 °C

Shipping
T = Tape & Reel Packing

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

REVISION HISTORY

Table 13. Document Revision History

Date	Version	Revision Details
February 2002	-01	First Issue
14-Mar-2002	-02	Tables 3, 5, 7 and 9 clarified Figures 3, 8, 9, 11, 12, 13 and 14 clarified
07-Jun-2002	-03	I_{CCDR} clarified (Table 9) I_{SB} clarified (Table 5)