

M5295AL/AP/AFP

Watchdog Timer

REJ03D0780-0200

Rev.2.00

Jun 15, 2007

Description

M5295A is a semiconductor integrated circuit which is designed for system reset to detect +5 V power supply.

This IC keeps the operation microcomputer watching. When the system is abnormal, it generates reset output until the system returns to normal states of the system.

It is possible to vary the two detective voltage by connecting the resistor, so it is suitable to high quality and high performance system.

Features

- Watchdog timer
- Power on reset timer
- Low circuit current: 0.8 mA (Typ, $V_{CC} = 5\text{ V}$)
- Wide supply voltage range: $V_{CC(max)} = 15\text{ V}$

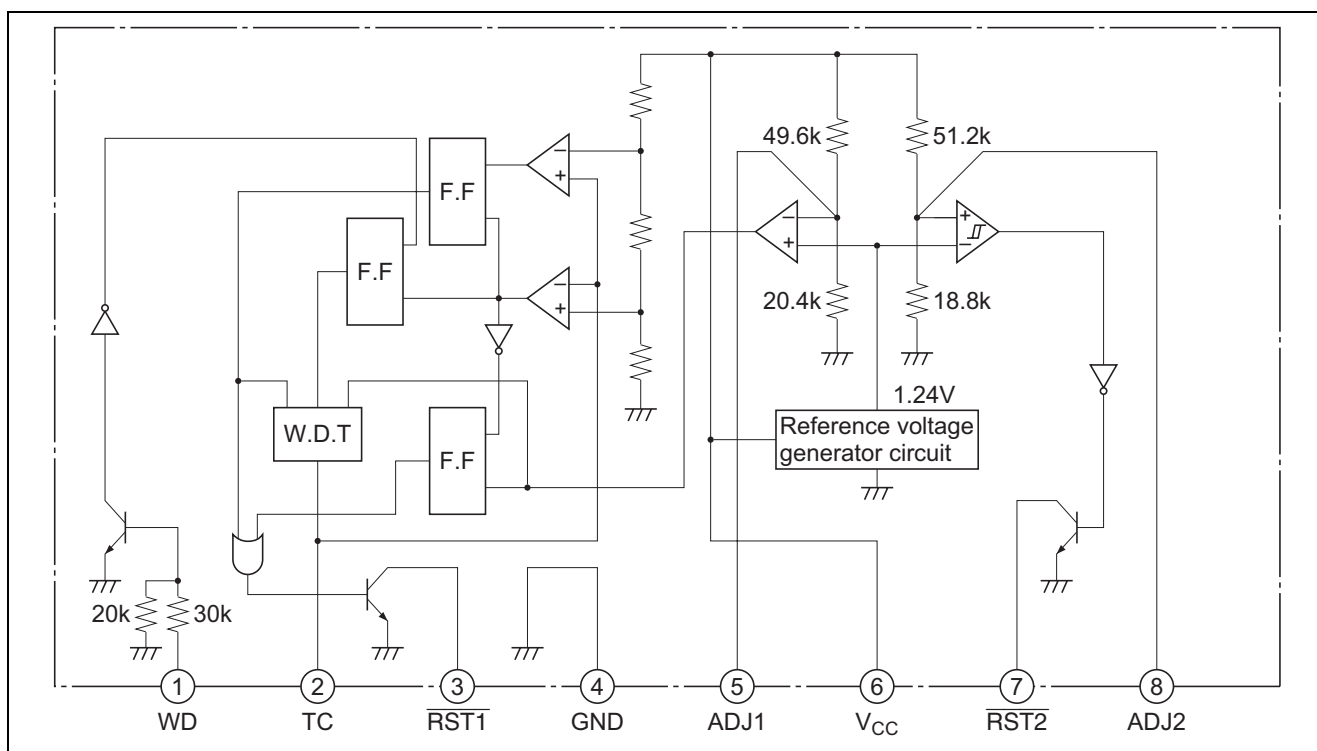
Application

- Microcomputer system

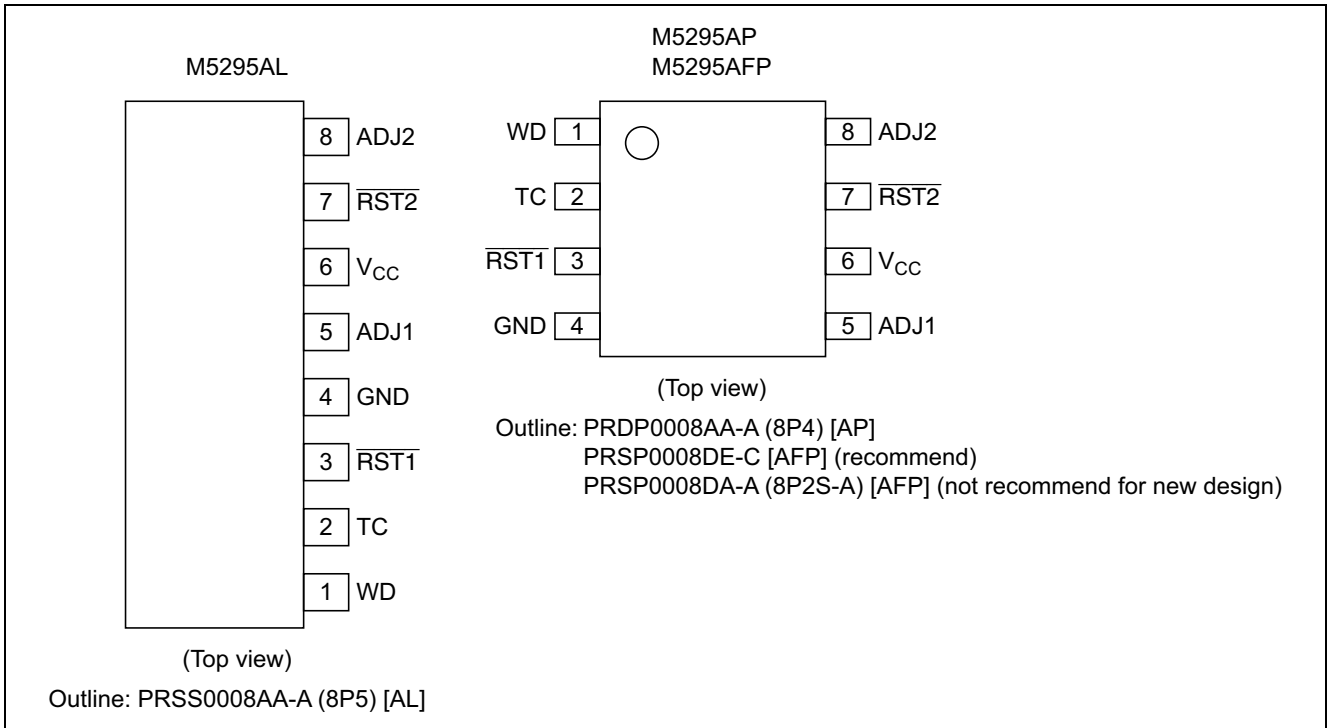
Recommended Operating Condition

- Supply voltage range: 4 V to 15 V
- Rated supply voltage: 5 V

Block Diagram



Pin Arrangement



Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	15	V
Input voltage	V _{IN}	-10 to +10	V
Output voltage	V _{OUT}	15	V
Output current	I _{OUT}	10	mA
Power dissipation	P _d	800(AL)/625(AP)/440(AFP)	mW
Thermal derating	K _θ	8.0(AL)/6.25(AP)/4.4(AFP)	mW/°C
Operating temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-55 to +125	°C

Electrical Characteristics

(Ta = 25°C, unless otherwise noted)

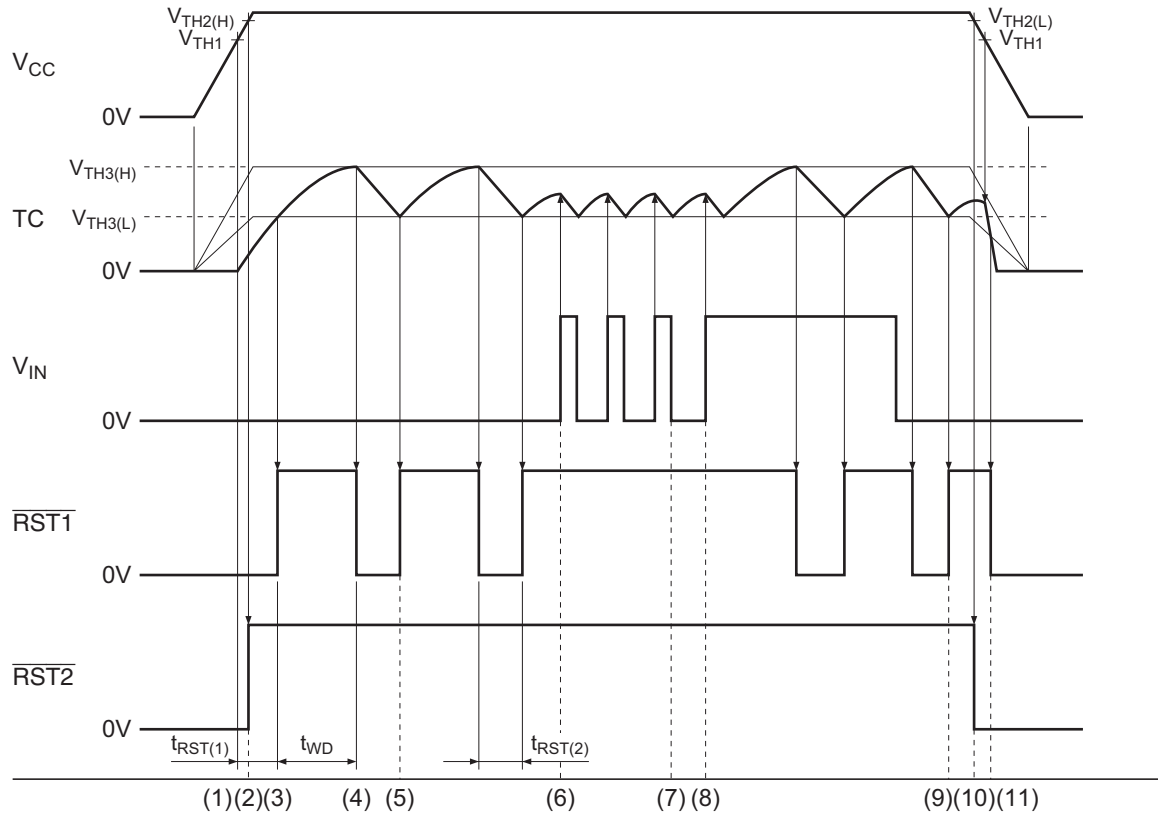
DC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Pin	
WD input current	I _{IH}	0.06	0.15	0.25	mA	WD	V _{IN} = 5V
	I _{IL}	-0.05	-0.1	-0.15			V _{IN} = -5V
WD input voltage	V _{IH}	2	—	—	V	WD	
	V _{IL}	—	—	0.8			
TC output current	I _{OUT}	—	—	-1	μA	TC	V _{IN} = 1.5V
TC input current	I _{IN}	—	3.3	—	mA	TC	V _{OUT} = 4.2V
Threshold voltage of watchdog timer	V _{TH3(H)}	3.7	4	4.3	V	TC	
	V _{TH3(L)}	1.7	2	2.3			
Output voltage	V _{OL}	—	0.1	0.5	V	RST1	I _{OUT} = 1mA
Output leakage current	I _{leak}	—	—	5	μA	RST2	V _{OUT} = 15V
V _{CC} detective voltage (1)	V _{TH1}	4.05	4.25	4.45	V	V _{CC}	
V _{CC} detective voltage (2)	V _{TH2(H)}	4.5	4.7	4.9	V	V _{CC}	
	V _{TH2(L)}	4.45	4.6	4.75			
	ΔV _{TH2}	0.05	0.1	0.2			
ADJ1 voltage	V ₅	1.17	1.46	1.75	V	ADJ1	
ADJ2 voltage	V ₈	1.07	1.34	1.61	V	ADJ2	
RST1 on voltage	RST1	—	—	0.5	V	RST1	V _{CC} = 1.2V, R _L = 4.7kΩ
RST2 on voltage	RST2	—	—	0.5	V	RST2	V _{CC} = 1.2V, R _L = 4.7kΩ
Circuit current	I _{CC}	—	0.8	1.5	mA	V _{CC}	

DC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Pin	
Watchdog timer	T _{WD}	—	1.1·C·R ₁	—	s	RST1	
		0.5	1.1	1.7	ms		C = 0.1μF, R ₁ = 10kΩ
Reset timer (1)	t _{RST(1)}	—	0.5·C·R ₁	—	s	RST1	
		0.2	0.5	1.1	ms		C = 0.1μF, R ₁ = 10kΩ
Reset timer (2)	t _{RST(2)}	—	830·C	—	s	RST1	R ₁ = 10kΩ
		40	83	220	μs		C = 0.1μF, R ₁ = 10kΩ
Input pulse watch	t _{WDIN}	3	—	—	μs	WD	
Transmittal delay time	t _{d1}	—	20	—	μs	RST1	
	t _{d2}	—	10	—	μs	RST2	

Operating Description



- (1): The V_{CC} rises up to 0.8 V, then $\overline{RST1}$ and $\overline{RST2}$ generates low output, and rising up to 4.25 V, charge of C1 begins.
- (2): The V_{CC} rises up to 4.7 V, then $\overline{RST2}$ generates high.
- (3), (4): The voltage at TC pin is 2 V, then $\overline{RST2}$ generates high, when 4 V, C1 is discharged and $\overline{RST1}$ generates low.
- (5): The voltage at TC pin falls to 2 V, then $\overline{RST1}$ generates high unless normal clock signal is entered to WD pin, $\overline{RST1}$ repeats this operation.
- (6), (7): Before the voltage at TC pin reaches 4 V, if normal clock signal is entered to WD pin, low $\overline{RST1}$ is canceled.
- (8), (9): In the case of entrance of abnormal signal input, as the waveform of TC pin repeats charge and discharge of $\overline{RST1}$ alternatively from 2 V to 4 V, the $\overline{RST1}$ repeats high and low output operation.
- (10): The V_{CC} falls to 4.6 V, then $\overline{RST2}$ generates low, this detective voltage has a 100 mV hysteresis.
- (11): When V_{CC} goes down to 4.25 V (V_{TH1}), the status of TC pin is switched to discharge. When the potential at TC pin is detected being $V_{TH3(H)}$ or $V_{TH3(L)}$, the status of $\overline{RST1}$ becomes "low".

Terminology

$t_{RST(1)}$: Time required for TC pin potential to rise from 0 V $V_{TH3(L)}$ when V_{CC} is being applied.

t_{WD} : Time required for TC pin potential to rise from $V_{TH3(L)}$ to $V_{TH3(H)}$.

$t_{RST(2)}$: Time required for TC pin potential to go down from $V_{TH3(H)}$ to $V_{TH3(L)}$.

Figure 1 Operating Waveform

1. Pin(2) (TC pin) charge time and discharge time

When input to WD pin is abnormal, TC pin output waveform is as shown below:

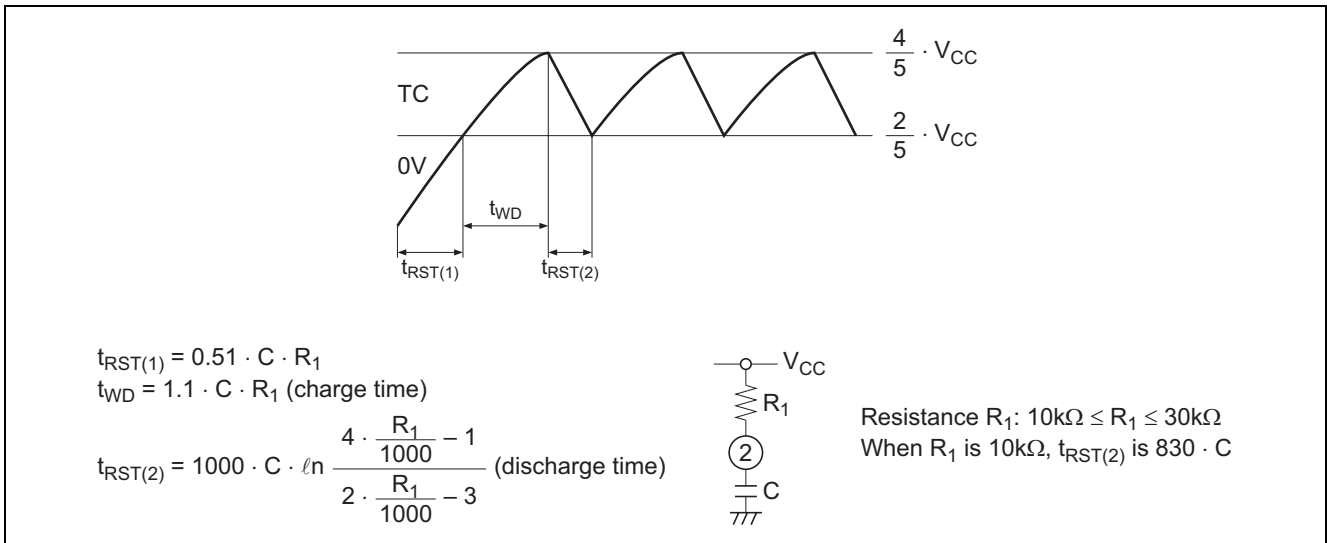


Figure 2

2. Pin (1) (WD pin) input frequency, input pulse width, charge time and discharge time

When input to WD pin is normal, TC pin output waveform is as shown below:

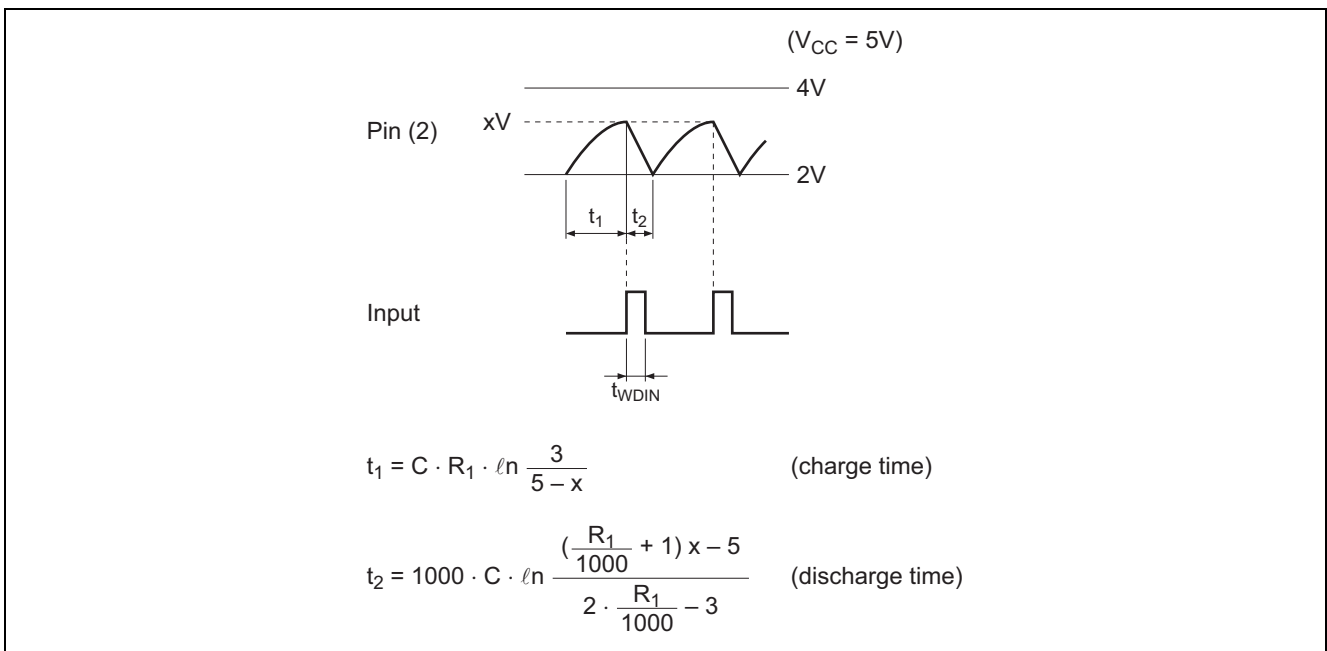


Figure 3

- Pin (1) (WD pin) input requirements
 - Connect capacitor between WD pin and voltage input. (refer to section 3)
 - Input cycle: t_{WD} or less (discharge should start before voltage at WD pin reaches 4 V.)

$$\frac{1}{1.1 \cdot C \cdot R_1} < f$$

- Input pulse width t_{WDIN} : t_2 or less

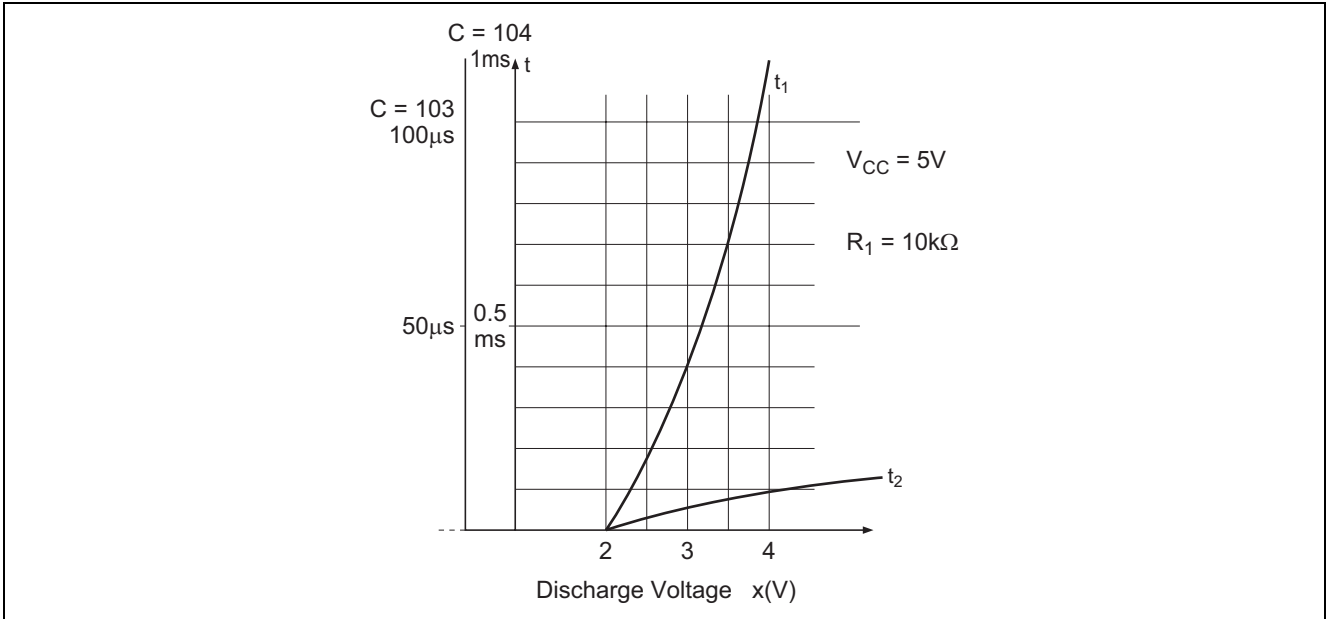


Figure 4

3. Relationship between input pulse width and input capacitance Cin

When input to pin (1) is 1.5 V or more, TC pin discharges electricity. Determine pulse width and input capacitance C_{in} with reference to the diagram shown in figure 5.

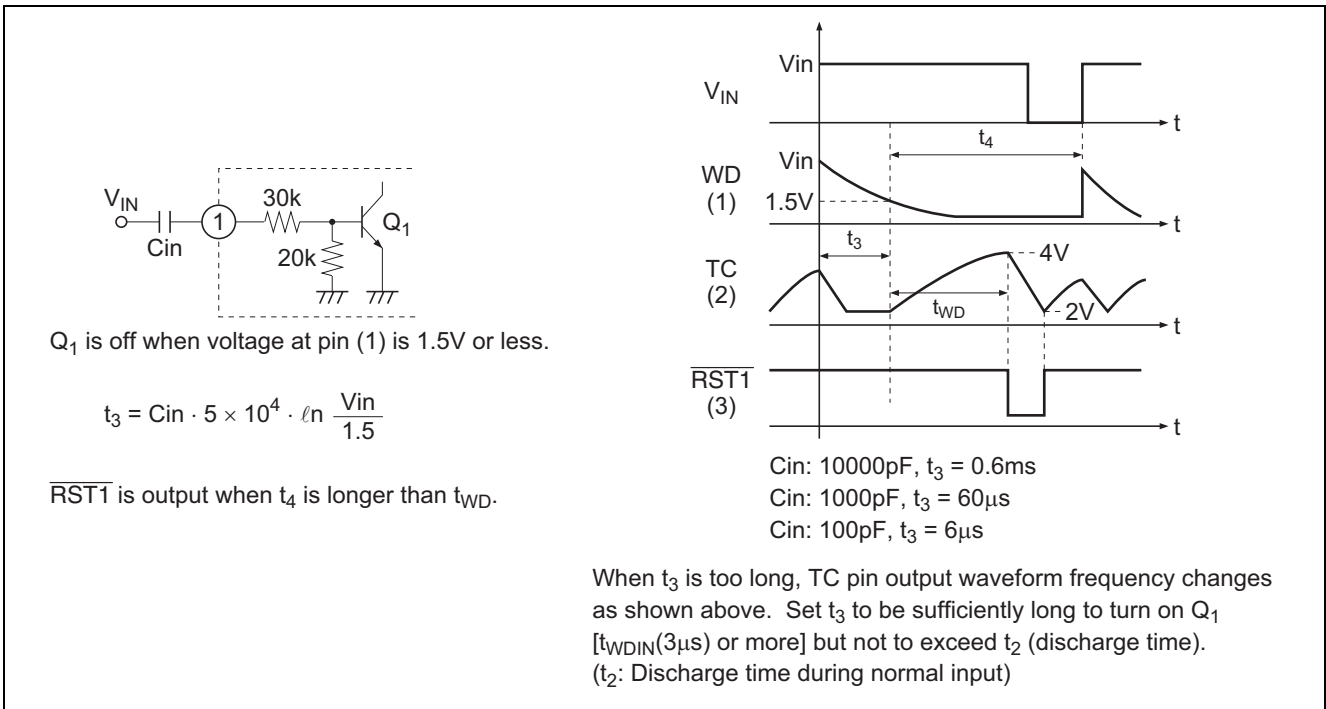


Figure 5

4. V_{CC} detection voltage adjustment

(1) Detection voltage 1 (V_{TH1}) adjustment

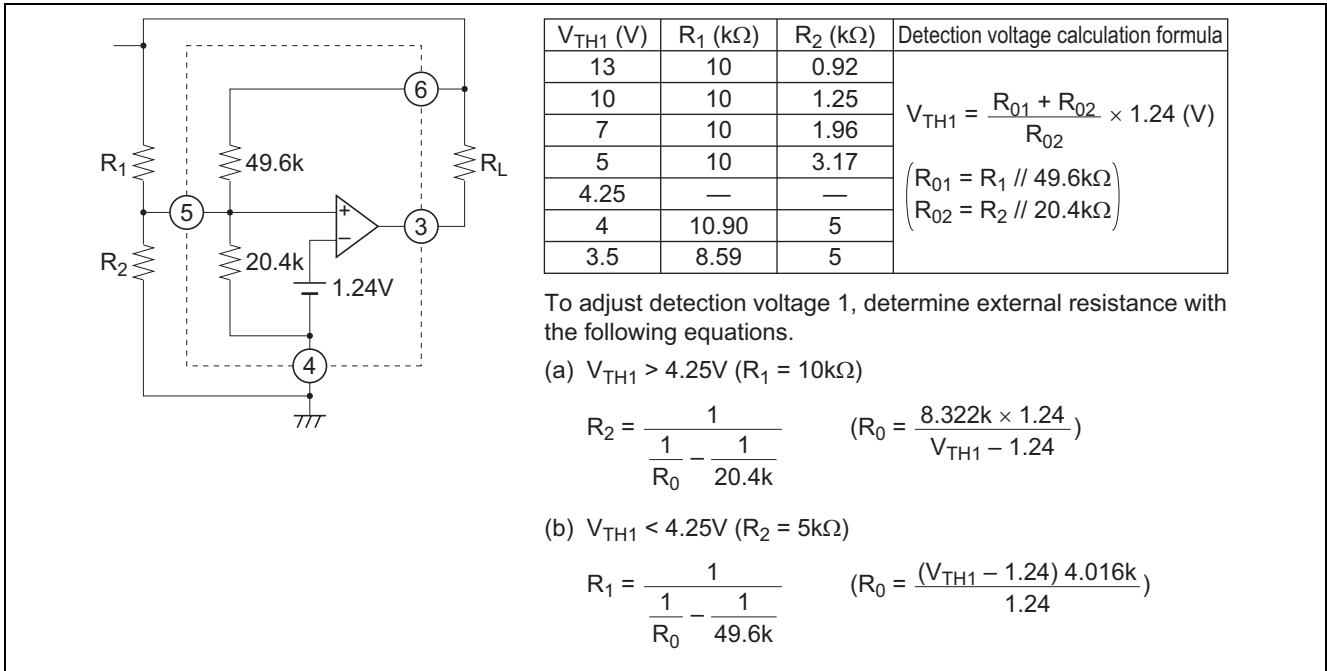


Figure 6 Detection Voltage 1 (V_{TH1}) Adjustment

(2) Detection voltage 2 (V_{TH2(L)}) adjustment

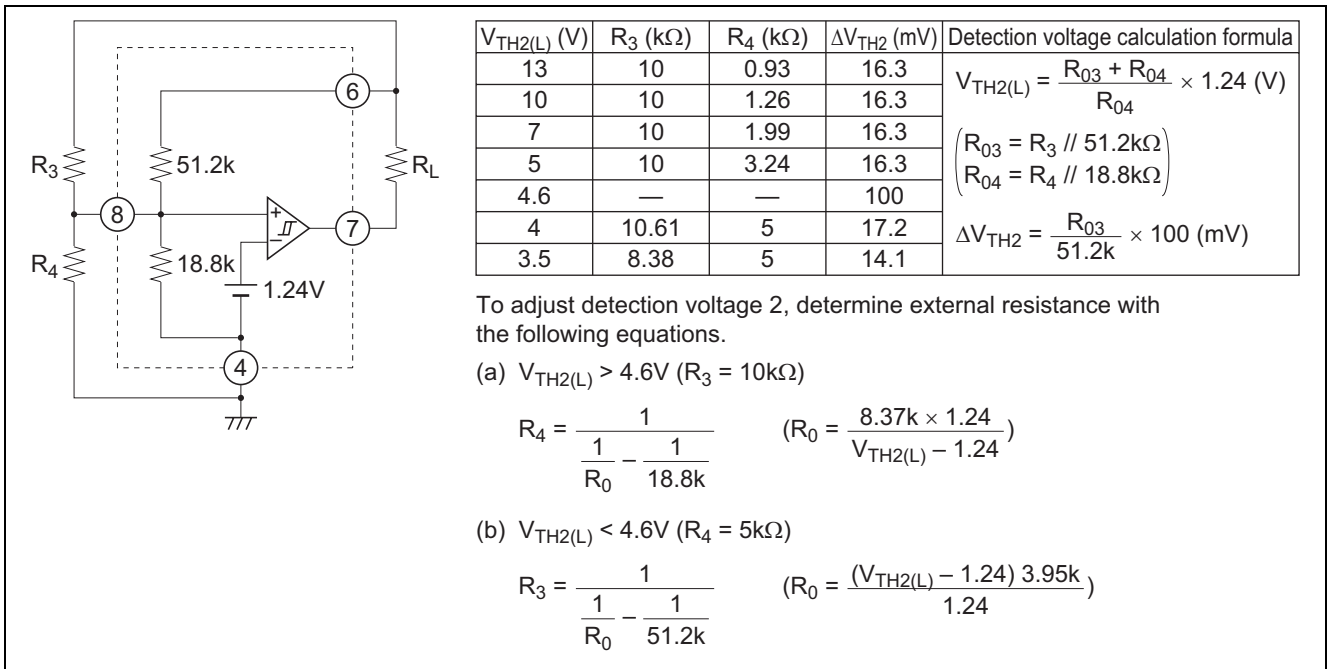


Figure 7 Detection Voltage 2 (V_{TH2(L)}) Adjustment

Application Example

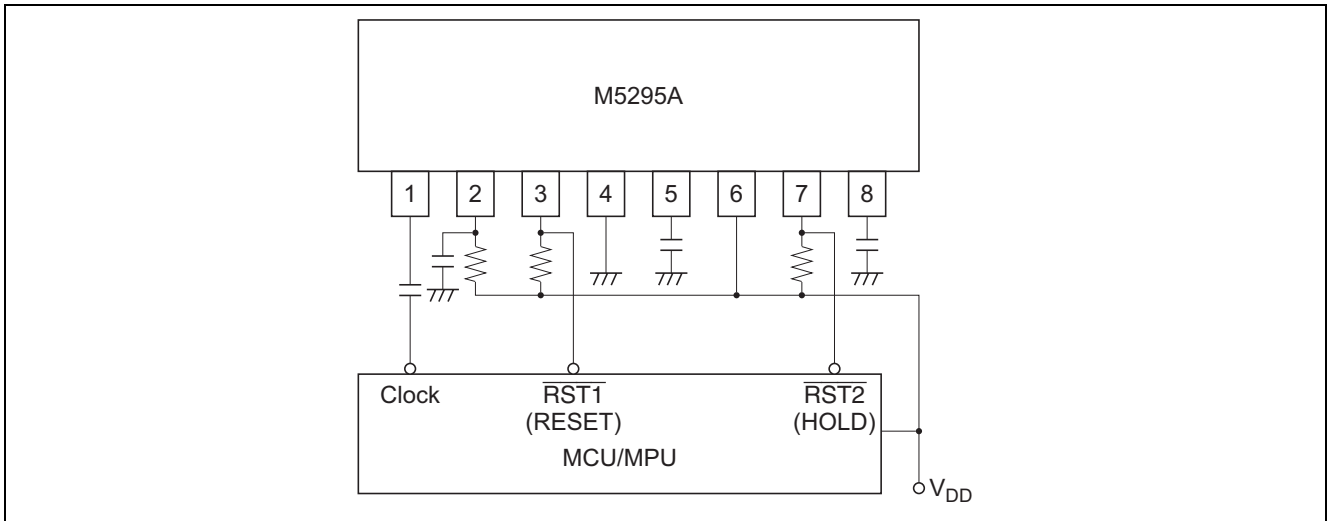


Figure 8 Application Example

Notice for Use

- When malfunction occurs due to noise or order related trouble, connect capacitance of approximately 1000 pF between pin (5) and GND as well as pin (8) and GND to stabilize operation.
- To adjust detection voltage, add resistance of 15 kΩ or less to both V_{CC} and GND via adjusting pins. (Set detection voltage to no less than 3 V.)
- Set t_{WD} and t_{RST(2)} as shown below:
 $110 \mu\text{s} \leq t_{\text{WD}} \leq 1.1 \text{ s}$
 $8.3 \mu\text{s} \leq t_{\text{RST(2)}} \leq 83 \text{ ms}$
 $10 \text{ k}\Omega \leq R_1 \leq 30 \text{ k}\Omega$
- Input clock pulses to pin (1) via capacitor. To determine capacitance, refer to “Relationship between input pulse width and input capacitance C_{in}”.

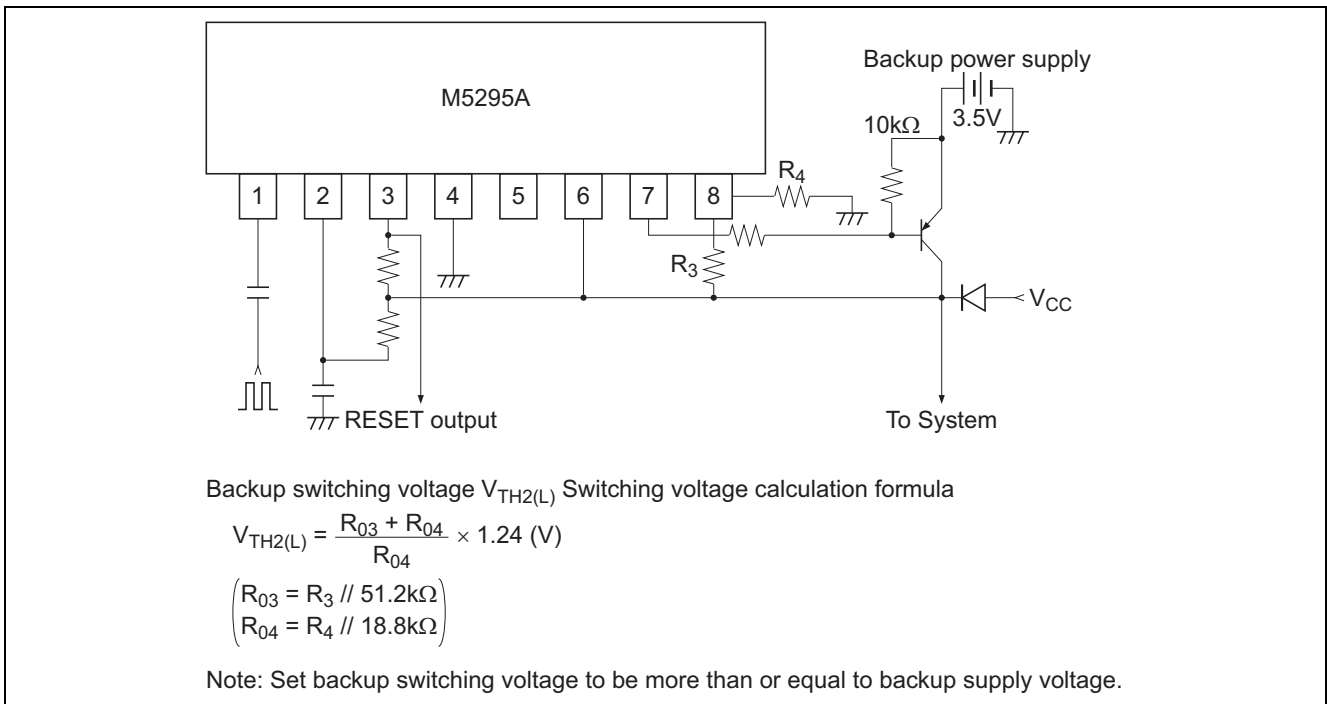
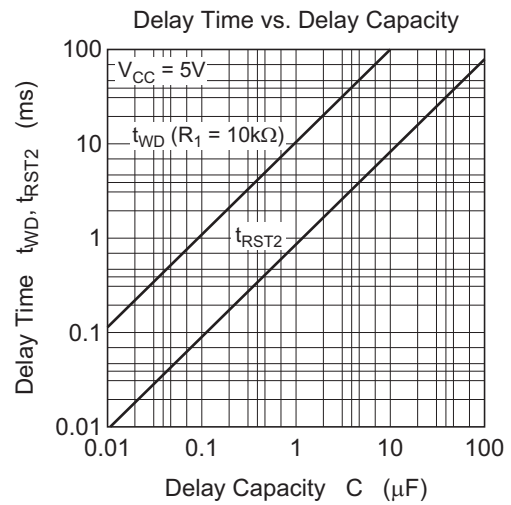
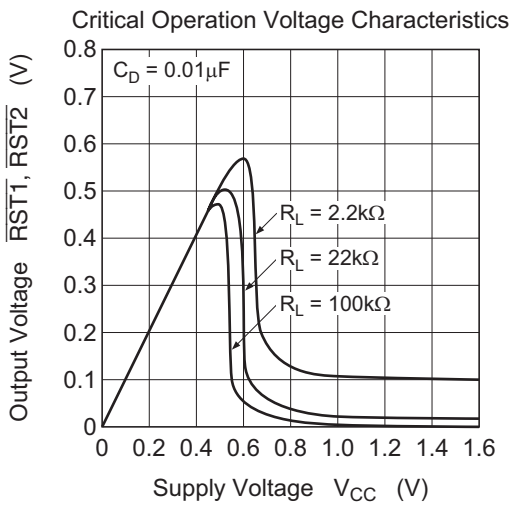
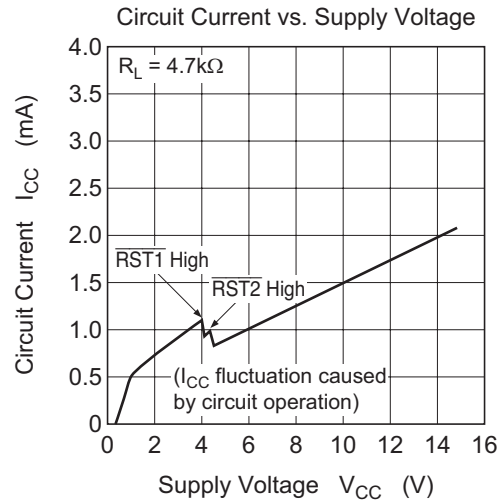
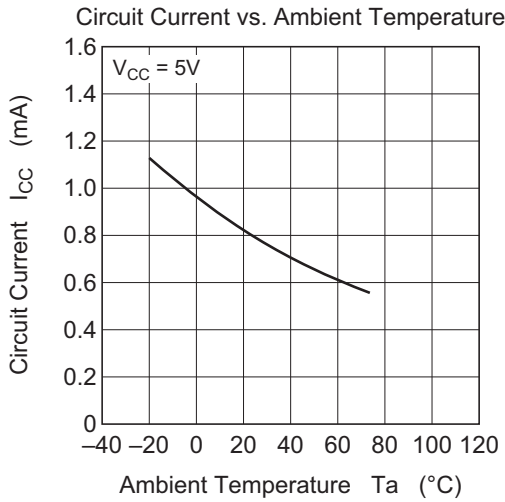
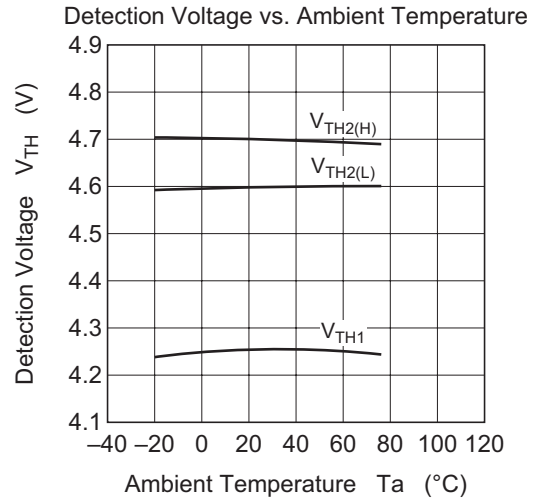
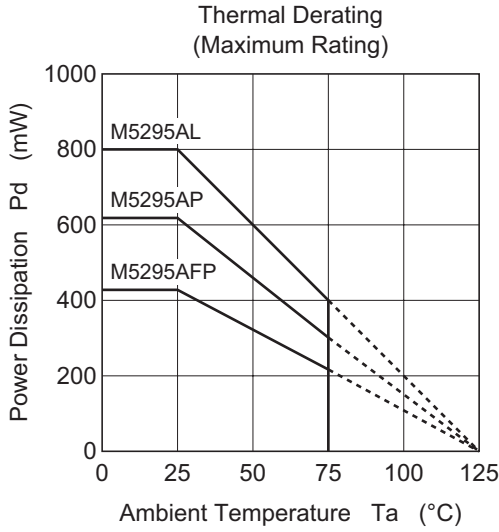
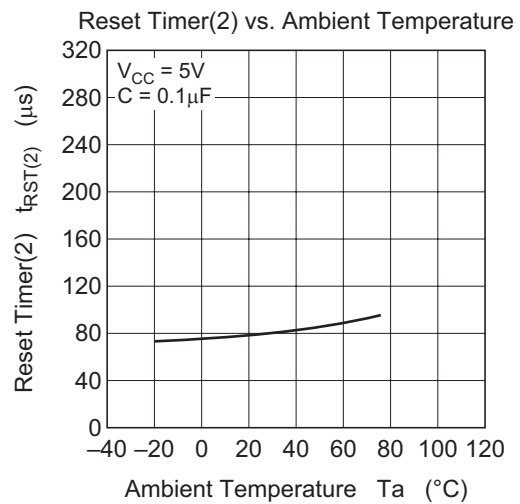
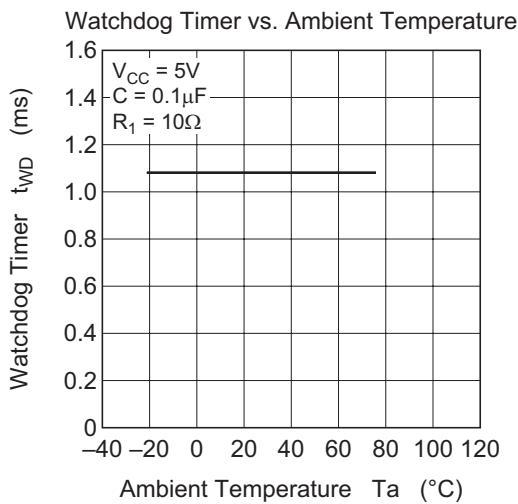
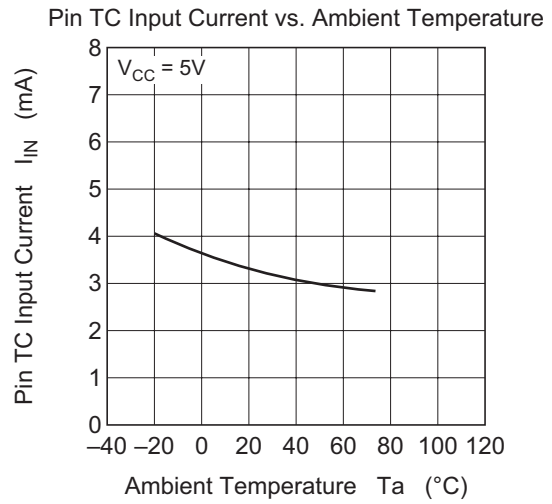
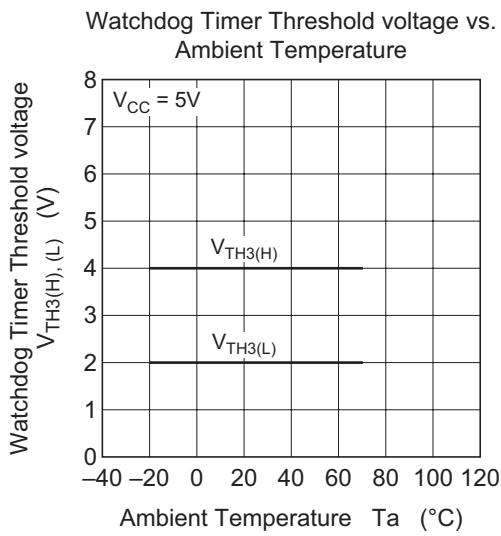
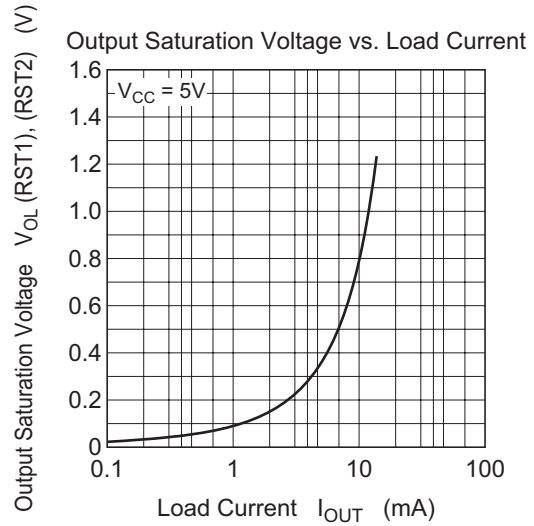
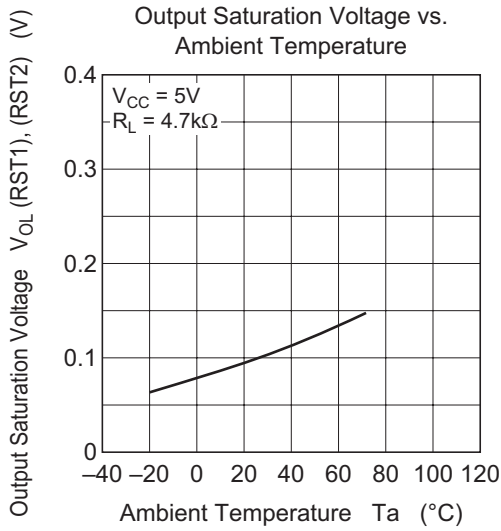


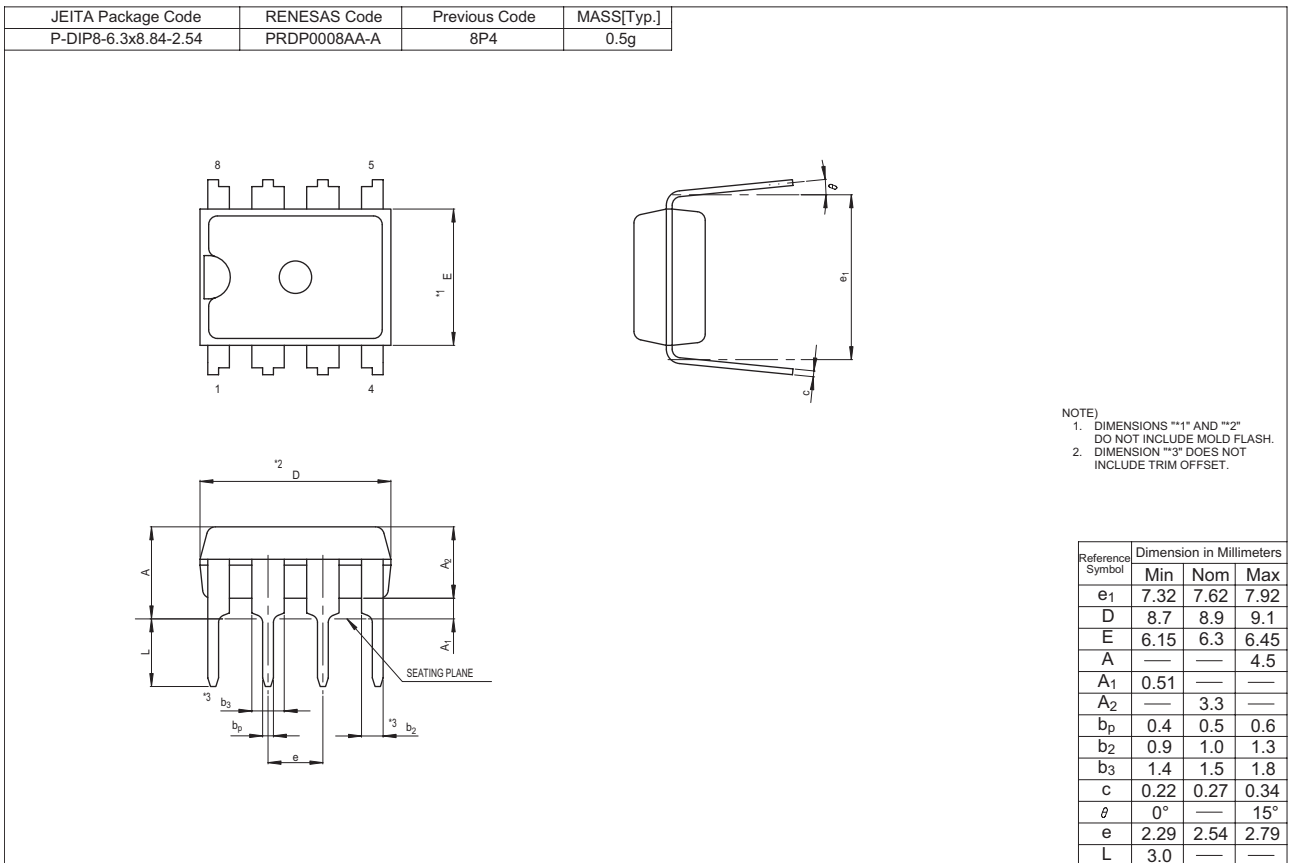
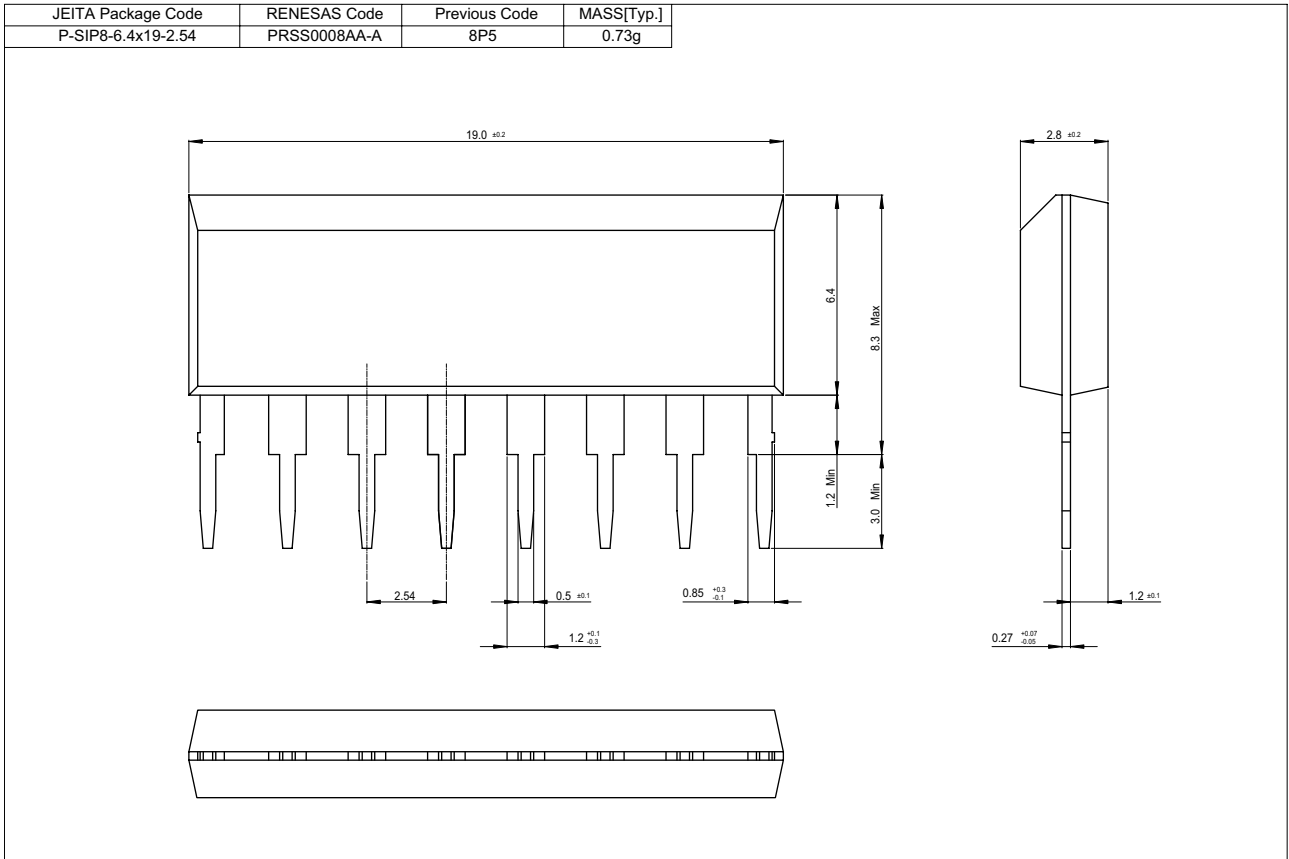
Figure 9 Example of Backup Circuit with M5295AL

Typical Characteristics



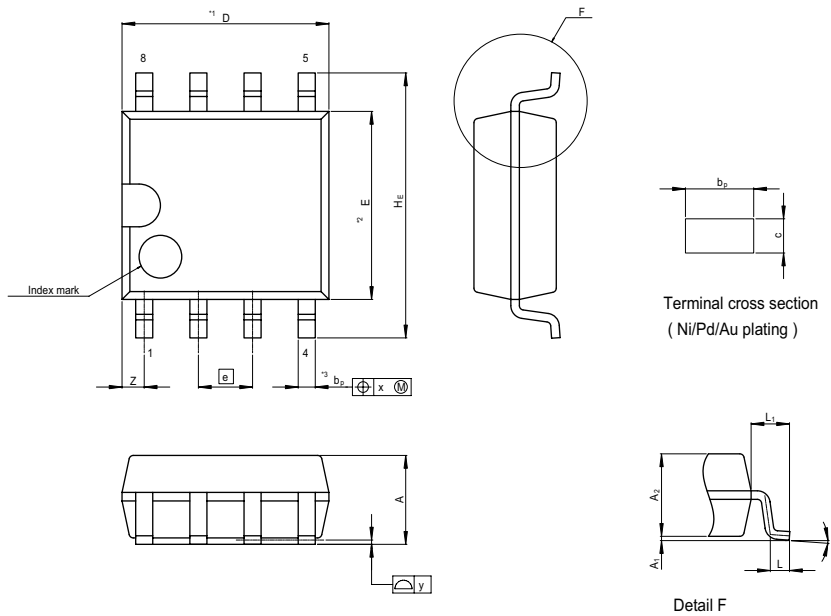


Package Dimensions



M5295AL/AP/AFP

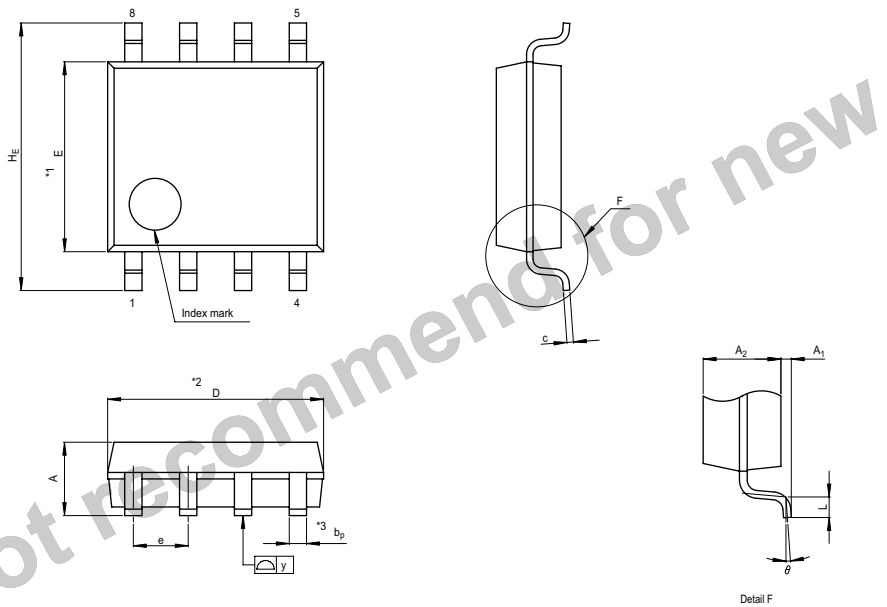
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x4.85-1.27	PRSP0008DE-C	—	0.1g



NOTE)
 1. DIMENSIONS **1 (Nom)** AND **2*
 DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3* DOES NOT
 INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.65	4.85	5.05
E	4.2	4.4	4.6
A ₂	—	1.85	—
A ₁	0.00	0.1	0.20
A	—	—	2.03
b _p	0.34	0.4	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
c ₁	—	—	—
θ	0°	—	8°
H _E	5.7	6.2	6.5
Ⓧ	1.12	1.27	1.42
x	—	—	0.12
y	—	—	0.10
Z	—	—	0.75
L	0.25	0.45	0.65
L ₁	—	0.90	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x5-1.27	PRSP0008DA-A	8P2S-A	0.07g



NOTE)
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 DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3* DOES NOT
 INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
A ₂	—	1.5	—
A ₁	0.05	—	—
A	—	—	1.9
b _p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H _E	5.9	6.2	6.5
e	1.12	1.27	1.42
y	—	—	0.1
L	0.2	0.4	0.6

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