## *8M x 16Bit x 4 Banks Mobile SDRAM in 54FBGA*

### FEATURES

- 3.0V or 3.3V power supply.
- LVCMOS compatible with multiplexed address.
- Four banks operation.
- MRS cycle with address key programs.
  - -. CAS latency (1, 2 & 3).
  - -. Burst length (1, 2, 4, 8 & Full page).
  - -. Burst type (Sequential & Interleave).
- EMRS cycle with address key programs.
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation.
- Special Function Support.
  - -. PASR (Partial Array Self Refresh).
  - -. Internal TCSR (Temperature Compensated Self Refresh)
- DQM for masking.
- Auto refresh.
- 64ms refresh period (8K cycle).
- Commercial Temperature Operation (-25°C ~ 70°C).
- 2 /CS Support.
- 2chips DDP 54Balls FBGA with 0.8mm ball pitch ( -YXXX : Leaded , -PXXX : Lead Free).

### GENERAL DESCRIPTION

The K4M511533E is 536,870,912 bits synchronous high data rate Dynamic RAM organized as 4 x 8,388,608 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

### ORDERING INFORMATION

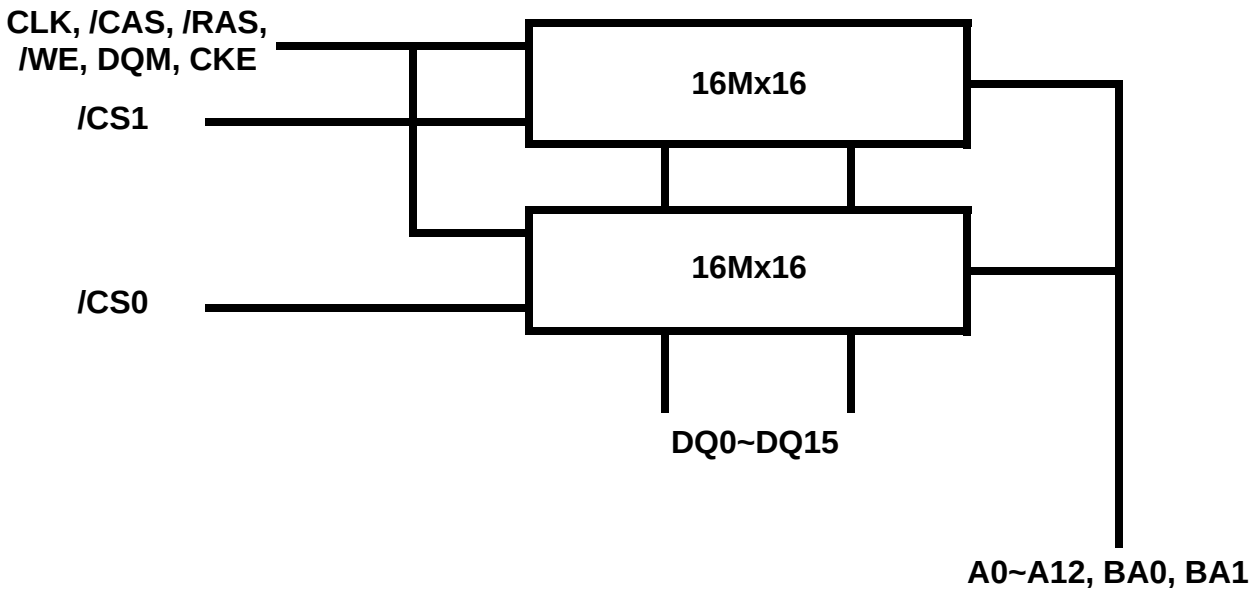
| Part No. | Max Freq. | Interface | Package |
|---|---|---|---|
| K4M511533E-Y(P)C/L/F75 | 133MHz(CL=3) | LVCMOS | 54 FBGA Leaded (Lead Free) |
| K4M511533E-Y(P)C/L/F1H | 105MHz(CL=2) | | |
| K4M511533E-Y(P)C/L/F1L | 105MHz(CL=3)*1 | | |

- Y(P)C/L/F : Normal / Low Power, Commercial Temperature(-25°C ~ 70°C)

**Notes :**

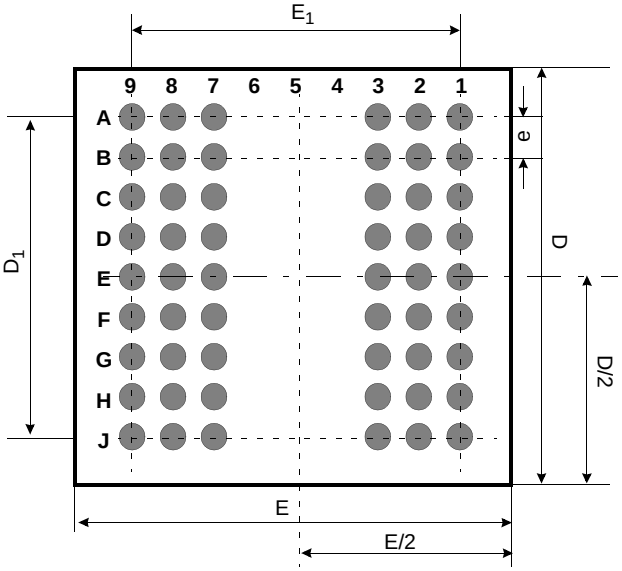
1. In case of 40MHz Frequency, CL1 can be supported.
2. Samsung shall not offer for sale or sell either directly or through and third-party proxy, and DRAM memory products that include "Multi-Die Plastic DRAM" for use as components in general and scientific computers such as, by way of example, mainframes, servers, work stations or desk top computers for the first three years of five year term of this license. Nothing herein limits the rights of Samsung to use Multi-Die Plastic DRAM in other products or other applications under paragrangh such as mobile, telecom or non-computer application(which include by way of example laptop or notebook computers, cell phones, televisions or visual monitors)
   Violation may subject the customer to legal claims and also excludes any warranty against infringement from Samsung." .
3. Samsung are not designed or manufactured for use in a device or system that is used under circumstance in which human life is potentially at stake. Please contact to the memory marketing team in samsung electronics when considering the use of a product contained herein for any specific purpose, such as medical, aerospace, nuclear, military, vehicular or undersea repeater use.

## FUNCTIONAL BLOCK DIAGRAM

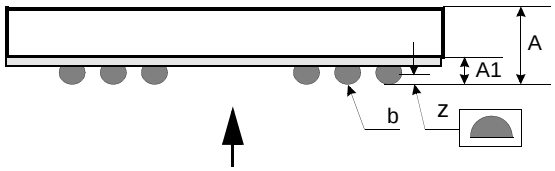


## Package Dimension and Pin Configuration

**< Bottom View*1 >**

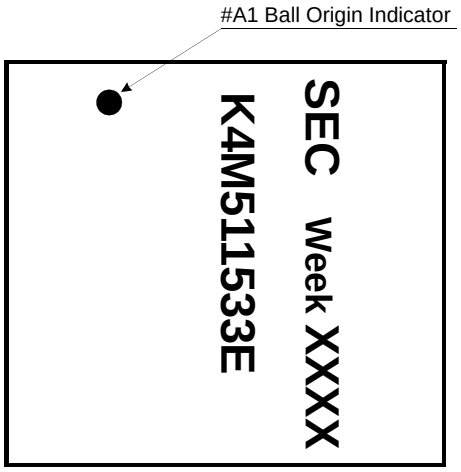



*2: Top View




*1: Bottom View

**< Top View*2 >**




**< Top View*2 >**

| 54Ball(6x9) FBGA | | | | | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 7 | 8 | 9 |
| A | VSS | DQ15 | VSSQ | VDDQ | DQ0 | VDD |
| B | DQ14 | DQ13 | VDDQ | VSSQ | DQ2 | DQ1 |
| C | DQ12 | DQ11 | VSSQ | VDDQ | DQ4 | DQ3 |
| D | DQ10 | DQ9 | VDDQ | VSSQ | DQ6 | DQ5 |
| E | DQ8 | **$\overline{CS1}$** | VSS | VDD | LDQM | DQ7 |
| F | UDQM | CLK | CKE | $\overline{CAS}$ | $\overline{RAS}$ | $\overline{WE}$ |
| G | A12 | A11 | A9 | BA0 | BA1 | **$\overline{CS0}$** |
| H | A8 | A7 | A6 | A0 | A1 | A10 |
| J | VSS | A5 | A4 | A3 | A2 | VDD |

| Pin Name | Pin Function |
|---|---|
| CLK | *System Clock* |
| $\overline{CS}_{0 \sim 1}$ | *Chip Select* |
| CKE | *Clock Enable* |
| $A_0 \sim A_{12}$ | *Address* |
| $BA_0 \sim BA_1$ | *Bank Select Address* |
| $\overline{RAS}$ | *Row Address Strobe* |
| $\overline{CAS}$ | *Column Address Strobe* |
| $\overline{WE}$ | *Write Enable* |
| L(U)DQM | *Data Input/Output Mask* |
| $DQ_{0 \sim 15}$ | *Data Input/Output* |
| $V_{DD}/V_{SS}$ | *Power Supply/Ground* |
| $V_{DDQ}/V_{SSQ}$ | *Data Output Power/Ground* |

[Unit:mm]

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | 1.00 | 1.10 | 1.20 |
| $A_1$ | 0.27 | 0.32 | 0.37 |
| E | - | 11.5 | - |
| $E_1$ | - | 6.40 | - |
| D | - | 10.0 | - |
| $D_1$ | - | 6.40 | - |
| e | - | 0.80 | - |
| b | 0.40 | 0.45 | 0.50 |
| z | - | - | 0.10 |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -1.0 ~ 4.6 | V |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}$, $V_{DDQ}$ | -1.0 ~ 4.6 | V |
| Storage temperature | $T_{STG}$ | -55 ~ +150 | °C |
| Power dissipation | $P_D$ | 1.0 | W |
| Short circuit current | $I_{OS}$ | 50 | mA |

**NOTES:**
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to $V_{SS}$ = 0V, $T_A$ = -25°C ~ 70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 2.7 | 3.0 | 3.6 | V | |
| | $V_{DDQ}$ | 2.7 | 3.0 | 3.6 | V | |
| Input logic high voltage | $V_{IH}$ | 2.2 | 3.0 | $V_{DDQ}$ + 0.3 | V | 1 |
| Input logic low voltage | $V_{IL}$ | -0.3 | 0 | 0.5 | V | 2 |
| Output logic high voltage | $V_{OH}$ | 2.4 | - | - | V | $I_{OH}$ = -2mA |
| Output logic low voltage | $V_{OL}$ | - | - | 0.4 | V | $I_{OL}$ = 2mA |
| Input leakage current | $I_{LI}$ | -10 | - | 10 | uA | 3 |

**NOTES :**
1. VIH (max) = 5.3V AC.The overshoot voltage duration is ≤ 3ns.
2. VIL (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ VIN ≤ VDDQ.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.
4. Dout is disabled, 0V ≤ VOUT ≤ VDDQ.

## CAPACITANCE ($V_{DD}$ = 3.0V & 3.3V, $T_A$ = 23°C, f = 1MHz, $V_{REF}$ =0.9V ± 50 mV)

| Pin | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Clock | $C_{CLK}$ | 3.0 | 12.0 | pF | |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE | $C_{IN}$ | 3.0 | 12.0 | pF | |
| $\overline{CS}$ | $C_{IN}$ | 1.5 | 6.0 | pF | |
| DQM | $C_{IN}$ | 3.0 | 12.0 | pF | |
| Address | $C_{ADD}$ | 3.0 | 12.0 | pF | |
| $DQ_0$ ~ $DQ_{15}$ | $C_{OUT}$ | 6.0 | 13.0 | pF | |

## DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to $V_{SS}$ = 0V, $T_A$ = -25 to 70°C)

| Parameter | Symbol | Test Condition | | | Version | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | -75 | -1H | -1L | | |
| Operating Current (One Bank Active) | $I_{CC1}$ | Burst length = 1<br>$t_{RC} \geq t_{RC}$(min)<br>$I_O$ = 0 mA | | | 100 | 90 | 85 | mA | 1 |
| Precharge Standby Current in power-down mode | $I_{CC2P}$ | CKE ≤ $V_{IL}$(max), $t_{CC}$ = 10ns | | | 1.5 | | | mA | |
| | $I_{CC2PS}$ | CKE & CLK ≤ $V_{IL}$(max), $t_{CC}$ = ∞ | | | 1.5 | | | | |
| Precharge Standby Current in non power-down mode | $I_{CC2N}$ | CKE ≥ $V_{IH}$(min), $\overline{CS}$ ≥ $V_{IH}$(min), $t_{CC}$ = 10ns<br>Input signals are changed one time during 20ns | | | 20 | | | mA | |
| | $I_{CC2NS}$ | CKE ≥ $V_{IH}$(min), CLK ≤ $V_{IL}$(max), $t_{CC}$ = ∞<br>Input signals are stable | | | 10 | | | | |
| Active Standby Current in power-down mode | $I_{CC3P}$ | CKE ≤ $V_{IL}$(max), $t_{CC}$ = 10ns | | | 8 | | | mA | |
| | $I_{CC3PS}$ | CKE & CLK ≤ $V_{IL}$(max), $t_{CC}$ = ∞ | | | 8 | | | | |
| Active Standby Current in non power-down mode (One Bank Active) | $I_{CC3N}$ | CKE ≥ $V_{IH}$(min), $\overline{CS}$ ≥ $V_{IH}$(min), $t_{CC}$ = 10ns<br>Input signals are changed one time during 20ns | | | 45 | | | mA | |
| | $I_{CC3NS}$ | CKE ≥ $V_{IH}$(min), CLK ≤ $V_{IL}$(max), $t_{CC}$ = ∞<br>Input signals are stable | | | 35 | | | mA | |
| Operating Current (Burst Mode) | $I_{CC4}$ | $I_O$ = 0 mA<br>Page burst<br>4Banks Activated<br>$t_{CCD}$ = 2CLKs | | | 145 | 125 | 115 | mA | 1 |
| Refresh Current | $I_{CC5}$ | $t_{RC} \geq t_{RC}$(min) | | | 190 | 170 | 160 | mA | 2 |
| Self Refresh Current | $I_{CC6}$ | CKE ≤ 0.2V | **-C** | | 1800 | | | uA | 4 |
| | | | **-L** | | 1500 | | | | 5 |
| | | | **-F** | **Internal TCSR** | **Max 40** | **Max 70** | | °C | 3 |
| | | | | Full Array | 850 | 1300 | | uA | 6 |
| | | | | 1/2 of Full Array | 600 | 900 | | | |
| | | | | 1/4 of Full Array | 500 | 700 | | | |

**NOTES:**

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Internal TCSR can be supported(In commercial Temp : Max 40°C/Max 70°C).
4. K4M511533E-Y(P)C**
5. K4M511533E-Y(P)L**
6. K4M511533E-Y(P)F**
7. Unless otherwise noted, input swing level is CMOS(VIH /VIL=VDDQ/VSSQ).

## AC OPERATING TEST CONDITIONS ($V_{DD}$ = 2.7V ~ 3.6V, $T_A$ = -25 to 70°C)

| Parameter | Value | Unit |
|---|---|---|
| AC input levels (Vih/Vil) | 2.4 / 0.4 | V |
| Input timing measurement reference level | 1.4 | V |
| Input rise and fall time | tr/tf = 1/1 | ns |
| Output timing measurement reference level | 1.4 | V |
| Output load condition | See Figure 2 | |

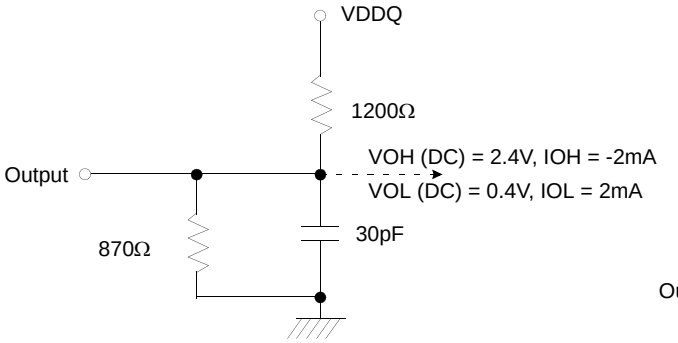



**Figure 1. DC Output Load Circuit**

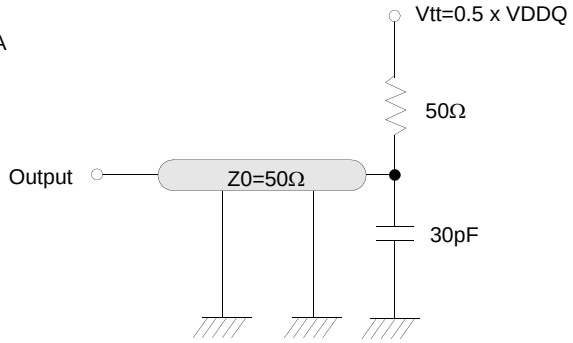



**Figure 2. AC Output Load Circuit**

## OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

| Parameter | Symbol | Version | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | -75 | -1H | -1L | | |
| Row active to row active delay | $t_{RRD}$(min) | 15 | 19 | 19 | ns | 1 |
| $\overline{RAS}$ to $\overline{CAS}$ delay | $t_{RCD}$(min) | 19 | 19 | 24 | ns | 1 |
| Row precharge time | $t_{RP}$(min) | 19 | 19 | 24 | ns | 1 |
| Row active time | $t_{RAS}$(min) | 45 | 50 | 60 | ns | 1 |
| | $t_{RAS}$(max) | 100 | | | us | |
| Row cycle time | $t_{RC}$(min) | 64 | 69 | 84 | ns | 1 |
| Last data in to row precharge | $t_{RDL}$(min) | 2 | | | CLK | 2 |
| Last data in to Active delay | $t_{DAL}$(min) | tRDL + tRP | | | - | 3 |
| Last data in to new col. address delay | $t_{CDL}$(min) | 1 | | | CLK | 2 |
| Last data in to burst stop | $t_{BDL}$(min) | 1 | | | CLK | 2 |
| Col. address to col. address delay | $t_{CCD}$(min) | 1 | | | CLK | 4 |
| Number of valid output data | CAS latency=3 | 2 | | | ea | 5 |
| Number of valid output data | CAS latency=2 | 1 | | | | |
| Number of valid output data | CAS latency=1 | 0 | | | | |

**NOTES:**

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. Minimum tRDL=2CLK and tDAL(= tRDL + tRP) is required to complete both of last data write command(tRDL) and precharge command(tRP).
4. All parts allow every cycle column address change.
5. In case of row precharge interrupt, auto precharge and read burst stop.

## AC CHARACTERISTICS(AC operating conditions unless otherwise noted)

| Parameter | | Symbol | -75 | | -1H | | -1L | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| CLK cycle time | CAS latency=3 | $t_{CC}$ | 7.5 | 1000 | 9.5 | 1000 | 9.5 | 1000 | ns | 1 |
| CLK cycle time | CAS latency=2 | $t_{CC}$ | 9.5 | | 9.5 | | 12 | | | |
| CLK cycle time | CAS latency=1 | $t_{CC}$ | - | | - | | 25 | | | |
| CLK to valid output delay | CAS latency=3 | $t_{SAC}$ | | 5.4 | | 7 | | 7 | ns | 1,2 |
| CLK to valid output delay | CAS latency=2 | $t_{SAC}$ | | 7 | | 7 | | 8 | | |
| CLK to valid output delay | CAS latency=1 | $t_{SAC}$ | | - | | - | | 20 | | |
| Output data hold time | CAS latency=3 | $t_{OH}$ | 2.5 | | 2.5 | | 2.5 | | ns | 2 |
| Output data hold time | CAS latency=2 | $t_{OH}$ | 2.5 | | 2.5 | | 2.5 | | | |
| Output data hold time | CAS latency=1 | $t_{OH}$ | - | | - | | 2.5 | | | |
| CLK high pulse width | | $t_{CH}$ | 2.5 | | 3.0 | | 3.0 | | ns | 3 |
| CLK low pulse width | | $t_{CL}$ | 2.5 | | 3.0 | | 3.0 | | ns | 3 |
| Input setup time | | $t_{SS}$ | 2.0 | | 2.5 | | 2.5 | | ns | 3 |
| Input hold time | | $t_{SH}$ | 1.0 | | 1.5 | | 1.5 | | ns | 3 |
| CLK to output in Low-Z | | $t_{SLZ}$ | 1 | | 1 | | 1 | | ns | 2 |
| CLK to output in Hi-Z | CAS latency=3 | $t_{SHZ}$ | | 5.4 | | 7 | | 7 | ns | |
| | CAS latency=2 | | | 7 | | 7 | | 8 | | |
| | CAS latency=1 | | | - | | - | | 20 | | |

**NOTES :**

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

## SIMPLIFIED TRUTH TABLE

| COMMAND | | | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | BA0,1 | A10/AP | A12,A11, A9 ~ A0 | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register | Mode Register Set | | H | X | L | L | L | L | X | OP CODE | | | 1, 2 |
| Refresh | Auto Refresh | | H | H | L | L | L | H | X | X | | | 3 |
| | Self Refresh | Entry | | L | | | | | | | | | 3 |
| | | Exit | L | H | L | H | H | H | X | X | | | 3 |
| | | | | | H | X | X | X | | | | | 3 |
| Bank Active & Row Addr. | | | H | X | L | L | H | H | X | V | Row Address | | |
| Read & Column Address | Auto Precharge Disable | | H | X | L | H | L | H | X | V | L | Column Address (A0~A8) | 4 |
| | Auto Precharge Enable | | | | | | | | | | H | | 4, 5 |
| Write & Column Address | Auto Precharge Disable | | H | X | L | H | L | L | X | V | L | Column Address (A0~A8) | 4 |
| | Auto Precharge Enable | | | | | | | | | | H | | 4, 5 |
| Burst Stop | | | H | X | L | H | H | L | X | X | | | 6 |
| Precharge | Bank Selection | | H | X | L | L | H | L | X | V | L | X | |
| | All Banks | | | | | | | | | X | H | | |
| Clock Suspend or Active Power Down | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | V | V | V | | | | | |
| | | Exit | L | H | X | X | X | X | X | | | | |
| Precharge Power Down Mode | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |
| | | Exit | L | H | H | X | X | X | X | | | | |
| | | | | | L | V | V | V | | | | | |
| DQM | | | H | X | | | | | V | X | | | 7 |
| No Operation Command | | | H | X | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |

(V=Valid, X=Don′t Care, H=Logic High, L=Logic Low)

**NOTES :**

1. OP Code : Operand Code
   A0 ~ A12 & BA0 ~ BA1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are the same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
   Partial self refresh can be issued only after setting partial self refresh mode of EMRS.
4. BA0 ~ BA1 : Bank select addresses.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation, it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).

## A. MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with Normal MRS

| Address | BA0 ~ BA1 | A12 ~ A10/AP | A9*2 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | "0" Setting for Normal MRS | RFU*1 | W.B.L | Test Mode | | CAS Latency | | | BT | Burst Length | | |

### Normal MRS Mode

| Test Mode | | | CAS Latency | | | | Burst Type | | | Burst Length | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A8 | A7 | Type | A6 | A5 | A4 | Latency | A3 | Type | | A2 | A1 | A0 | BT=0 | BT=1 |
| 0 | 0 | Mode Register Set | 0 | 0 | 0 | Reserved | 0 | Sequential | | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | Reserved | 0 | 0 | 1 | 1 | 1 | Interleave | | 0 | 0 | 1 | 2 | 2 |
| 1 | 0 | Reserved | 0 | 1 | 0 | 2 | Mode Select | | | 0 | 1 | 0 | 4 | 4 |
| 1 | 1 | Reserved | 0 | 1 | 1 | 3 | BA1 | BA0 | Mode | 0 | 1 | 1 | 8 | 8 |
| Write Burst Length | | | 1 | 0 | 0 | Reserved | 0 | 0 | Setting for Normal MRS | 1 | 0 | 0 | Reserved | Reserved |
| A9 | Length | | 1 | 0 | 1 | Reserved | | | | 1 | 0 | 1 | Reserved | Reserved |
| 0 | Burst | | 1 | 1 | 0 | Reserved | | | | 1 | 1 | 0 | Reserved | Reserved |
| 1 | Single Bit | | 1 | 1 | 1 | Reserved | | | | 1 | 1 | 1 | Full Page | Reserved |

Full Page Length x16 : 512Mb(1024)

Register Programmed with Extended MRS

| Address | BA1 | BA0 | A12 ~ A10/AP | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | Mode Select | | RFU*1 | | | | DS | | RFU*1 | | PASR | | |

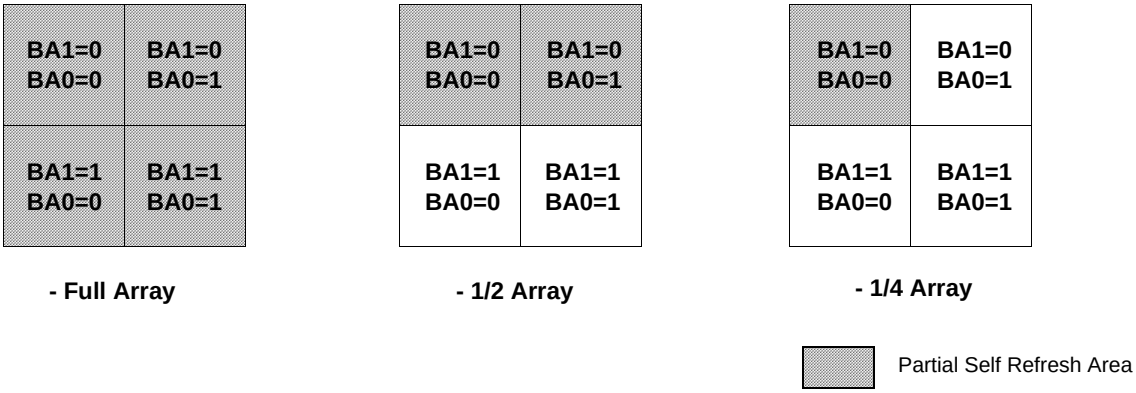
### EMRS for PASR(Partial Array Self Ref.) & DS(Driver Strength)

| Mode Select | | | Driver Strength | | | PASR | | | |
|---|---|---|---|---|---|---|---|---|---|
| BA1 | BA0 | Mode | A6 | A5 | Driver Strength | A2 | A1 | A0 | Size of Refreshed Array |
| 0 | 0 | Normal MRS | 0 | 0 | Full | 0 | 0 | 0 | Full Array |
| 0 | 1 | Reserved | 0 | 1 | 1/2 | 0 | 0 | 1 | 1/2 of Full Array |
| 1 | 0 | EMRS for Mobile SDRAM | 1 | 0 | Reserved | 0 | 1 | 0 | 1/4 of Full Array |
| 1 | 1 | Reserved | 1 | 1 | Reserved | 0 | 1 | 1 | Reserved |
| Reserved Address | | | | | | 1 | 0 | 0 | Reserved |
| A12~A10/AP | A9 | A8 | A7 | A4 | A3 | 1 | 0 | 1 | Reserved |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | Reserved |
| | | | | | | 1 | 1 | 1 | Reserved |

**NOTES:**
1. RFU(Reserved for future use) should stay "0" during MRS cycle.
2. If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.

## Partial Array Self Refresh

1. In order to save power consumption, Mobile SDRAM has PASR option.
2. Mobile SDRAM supports 3 kinds of PASR in self refresh mode : Full Array, 1/2 of Full Array and 1/4 of Full Array.




## Internal Temperature Compensated Self Refresh(Internal TCSR)

1. In order to save power consumption, Mobile-DRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the two temperature range : Max 40 °C and Max 70 °C(for Commercial Temperature).
2. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.

| Temperature Range | Self Refresh Current (Icc6) | | | | | Unit |
|---|---|---|---|---|---|---|
| | - C | - L | - F | | | |
| | | | Full Array | 1/2 of Full Array | 1/4 of Full Array | |
| Max 70 °C | 1800 | 1500 | 1300 | 900 | 700 | uA |
| Max 40 °C | | | 850 | 600 | 500 | |

## B. POWER UP SEQUENCE

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
   - Apply VDD before or at the same time as VDDQ.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Issue a extended mode register set command to define DS or PASR operating type of the device after normal MRS.

EMRS cycle is not mandatory and the EMRS command needs to be issued only when DS or PASR is used.
The default state without EMRS command issued is the full driver strength and full array refreshed.
The device is now ready for the operation selected by EMRS.
For operating with DS or PASR , set DS or PASR mode in EMRS setting stage.
In order to adjust another mode in the state of DS or PASR mode, additional EMRS set is required but power up sequence is not needed again at this time. In that case, all banks have to be in idle state prior to adjusting EMRS set.

## C. BURST SEQUENCE

### 1. BURST LENGTH = 4

| Initial Address | | Sequential | | | | Interleave | | | |
|---|---|---|---|---|---|---|---|---|---|
| A1 | A0 | | | | | | | | |
| 0 | 0 | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 |
| 0 | 1 | 1 | 2 | 3 | 0 | 1 | 0 | 3 | 2 |
| 1 | 0 | 2 | 3 | 0 | 1 | 2 | 3 | 0 | 1 |
| 1 | 1 | 3 | 0 | 1 | 2 | 3 | 2 | 1 | 0 |

### 2. BURST LENGTH = 8

| Initial Address | | | Sequential | | | | | | | | Interleave | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A2 | A1 | A0 | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 1 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 0 | 3 | 2 | 5 | 4 | 7 | 6 |
| 0 | 1 | 0 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 0 | 1 | 6 | 7 | 4 | 5 |
| 0 | 1 | 1 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 |
| 1 | 0 | 0 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 1 | 0 | 1 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 4 | 7 | 6 | 1 | 0 | 3 | 2 |
| 1 | 1 | 0 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 4 | 5 | 2 | 3 | 0 | 1 |
| 1 | 1 | 1 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |