

**200 Volt, 0.40Ω, MEGA RAD HARD HEXFET**

International Rectifier's MEGA RAD HARD technology HEXFETs demonstrate excellent threshold voltage stability and breakdown voltage stability at total radiation doses as high as  $1 \times 10^6$  Rads (Si). Under **identical** pre- and post-radiation test conditions, International Rectifier's RAD HARD HEXFETs retain **identical** electrical specifications up to  $1 \times 10^5$  Rads (Si) total dose. At  $1 \times 10^6$  Rads (Si) total dose, under the same pre-dose conditions, only minor shifts in the electrical specifications are observed and are so specified in table 1. No compensation in gate drive circuitry is required. In addition, these devices are capable of surviving transient ionization pulses as high as  $1 \times 10^{12}$  Rads (Si)/Sec, and return to normal operation within a few microseconds. Single Event Effect (SEE) testing of International Rectifier RAD HARD HEXFETs has demonstrated virtual immunity to SEE failure. Since the MEGA RAD HARD process utilizes International Rectifier's patented HEXFET technology, the user can expect the highest quality and reliability in the industry.

RAD HARD HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits in space and weapons environments.

**Product Summary**

Part Number	BV <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
IRHN7230	200V	0.40Ω	9.0A
IRHN8230	200V	0.40Ω	9.0A

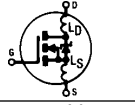
**Features:**

- Radiation Hardened up to  $1 \times 10^6$  Rads (Si)
- Single Event Burnout (SEB) Hardened
- Single Event Gate Rupture (SEGR) Hardened
- Gamma Dot (Flash X-Ray) Hardened
- Neutron Tolerant
- Identical Pre- and Post-Electrical Test Conditions
- Repetitive Avalanche Rating
- Dynamic  $dv/dt$  Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Light-weight

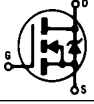
**Absolute Maximum Ratings**
**Pre-Radiation**

	Parameter	IRHN7230, IRHN8230	Units
I <sub>D</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 25°C	Continuous Drain Current	9.0	A
I <sub>D</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 100°C	Continuous Drain Current	6.0	
I <sub>DM</sub>	Pulsed Drain Current ①	36	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Max. Power Dissipation	75	W
	Linear Derating Factor	0.60	W/K ⑤
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	330 (see fig. 29)	mJ
I <sub>AR</sub>	Avalanche Current ①	9.0	A
EAR	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0 (see fig. 30)	V/ns
T <sub>J</sub>	Operating Junction	-55 to 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Package Mounting Surface Temperature	300 (for 5 seconds)	
	Weight	2.6 (typical)	g

Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0 mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	0.27	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0 mA
RDS(on)	Static Drain-to-Source	—	—	0.40	Ω	V <sub>GS</sub> = 12V, I <sub>D</sub> = 6.0A V <sub>GS</sub> = 12V, I <sub>D</sub> = 9.0A ④
	On-State Resistance	—	—	0.49		
VGS(th)	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0 mA
g <sub>fs</sub>	Forward Transconductance	3.0	—	—	S (r)	V <sub>DS</sub> > 15V, I <sub>DS</sub> = 6.0A ④
IDSS	Zero Gate Voltage Drain Current	—	—	25	μA	V <sub>DS</sub> = 0.8 x Max Rating, V <sub>GS</sub> = 0V V <sub>DS</sub> = 0.8 x Max Rating V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
		—	—	250		
IGSS	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
IGSS	Gate-to-Source Leakage Reverse	—	—	-100	nA	V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	50	nC	V <sub>GS</sub> = 12V, I <sub>D</sub> = 9.0A V <sub>DS</sub> = Max. Rating x 0.5 (see figures 23 and 31)
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	10		
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	20		
td(on)	Turn-On Delay Time	—	—	35	ns	V <sub>DD</sub> = 100V, I <sub>D</sub> = 9.0A, R <sub>G</sub> = 7.5Ω (see figure 28)
t <sub>r</sub>	Rise Time	—	—	80		
td(off)	Turn-Off Delay Time	—	—	60		
t <sub>f</sub>	Fall Time	—	—	46		
LD	Internal Drain Inductance	—	2.0	—	nH	<p>Measured from the drain lead, 6mm (0.25 in.) from package to center of die.</p> <p>Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.</p> 
LS	Internal Source Inductance	—	4.1	—		
C <sub>iss</sub>	Input Capacitance	—	1100	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V f = 1.0 MHz (see figure 22)
C <sub>oss</sub>	Output Capacitance	—	250	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	65	—		

## Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	9.0	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier. 
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	36		
V <sub>SD</sub>	Diode Forward Voltage	—	—	2.0	V	T <sub>j</sub> = 25°C, I <sub>S</sub> = 9A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	460	ns	T <sub>j</sub> = 25°C, I <sub>F</sub> = 9A, di/dt ≤ 100A/μs V <sub>DD</sub> ≤ 50V ④
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	5.0	μC	
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

## Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R <sub>thJC</sub>	Junction-to-Case	—	—	1.67	K/W <sup>®</sup>	soldered to a copper-clad PC board
R <sub>thJPCB</sub>	Junction-to-PC board	—	TBD	—		

**Radiation Performance of Mega Rad Hard HEXFETs**

International Rectifier Radiation Hardened HEX-FETs are tested to verify their hardness capability. The hardness assurance program at International Rectifier uses two radiation environments.

Every manufacturing lot is tested in a low dose rate (total dose) environment per MIL-STD-750, test method 1019. International Rectifier has imposed a standard gate voltage of 12 volts per note 6 and a  $V_{DS}$  bias condition equal to 80% of the device rated voltage per note 7 and figure 8b. Pre- and post-radiation limits of the devices irradiated to  $1 \times 10^5$  Rads (Si) are identical and are presented in Table 1, column 1, IRHN7230. Device performance limits at a post radiation level of  $1 \times 10^6$  Rads (Si) are presented in Table 1, column 2, IRHN8230. The values in Table 1 will be met for either of the two low dose rate test circuits that are used. Typical delta curves showing radiation response appear in figures 1 through 5. Typical post-radiation curves appear in figures 10 through 17.

Both pre- and post-radiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison. It should be noted that at a radiation level of  $1 \times 10^6$  Rads (Si), no change in limits are specified in DC parameters. At a radiation level of  $1 \times 10^6$  Rads (Si), leakage remains low and the device is usable with no change in drive circuitry required.

High dose rate testing may be done on a special request basis, using a dose rate up to  $1 \times 10^{12}$  Rads (Si)/Sec. Photocurrent and transient voltage waveforms are shown in figure 7 and the recommended test circuit to be used is shown in figure 9.

International Rectifier radiation hardened HEXFETs have been characterized in neutron and heavy ion Single Event Effects (SEE) environments. The effects on bulk silicon of the type used by International Rectifier on RAD HARD HEXFETs are shown in figure 6. Single Event Effects characterization is shown in Table 3.

**Table 1. Low Dose Rate** ⑥ ⑦

Parameter		IRHN7230		IRHN8230		Units	Test Conditions ⑩
		100K Rads (Si) min.	max.	1000K Rads (Si) min.	max.		
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	200	—	200	—	V	$V_{GS} = 0V, I_D = 1.0 \text{ mA}$
$V_{GS(th)}$	Gate Threshold Voltage ④	2.0	4.0	1.25	4.5		$V_{GS} = V_{DS}, I_D = 1.0 \text{ mA}$
$I_{GSS}$	Gate-to-Source Leakage Forward	—	100	—	100	nA	$V_{GS} = +20V$
$I_{GSS}$	Gate-to-Source Leakage Reverse	—	-100	—	-100		$V_{GS} = -20V$
$I_{DSS}$	Zero Gate Voltage Drain Current	—	25	—	25	$\mu A$	$V_{DS} = 0.8 \times \text{Max Rating}, V_{GS} = 0$
$R_{DS(on)1}$	Static Drain-to-Source ④ On-State Resistance One	—	0.40	—	0.53	$\Omega$	$V_{GS} = 12V, I_D = 6.0A$
$V_{SD}$	Diode Forward Voltage ④	—	1.6	—	1.6	V	$T_C = 25^\circ C, I_S = 9.0A, V_{GS} = 0V$

**Table 2. High Dose Rate** ⑧

Parameter		10 <sup>11</sup> Rads (Si)/sec			10 <sup>12</sup> Rads (Si)/sec			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
$V_{DSS}$	Drain-to-Source Voltage	—	—	160	—	—	160	V	Applied drain-to-source voltage during gamma-dot
$I_{PP}$		—	20	—	—	20	—	A	Peak radiation induced photo-current
$di/dt$		—	—	160	—	—	8.0	A/ $\mu$ sec	Rate of rise of photo-current
$L_1$		1.0	—	—	20	—	—	$\mu H$	Circuit inductance required to limit di/dt

**Table 3. Single Event Effects** ⑨

Parameter	Typ.	Units	Ion	LET (Si) (MeV/mg/cm <sup>2</sup> )	Fluence (ions/cm <sup>2</sup> )	Range ( $\mu m$ )	$V_{DS}$ Bias (V)	$V_{GS}$ Bias (V)
$BV_{DSS}$	200	V	Ni	28	$1 \times 10^5$	~41	160	-5

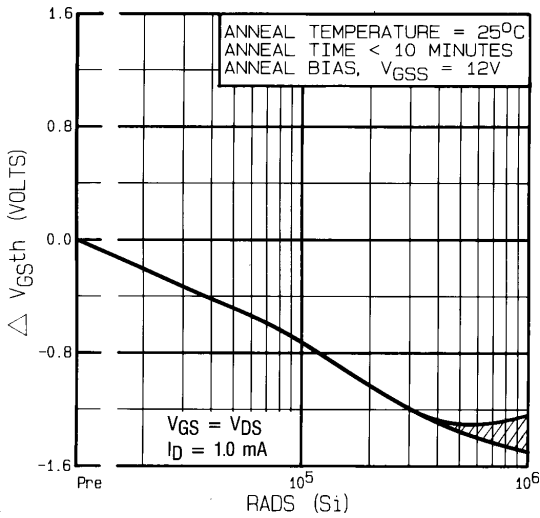


Figure 1. – Typical Response of Gate Threshold Voltage Vs. Total Dose Exposure

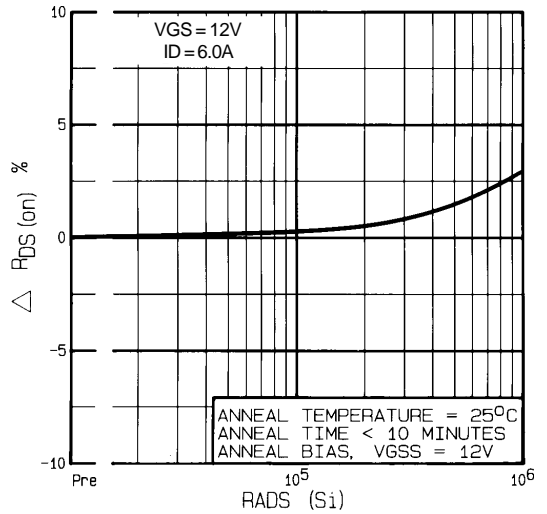


Figure 2. – Typical Response of On-State Resistance Vs. Total Dose Exposure

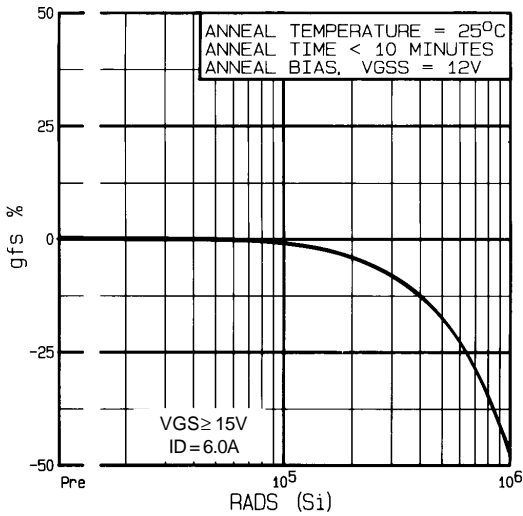


Figure 3. – Typical Response of Transconductance Vs. Total Dose Exposure

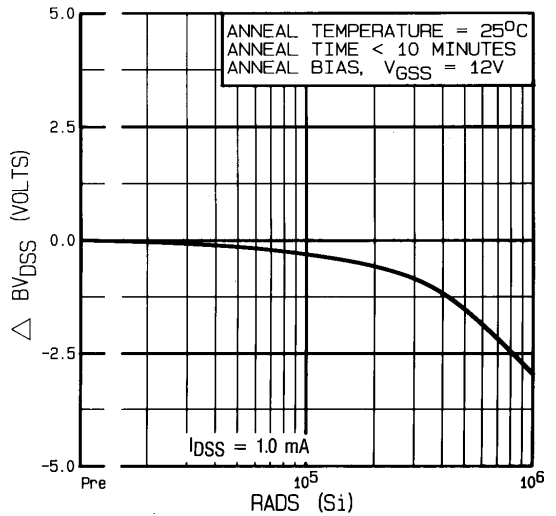


Figure 4. – Typical Response of Drain-to-Source Breakdown Vs. Total Dose Exposure

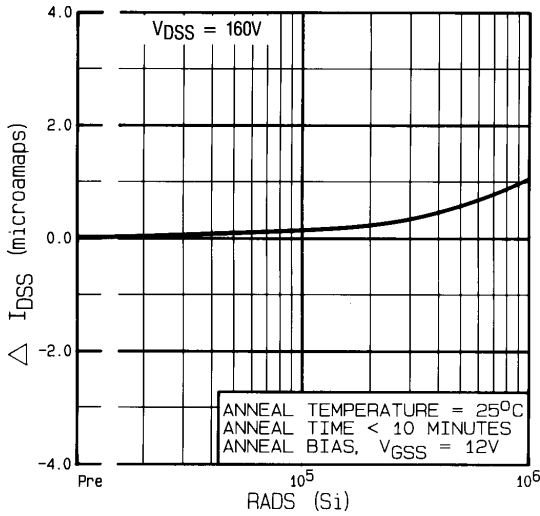


Figure 5. – Typical Zero Gate Voltage Drain Current Vs. Total Dose Exposure

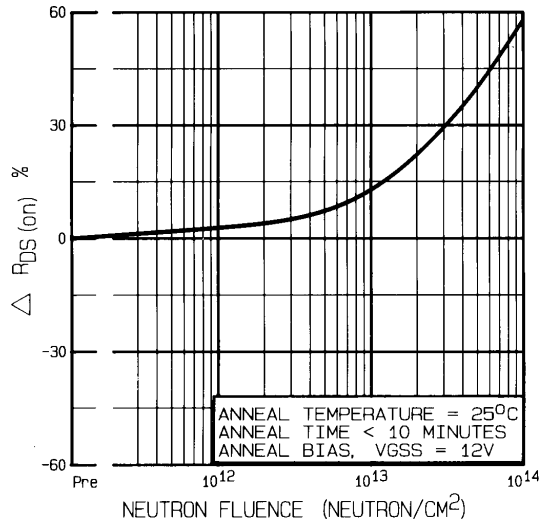


Figure 6. – Typical On-State Resistance Vs. Neutron Fluence Level

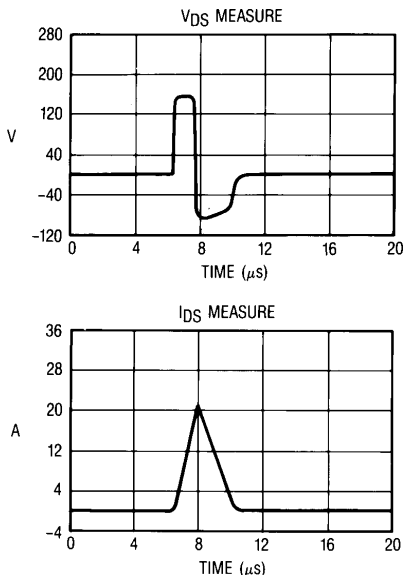


Figure 7. – Typical Transient Response of Rad Hard HEXFET During 1 x 10<sup>12</sup> Rad (Si)/Sec Exposure

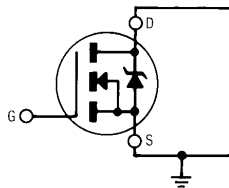


Figure 8a. – Gate Stress of VGSS Equals 12 Volts During Radiation

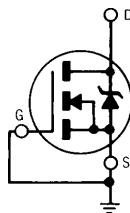


Figure 8b. – VDS Stress Equals 80% of BVDS During Radiation

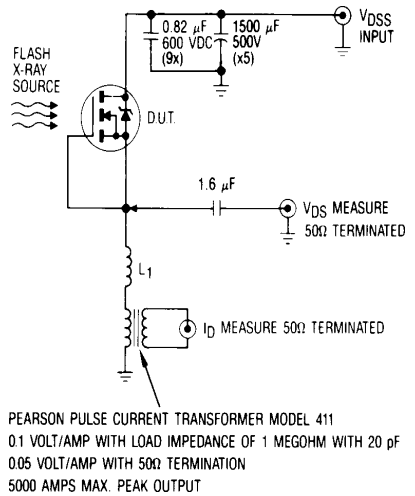


Figure 9. – High Dose Rate (Gamma Dot) Test Circuit

# IRHN7230, IRHN8230 Devices

# Radiation Characteristics

Note: Bias Conditions during radiation;  $V_{GS} = 12\text{ V}_{dc}$ ,  $V_{DS} = 0\text{ V}_{dc}$

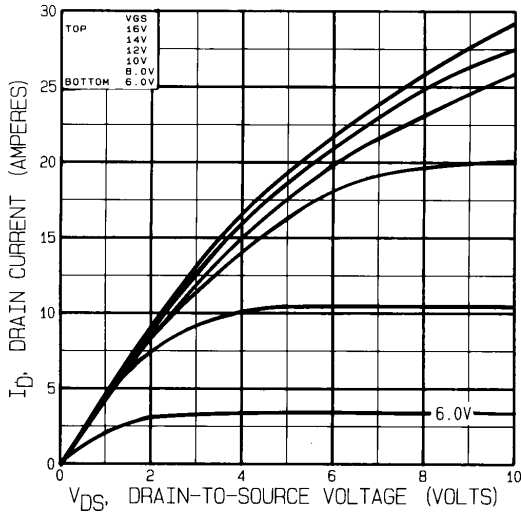


Figure 10. – Typical Output Characteristics Pre-Radiation

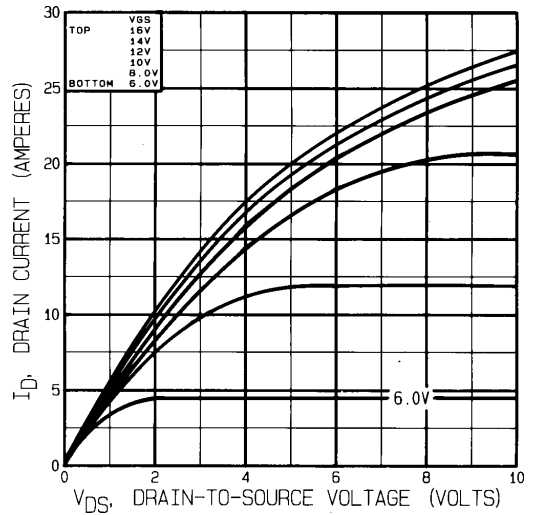


Figure 11. – Typical Output Characteristics Post-Radiation 100K Rads (Si)

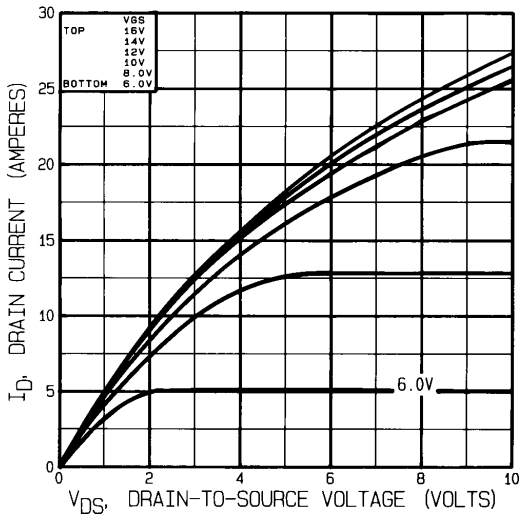


Figure 12. – Typical Output Characteristics Post-Radiation 300K Rads (Si)

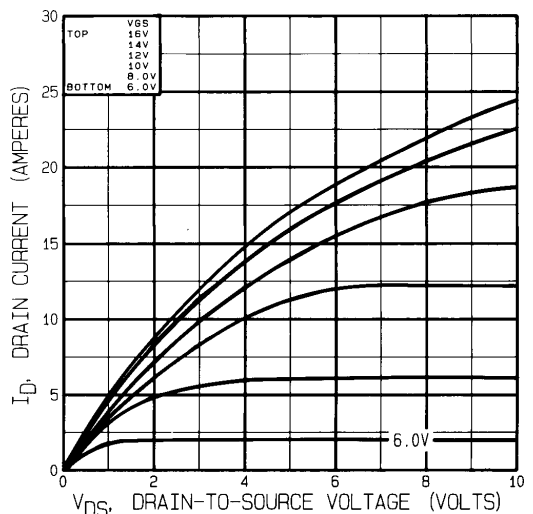


Figure 13. – Typical Output Characteristics Post-Radiation 1 Mega Rads (Si)

Note: Bias Conditions during radiation;  $V_{GS} = 0\text{ V}_{dc}$ ,  $V_{DS} = 400\text{ V}_{dc}$

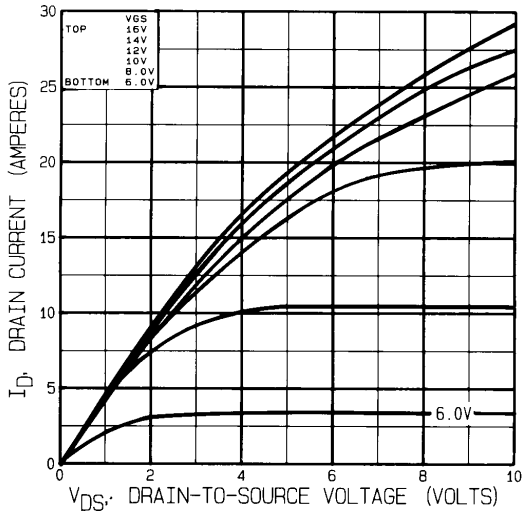


Figure 14. – Typical Output Characteristics Pre-Radiation

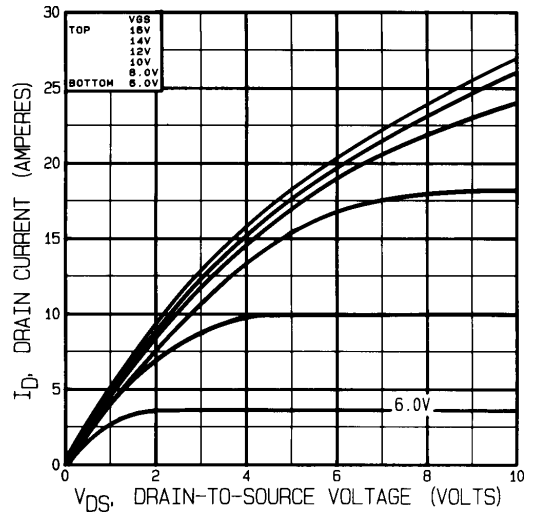


Figure 15. – Typical Output Characteristics Post-Radiation 100K Rads (Si)

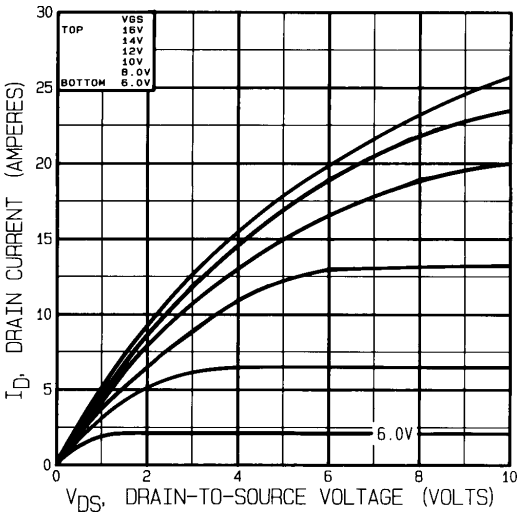


Figure 16. – Typical Output Characteristics Post-Radiation 300K Rads (Si)

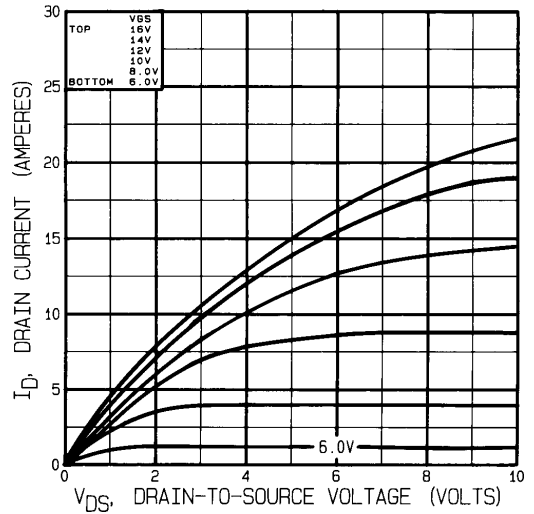


Figure 17. – Typical Output Characteristics Post-Radiation 1 Mega Rads (Si)

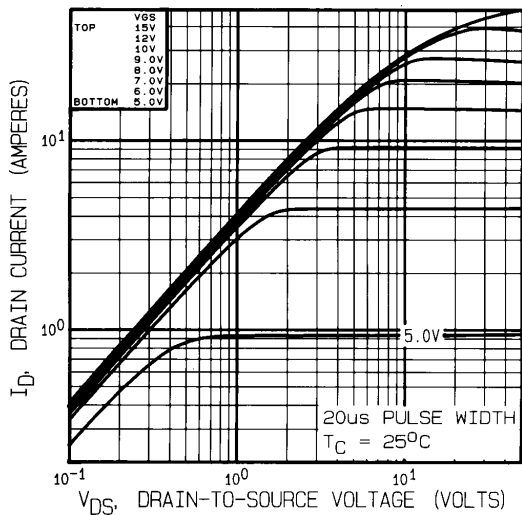


Figure 18. – Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

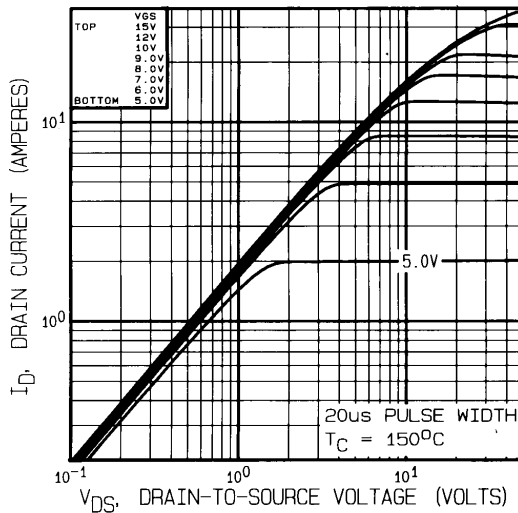


Figure 19. – Typical Output Characteristics,  $T_C = 150^\circ\text{C}$

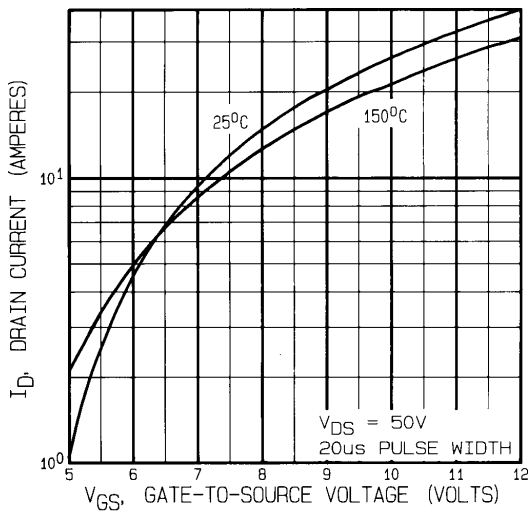


Figure 20. – Typical Transfer Characteristics

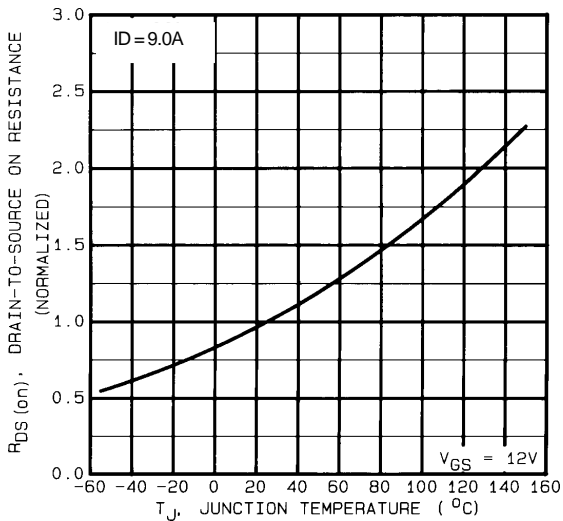


Figure 21. – Normalized On-Resistance Vs. Temperature



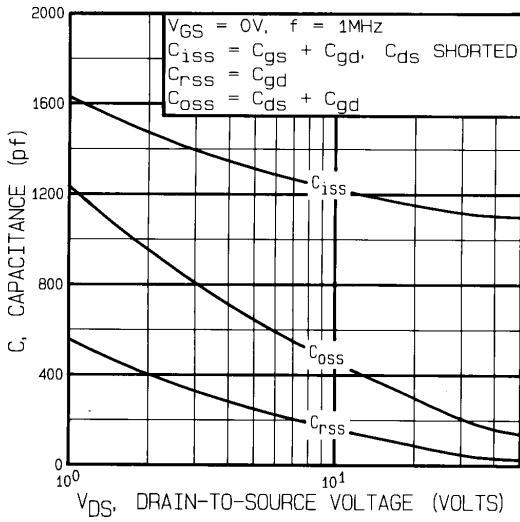


Figure 22. – Typical Capacitance Vs. Drain-to-Source Voltage

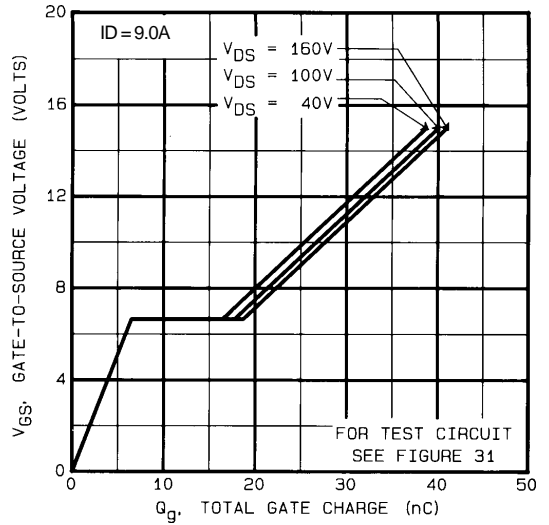


Figure 23. – Typical Gate Charge Vs. Gate-to-Source Voltage

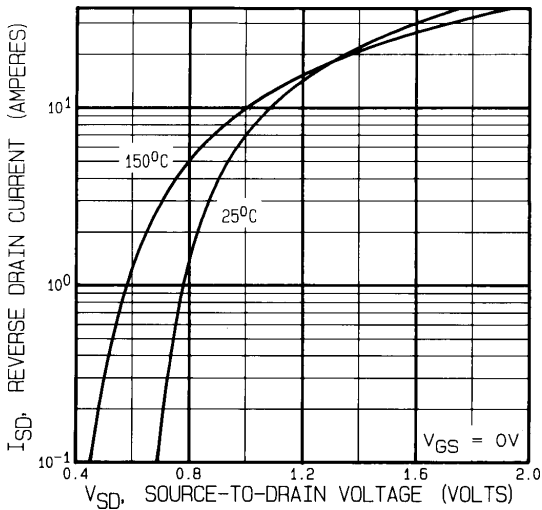


Figure 24. – Typical Source-Drain Diode Forward Voltage

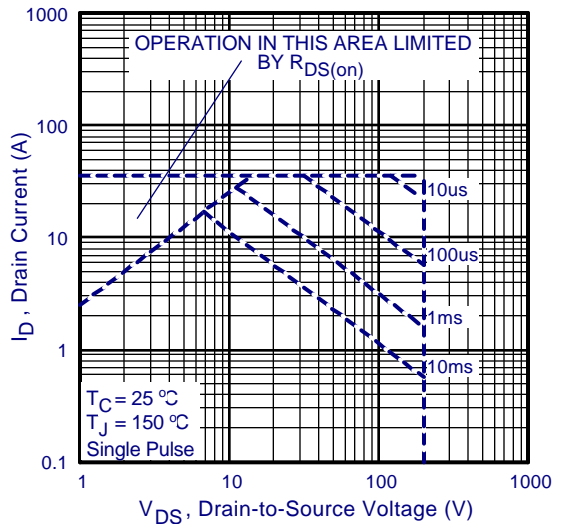


Figure 25. – Maximum Safe Operating Area

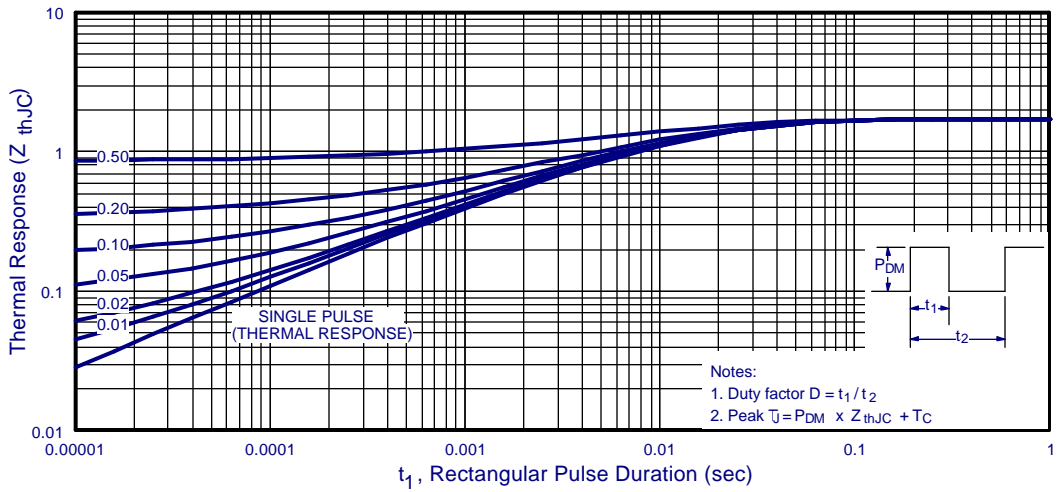


Figure 26. – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

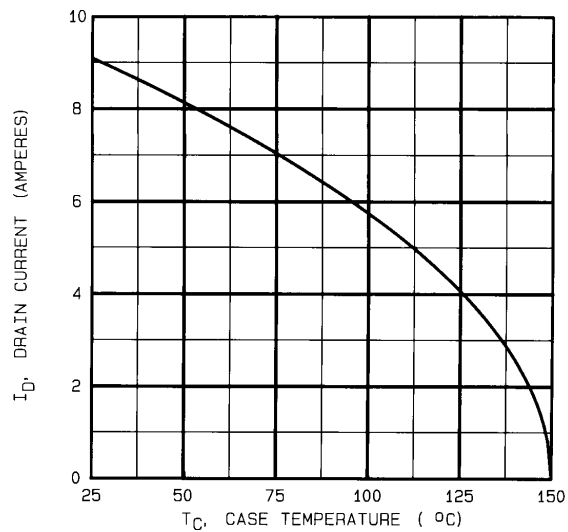


Figure 27. – Maximum Drain Current Vs. Case Temperature

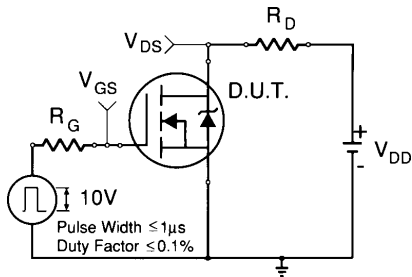


Figure 28a. – Switching Time Test Circuit

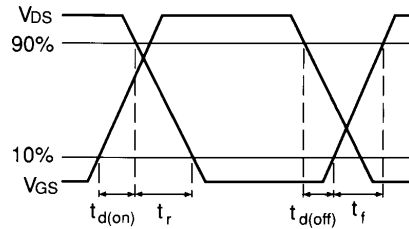


Figure 28b. – Switching Time Waveforms

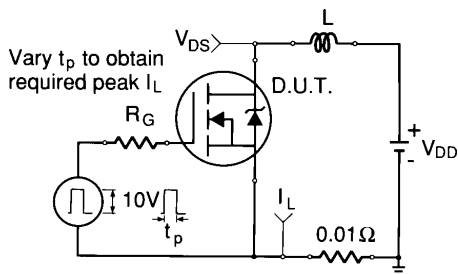


Figure 29a. – Unclamped Inductive Test Circuit

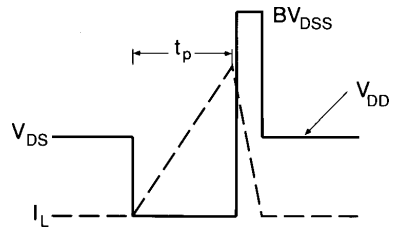


Figure 29b. – Unclamped Inductive Waveforms

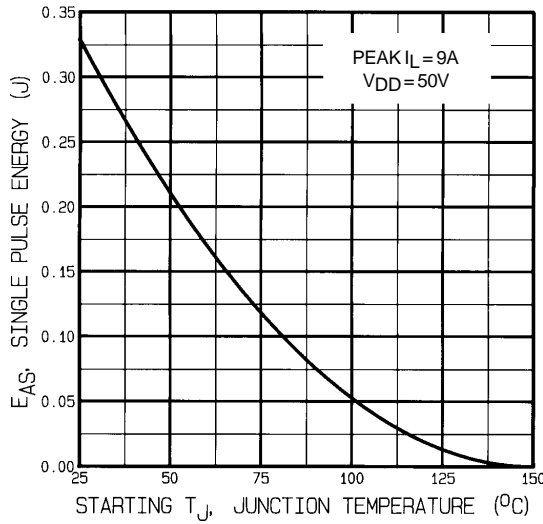


Figure 29c. – Maximum Avalanche Energy Vs. Starting Junction Temperature

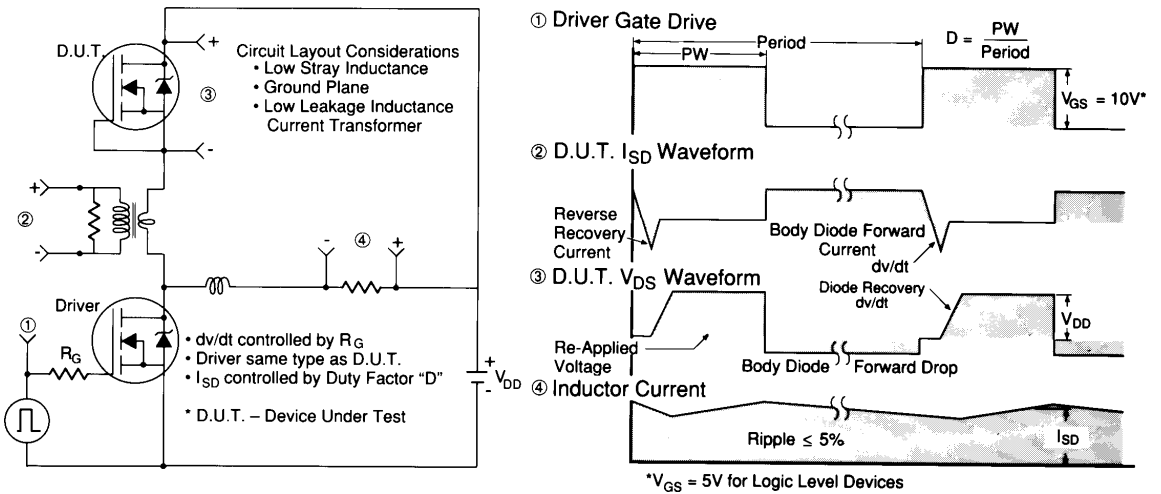


Figure 30. – Peak Diode Recovery  $dv/dt$  Test Circuit

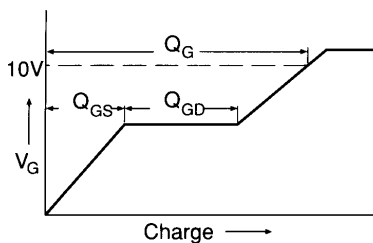


Figure 31a. – Basic Gate Charge Waveform

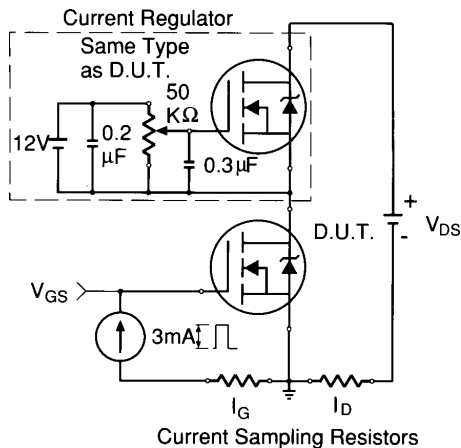


Figure 31b. – Gate Charge Test Circuit

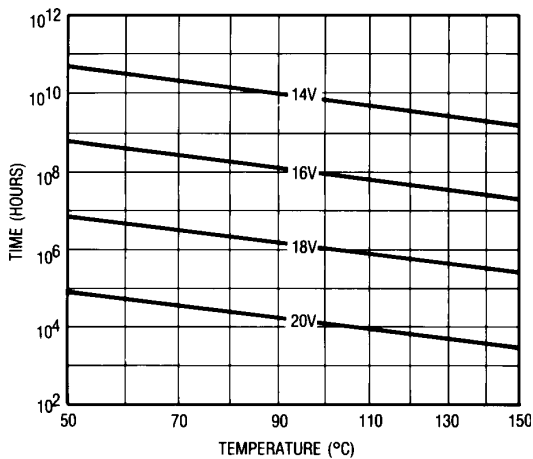
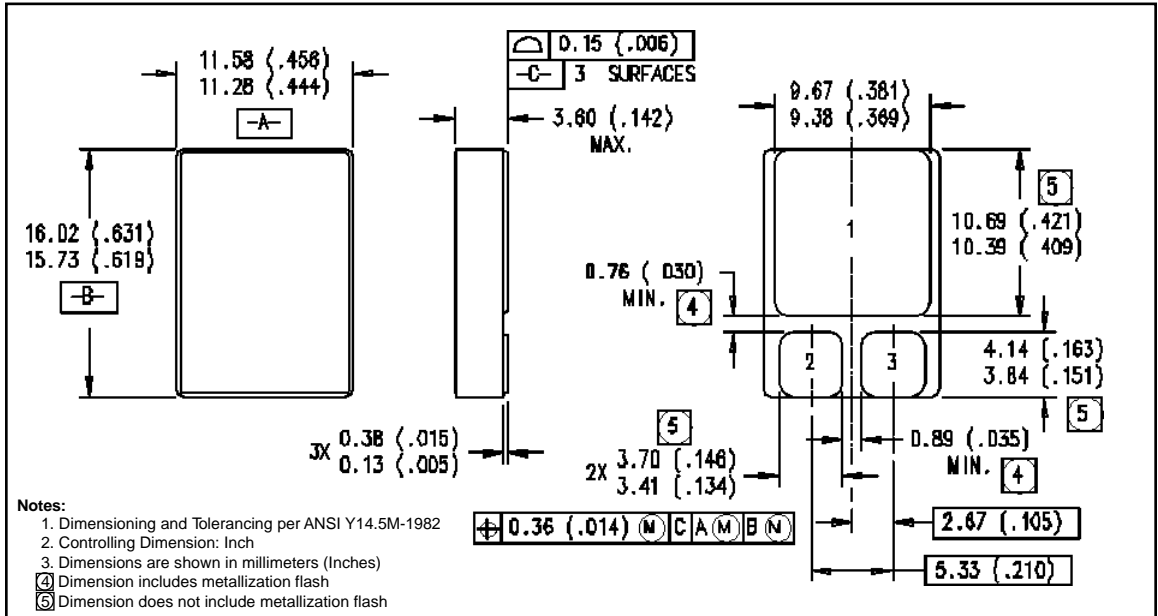


Figure 32 – Typical Time to Accumulated 1% Failure

- ① Repetitive Rating; Pulse width limited by maximum junction temperature. (figure 26)  
Refer to current HEXFET reliability report.
- ② @  $V_{DD} = 50V$ , Starting  $T_J = 25^\circ C$ ,  
 $E_{AS} = [0.5 * L * (I_L^2) * [BV_{DSS} / (BV_{DSS} - V_{DD})]]$   
Peak  $I_L = 9.0A$ ,  $V_{GS} = 12V$ ,  $25 \leq R_G \leq 200\Omega$
- ③  $I_{SD} \leq 9.0A$ ,  $di/dt \leq 120 A/\mu s$ ,  
 $V_{DD} \leq BV_{DSS}$ ,  $T_J \leq 150^\circ C$   
Suggested  $R_G = 7.5\Omega$
- ④ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$
- ⑤  $K/W = ^\circ C/W$   
 $W/K = W/^\circ C$
- ⑥ **Total Dose Irradiation with  $V_{GS}$  Bias.**  
 $+12$  volt  $V_{GS}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, method 1019. (figure 8a)
- ⑦ **Total Dose Irradiation with  $V_{DS}$  Bias.**  
 $V_{DS} = 0.8 \times$  rated  $BV_{DSS}$  (pre-radiation) applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, method 1019. (figure 8b)
- ⑧ This test is performed using a flash x-ray source operated in the e-beam mode (energy  $\sim 2.5$  MeV), 30 nsec pulse. (figure 9)
- ⑨ Study sponsored by NASA. Evaluation performed at Brookhaven National Labs.
- ⑩ All Pre-Radiation and Post-Radiation test conditions are **identical** to facilitate direct comparison for circuit applications.

Case Outline and Dimensions – SMD-1



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