

IN24LC16

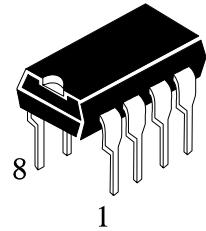
16K SERIAL EEPROM WITH I²C BUS

DESCRIPTION

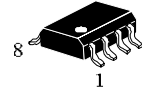
The IN24LC16 is a 16K bit Electrically Erasable PROM. The device is organized as eight blocks of 256 x 8 bit memory with a 2-wire serial interface. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5 μ A and 1 mA respectively. The IN24LC16 also has a page-write capability for up to 16 bytes of data. The IN24LC16 is available in the standard 8-pin DIP surface mount SO.

FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
 - 1 mA active current typical
 - 10 μ A standby current typical at 5.5V
 - 5 μ A standby current typical at 3.0V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- 2-wire serial interface bus, I²C compatible
- Schmitt trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (E-temp) and 400 kHz (C/I-temp) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- 1,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-lead SOIC,



IN24LC16N Plastic DIP

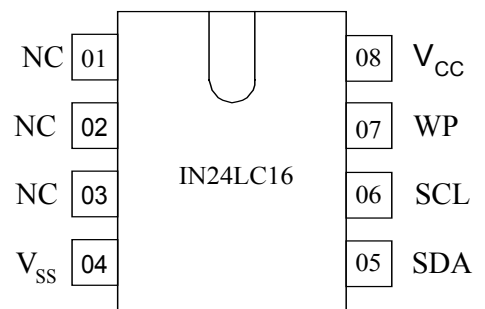


IN24LC16D SO

T_A = от -40 до 85 °C

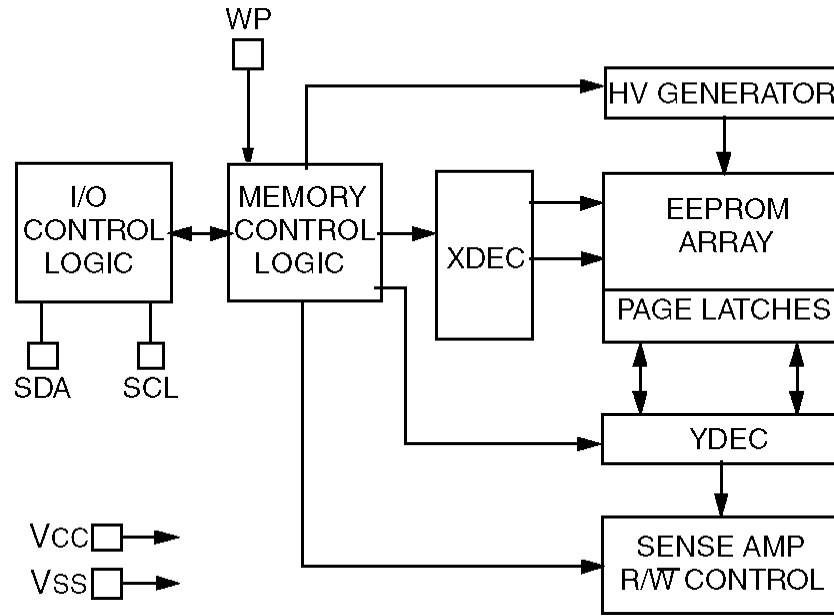
Pinning

Pin	Name	Function
01	NC	Not connected
02	NC	Not connected
03	NC	Not connected
04	V _{SS}	Negative power supply input
05	SDA	Serial Address/Data I/O
06	SCL	Serial Clock
07	WP	Write Protect Input
08	V _{CC}	Power Supply input



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BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Symbol	Parameter	Value		Unit
		min	max	
V_{CC}	Supply voltage	0	7.0	V
V_I	Input voltage	-0.3	$V_{CC}+1V$	V
T	Storage temperature	-65	150	°C
Ta	Ambient temperature	-65	125	°C

Maximum Ratings

Symbol	Parameter	Value		Unit
		min	max	
V_{CC}	Supply voltage	2.5	5.5	V
I_{OL}	Low level output current	-	3.0	mA
T	Operating ambient temperature	-40	85	°C

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DC CHARACTERISTICS ($V_{CC} = +2.5V$ to $+5.5V$ $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$)

Symbol	Parameter	Mode of measurements	Value		Unit
			Min	Max	
I_{CCS}	Standby current	$V_{CC} = 3.0 V$ $V_{CC} = 5.5 V$ $SDA=SCL= V_{CC}$	-	30 100	μA
$I_{CCO(RD)}$	Operating current (read mode)	$f_{SCL} = 400 kHz$ $V_{CC} = 5.5 V$		1.0	mA
$I_{CCO(EWR)}$	Operating current (erase/write mode)	$f_{SCL} = 400 kHz$ $V_{CC} = 5.5 V$		3.0	
I_{LI}	Input leakage current	$V_{IN} = (0.1 - 5.5) V$	-10	10	μA
I_{LO}	Output leakage current	$V_{OUT} = (0.1- 5.5) V$	-10	10	
C_{IN}	Input pin capacitance	$V_{CC} = 5.0 V$, $f = 1 MHz$ $T = 25^{\circ}C$	-	10	pF
C_{out}	Output pin capacitance	$V_{CC} = 5.0V$, $f = 1 MHz$ $T = 25^{\circ}C$		10	
V_{HYS}	Hysteresis of Schmitt trigger inputs		0.05 V_{CC}	-	V
V_{OL}	Low level output voltage	$I_{OL} = 3.0 mA$, $V_{CC} = 2.5 V$	-	0.4	
t_s	Time of data storage	$T = 25^{\circ}C$	200	-	years
$N_{C(EWR)}$	Number of ERASE/WRITE cycles guaranteed		10000 00		pcs

AC CHARACTERISTICS

Symbol	Parameter	Mode of measurements	Standard mode ($V_{CC}=2.5 \div 5.5 V$)		Speed mode ($V_{CC}=4.5 \div 5.5 V$)		Unit
			min	max	min	max	
t_{SP}	Input filter spike suppression (SDA and SCL pins)		-	50	-	50	ns
t_{OF}	Output fall time from VIH minimum to VIL maximum	$I_{OL} = 3 mA$, $C_{B*} < 100 pF$		250	$20+0.1C_{B*}$	250	
$t_{A(SCL)}$	Output valid from clock	Note 2		3500	-	900	
$t_{CY(EWR)}$	Write cycle time (byte or page)			10		10	ms
f_{SCL}	Clock frequency	Note 2	-	100	-	400	kHz
t_{BUF}	Bus free time: Time the bus must be free before a new transmission can start		4.7	-	1.3	-	μs
$t_{SU,STA}$	START condition setup time	For recurrent signal Note 2	4.7		0.6		

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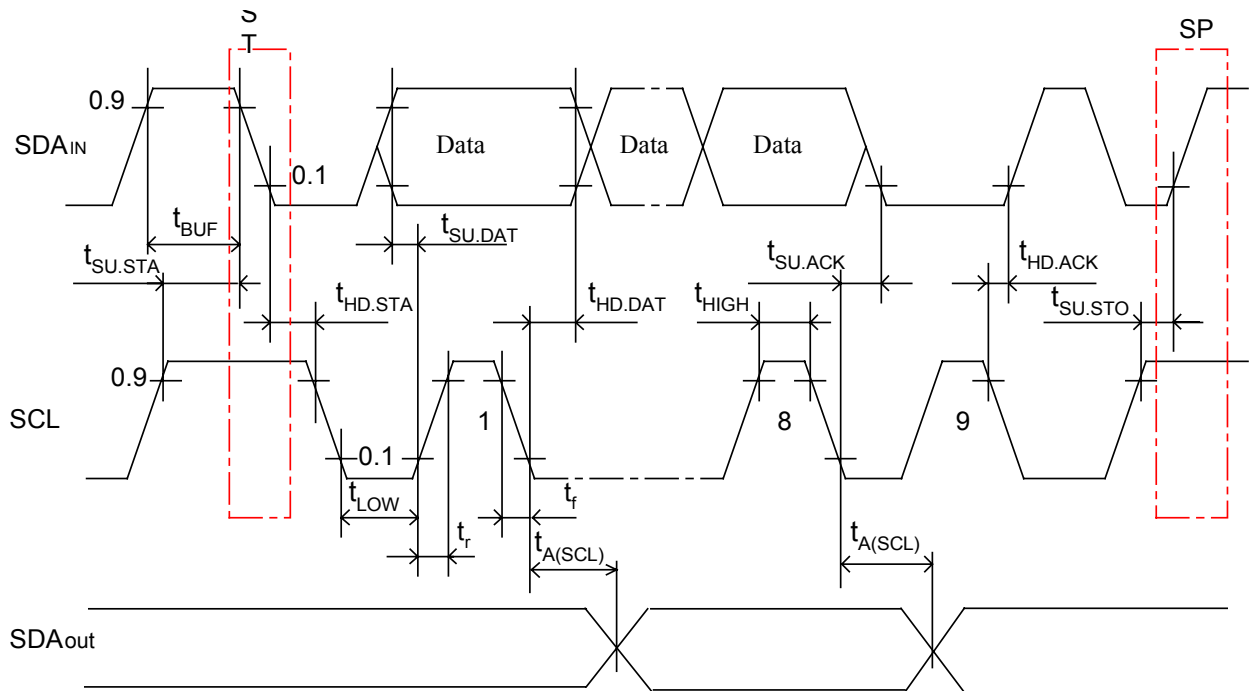
Symbol	Parameter	Mode of measurements	Standard mode ($V_{CC}=2.5 \div 5.5 V$)		Speed mode ($V_{CC}=4.5 \div 5.5 V$)		Unit
			min	max	min	max	
t_{HD_STA}	START condition hold time	Note 2	4.0		0.6		ns
t_{LOW}	Clock high time		4.7		1.3		
t_{HIGH}	Clock low time		4.0		0.6		
t_r	SDA and SCL rise time		-	1000	-	300	
t_f	SDA and SCL fall time			300	300		
t_{HD_DAT}	Data input hold time	Note 1, 2	0	-	0	-	
t_{SU_DAT}	Data input setup time	Note 2	250		100		
t_{SU_STO}	STOP condition setup time		4		0.6		us

Notes

- As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
- This parameter is not tested but guaranteed by characterization.

* C_B - total bus capacity

BUS TIMING DATA



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FUNCTIONAL DESCRIPTION

The 24LC16B supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC16B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

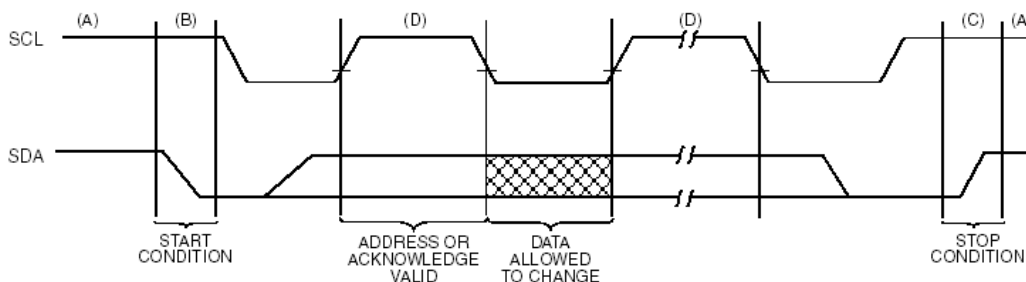
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC16B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC16B) will leave the data line HIGH to enable the master to generate the STOP condition.

DATA TRANSFER SEQUENCE ON THE SERIAL BUS



Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24LC16B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect

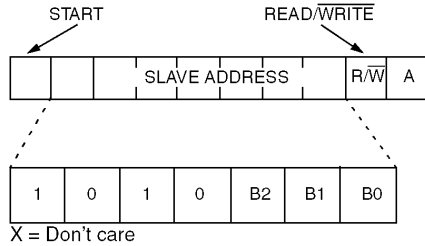
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the three most significant bits of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore the protocol can support only one 24LC16B per system.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC16B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24LC16B will select a read or write operation.

Operation	Control Code	Block Select	R/W
Read	1010	Block Address	1
Write	1010	Block Address	0

CONTROL BYTE ALLOCATION



WRITE OPERATION

Byte Write

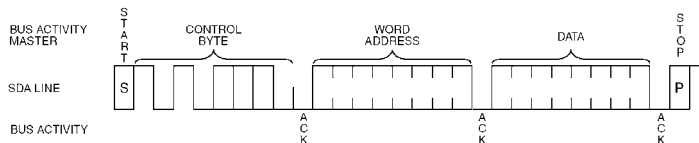
Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/W bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC16B. After receiving another acknowledge signal from the 24LC16B the master device will transmit the data word to be written into the addressed memory location. The 24LC16B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC16B will not generate acknowledge signals (Figure 4-1).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC16B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to 16 data bytes to the 24LC16B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin.

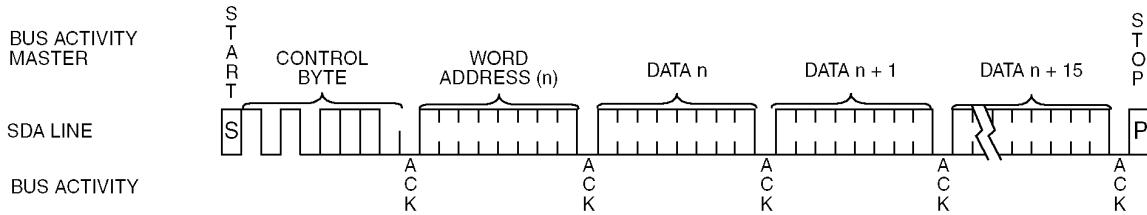
Note: Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

BYTE WRITE



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PAGE WRITE



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/W = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command.

WRITE PROTECTION

The 24LC16B can be used as a serial ROM when the WP pin is connected to VCC. Programming will be inhibited and the entire memory will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24LC16B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n , the next current address read operation would access data from address $n + 1$. Upon receipt of the slave address with R/W bit set to one, the 24LC16B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC16B discontinues transmission.

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC16B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a one. The 24LC16B will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC16B discontinues transmission (Figure 7-2).

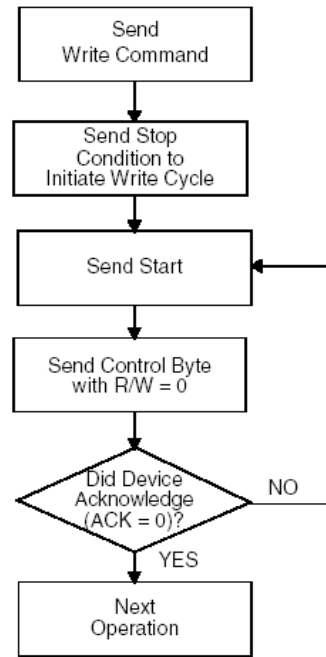
Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC16B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC16B to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24LC16B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

ACKNOWLEDGE POLLING FLOW

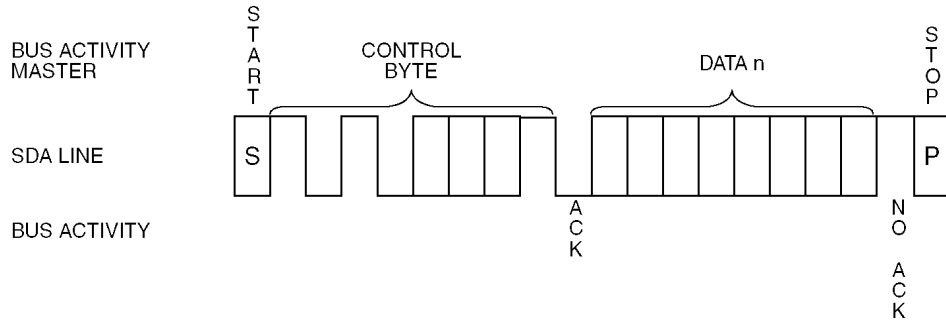


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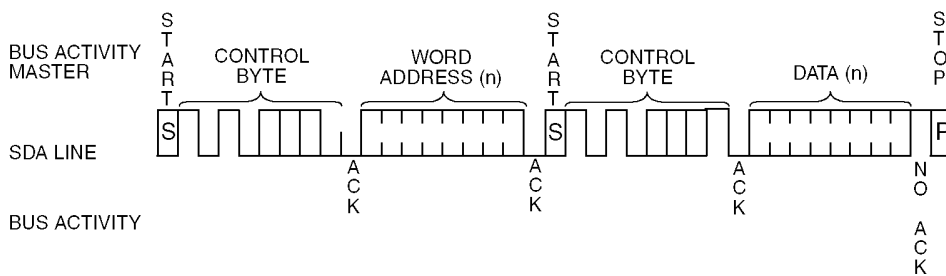
The 24LC16B employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

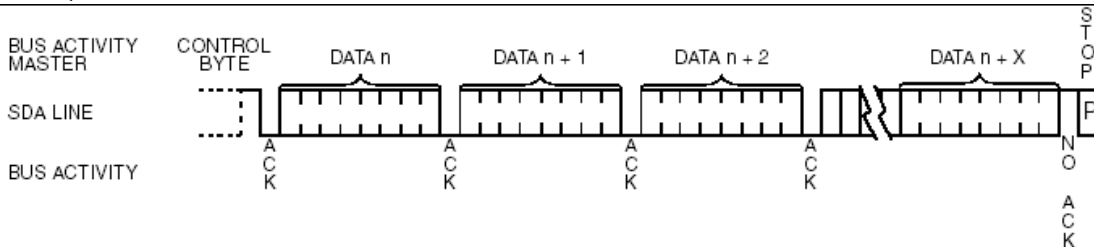
CURRENT ADDRESS READ



RANDOM READ



: SEQUENTIAL READ



PIN DESCRIPTIONS

SDA Serial Address/Data Input/Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10K Ω for 100 kHz, 2 K Ω for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP

This pin must be connected to either VSS or VCC.

If tied to Vss normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

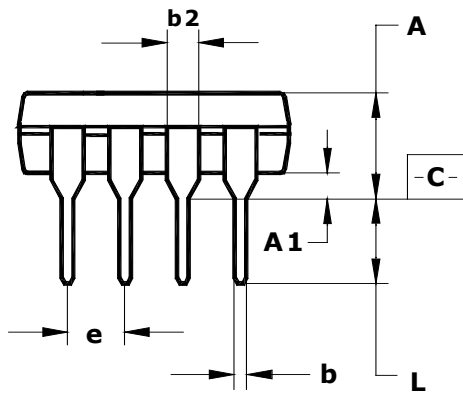
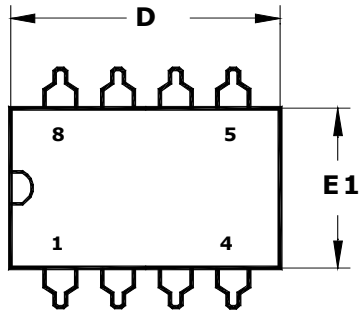
This feature allows the user to use the 24LC16B as a serial ROM when WP is enabled (tied to VCC).

A0, A1, A2

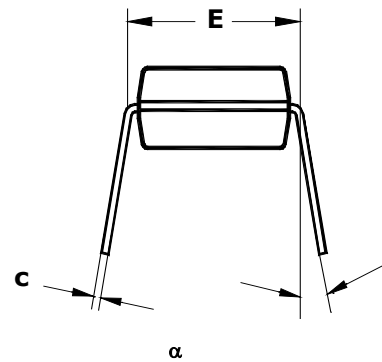
These pins are not used by the 24LC16B. They may be left floating or tied to either VSS or VCC.

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N SUFFIX PLASTIK DIP
(MS-001BA)



Mounting plate

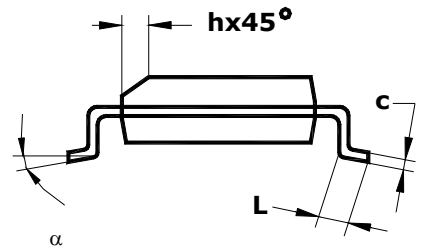
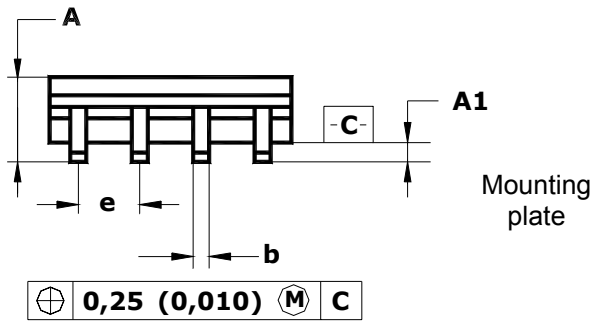
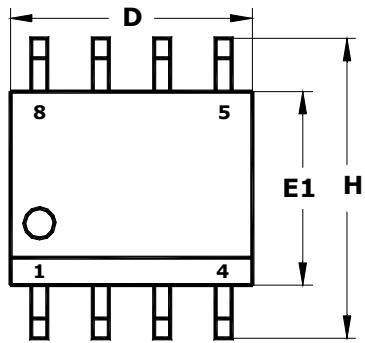


⊕ 0,25 (0,010) ⊕ M C

	D	E1	A	b	b2	e	α	L	E	c	A1
mm											
min	9.02	6.07	—	0.36	1.14	2.54	0	2.93	7.62	0.20	0.38
max	10.16	7.11	5.33	0.56	1.78		15	3.81	8.26	0.36	—
inches											
min	0.355	0.240	—	0.014	0.045	0.1	0	0.115	0.300	0.008	0.015
max	0.400	0.280	0.210	0.022	0.070		15	0.150	0.325	0.014	—

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N SUFFIX PLASTIK SOP
(MS-012AA)



⊕ 0,25 (0,010) Ⓜ C

	D	E1	H	b	e	α	A	A1	c	L	h
mm											
min	4.80	3.80	5.80	0.33	1.27	0°	1.35	0.10	0.19	0.41	0.25
max	5.00	4.00	6.20	0.51		8°	1.75	0.25	0.25	1.27	0.50
inches											
min	0.1890	0.1497	0.2284	0.013	0.100	0°	0.0532	0.0040	0.0075	0.016	0.0099
max	0.1968	0.1574	0.2440	0.020		8°	0.0688	0.0090	0.0098	0.050	0.0196