Integrated Circuit Systems, Inc.

ICS8702
LOW SKEW ÷1, ÷2 CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS8702 is a very low skew, ÷1, ÷2 Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8702 is designed to translate any differential signal levels to LVCMOS levels. True or inverting, single-ended to LVCMOS translation can be achieved with a resistor bias on the nCLK or CLK inputs, respectively. The effective fanout can be increased from 20 to 40 by utilizing the ability of the outputs to drive two series terminated lines.

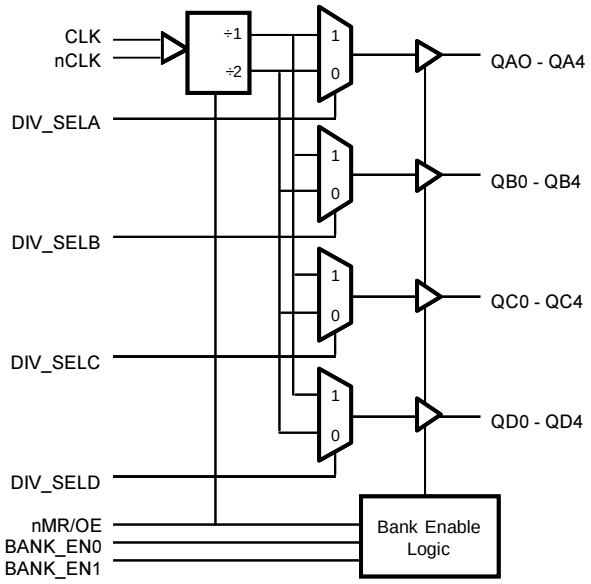
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The bank enable inputs, BANK_EN0:1, supports enabling and disabling each bank of outputs individually. The master reset input, nMR/OE, resets the internal frequency dividers and also controls the enabling and disabling of all outputs simultaneously.

The ICS8702 is characterized at 3.3V and mixed 3.3V input supply, and 2.5V output supply operating modes. Guaranteed bank, output, multiple frequency and part-to-part skew characteristics make the ICS8702 ideal for those clock distribution applications demanding well defined performance and repeatability.

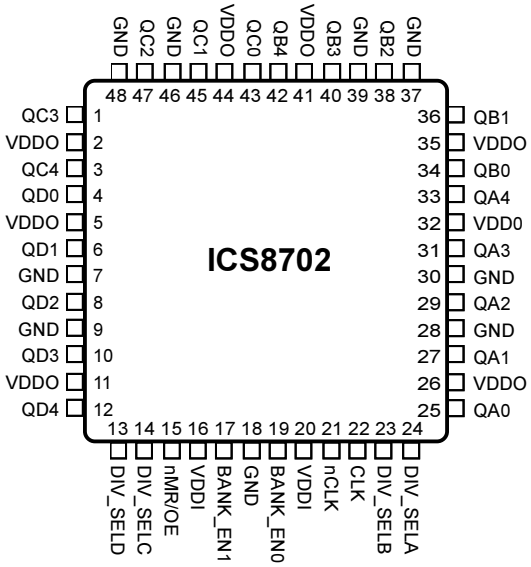
FEATURES

- 20 LVCMOS outputs, 7Ω typical output impedance
- Output frequency up to 250 MHz
- 150ps bank skew, 200ps output, 250ps multiple frequency skew, 650ps part-to-part skew
- Translates any differential input signal (PECL, HSTL, LVDS) to LVCMOS levels without external bias networks
- Translates any single-ended input signal to LVCMOS levels with a resistor bias on nCLK input
- Translates any single-ended input signal to inverted LVCMOS levels with a resistor bias on CLK input
- LVCMOS / LVTTL control inputs
- Bank enable logic allows unused banks to be disabled in reduced fanout applications
- 3.3V or mixed 3.3V input, 2.5V output operating supply modes
- 48 lead low-profile QFP (LQFP), 7mm x 7mm x 1.4mm package body, 0.5mm package lead pitch
- 0°C to 70°C ambient operating temperature
- Other divide values available on request

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
2, 5, 11, 26, 32, 35, 41, 44	VDDO	Power		Output power supply. Connect to 3.3V or 2.5V.
7, 9, 28, 30, 37, 39, 46, 48	GND	Power		Output power supply. Connect to ground.
16, 20	VDDI	Power		Input power supply. Connect to 3.3V.
18	GND	Power		Input power supply. Connect to ground.
25, 27, 29, 31, 33	QA0, QA1, QA2, QA3, QA4	Output		Bank A outputs. 7Ω typical output impedance.
34, 36, 38, 40, 42	QB0, QB1, QB2, QB3, QB4	Output		Bank B outputs. 7Ω typical output impedance.
43, 45, 47, 1, 3	QC0, QC1, QC2, QC3, QC4	Output		Bank C outputs. 7Ω typical output impedance.
4, 6, 8, 10, 12	QD0, QD1, QD2, QD3, QD4	Output		Bank D outputs. 7Ω typical output impedance.
22	CLK	Input	Pulldown	Non-inverting differential clock input. Accepts any differential levels.
21	nCLK	Input	Pullup	Inverting differential clock input. Accepts any differential levels.
13	DIV_SELD	Input	Pullup	Controls frequency division for bank D outputs. LVCMOS interface levels.
14	DIV_SELC	Input	Pullup	Controls frequency division for bank C outputs. LVCMOS interface levels.
23	DIV_SELB	Input	Pullup	Controls frequency division for bank B outputs. LVCMOS interface levels.
24	DIV_SELA	Input	Pullup	Controls frequency division for bank A outputs. LVCMOS interface levels.
17, 19	BANK_EN1, BANK_EN0	Input	Pullup	Enables and disables outputs by banks. LVCMOS interface levels.
15	nMR/OE	Input	Pullup	Asynchronous master reset. Resets clock dividers. Enables and disables all outputs. LVCMOS interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance					pF
RPULLUP	Input Pullup Resistor			51		KΩ
RPULLDOWN	Input Pulldown Resistor			51		KΩ
CPD	Power Dissipation Capacitance (per output)	VDDI, VDDO = 3.465V				pF
		VDDI = 3.465V, VDDO = 2.625V				pF
ROUT	Output Impedance			7		Ω

TABLE 3A. CONTROL INPUTS FUNCTION TABLE

Inputs				Outputs				
nMR/OE	BANK_EN1	BANK_EN0	DIV_SELx	QA0 - QA4	QB0 - QB4	QC0 - QC4	QD0 - QD4	Qx frequency
0	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z	zero
1	0	0	0	Active	Hi Z	Hi Z	Hi Z	fIN/2
1	1	0	0	Active	Active	Hi Z	Hi Z	fIN/2
1	0	1	0	Active	Active	Active	Hi Z	fIN/2
1	1	1	0	Active	Active	Active	Active	fIN/2
1	0	0	1	Active	Hi Z	Hi Z	Hi Z	fIN
1	1	0	1	Active	Active	Hi Z	Hi Z	fIN
1	0	1	1	Active	Active	Active	Hi Z	fIN
1	1	1	1	Active	Active	Active	Active	fIN

TABLE 3B. CLOCK INPUTS FUNCTION TABLE

Inputs			Outputs	Input to Output Mode	Polarity
nMR/OE	CLK	nCLK	Qx0 thru Qx4		
1	0	1	LOW	Differential to Single Ended	Non Inverting
1	1	0	HIGH	Differential to Single Ended	Non Inverting
1	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
1	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
1	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
1	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting

NOTE 1: Single ended input use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS input levels the recommended input bias network is a resistor to VDDI, a resistor of equal value to ground and a 0.1µF capacitor from the input to ground. The resulting switch point is approximately VDD/2 ± 300mV.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD + 0.5V
Outputs	-0.5V to VDDO + 0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. DC ELECTRICAL CHARACTERISTICS, VDDI=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage			3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage			3.135	3.3	3.465	V
VIH	Input High Voltage	All except CLK, nCLK	VDDI = 3.465V	2		3.8	V
VIL	Input Low Voltage	All except CLK, nCLK;	VDDI = 3.135V	-0.3		0.8	V
VPP	Peak-to-Peak Input Voltage	CLK, nCLK		0.15		1.3	V
VCMR	Common Mode Input Voltage; NOTE 1	CLK, nCLK	LVPECL Levels	1.8		2.4	V
			DCM, HSTL, LVDS, SSTL Levels	0.31		1.3	V
IIH	Input High Current	All except CLK	VDDI = VIN = 3.465V			5	µA
		CLK	VDDI = VIN = 3.465V			150	µA
IIL	Input Low Current	All except CLK	VDDI = 3.465, VIN = 0V	-150			µA
		CLK	VDDI = 3.465, VIN = 0	-5			µA
IDD	Quiescent Power Supply Current		VDDI = VIH = 3.465V VIL = 0V			70	mA
VOH	Output High Voltage		VDDI = VDDO = 3.135V IOH = -36mA	2.6			V
VOL	Output Low Voltage		VDDI = VDDO = 3.135V IOL = 36mA			0.5	V

NOTE 1: Common mode input voltage for LVPECL is defined as the minimum VIH. The LVPECL values noted in Table 4A are for VCCI = 3.3V. VCMR for LVPECL will vary 1:1 with VCCI. Common mode input voltage for DCM, HSTL, LVDS and SSTL is defined as the crossover voltage. See Figure 1.

TABLE 5A. AC ELECTRICAL CHARACTERISTICS, VDDI=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				250	MHz
tpLH	Propagation Delay, Low-to-High	0MHZ < f ≤ 200MHz	2.2		3.5	ns
tpHL	Propagation Delay, High-to-Low	0MHZ < f ≤ 200MHz	2.2		3.5	ns
tsk(b)	Bank Skew; NOTE 2	Measured on rising edge at VDDO/2			150	ps
tsk(o)	Output Skew; NOTE 3	Measured on rising edge at VDDO/2			200	ps
tsk(ω)	Multiple Frequency Skew; NOTE 4	Measured on rising edge at VDDO/2			250	ps
tsk(pp)	Part to Part Skew; NOTE 5	Measured on rising edge at VDDO/2			650	ps
tR	Output Rise Time; NOTE 6	30% to 70%	280		850	ps
tF	Output Fall Time; NOTE 6	30% to 70%	280		850	ps
tPW	Output Pulse Width	0MHZ < f < 200MHz	tCYCLE/2 - 0.5	tCYCLE/2	tCYCLE/2 + 0.5	ns
		f = 200MHz	2	2.5	3	ns
tEN	Output Enable Time; NOTE 6	f = 10MHz			6	ns
tDIS	Output Disable Time; NOTE 6	f = 10MHz			6	ns

NOTE 1: All parameters measured at fIN = 200MHz and VPP = 300mV unless noted otherwise. All outputs terminated with 50Ω to VDDO/2.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.
NOTE 5: Defined as the skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

TABLE 4B. DC ELECTRICAL CHARACTERISTICS, VDDI=3.3V±5%, VDDO=2.5V±5%, T_A=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage			3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage			2.375	2.5	2.625	V
VIH	Input High Voltage	All except CLK, nCLK	VDDI = 3.465V	2		3.8	V
VIL	Input Low Voltage	All except CLK, nCLK	VDDI = 3.135V	-0.3		0.8	V
VPP	Peak-to-Peak Input Voltage	CLK, nCLK		0.15		1.3	
VCMR	Common Mode Input Voltage; NOTE 1	CLK, nCLK	LVPECL Levels	1.8		2.4	
			DCM, HSTL, LVDS, SSTL Levels	0.31		1.3	
IIH	Input High Current	All except CLK	VDDI = VIN = 3.465V			5	µA
		CLK	VDDI = VIN = 3.465V			150	µA
IIL	Input Low Current	All except CLK	VDDI = 3.465V, VIN = 0V	-150			µA
		CLK	VDDI = 3.465V, VIN = 0V	-5			µA
IDD	Quiescent Power Supply Current		VDDI = VIH = 3.465V VIL = 0V			70	mA
VOH	Output High Voltage		VDDI = 3.135V, VDDO = 2.375V IOH = -27mA	1.9			V
VOL	Output Low Voltage		VDDI = 3.135V, VDDO = 2.375V IOL = 27mA			0.5	V

NOTE 1: Common mode input voltage for LVPECL is defined as the minimum VIH. The LVPECL values noted in Table 4B are for VCCI = 3.3V. VCMR for LVPECL will vary 1:1 with VCCI. Common mode input voltage for DCM, HSTL, LVDS and SSTL is defined as the crossover voltage. See Figure 1.

TABLE 5B. AC ELECTRICAL CHARACTERISTICS, VDDI=3.3V±5%, VDDO=2.5V±5%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				250	MHz
tpLH	Propagation Delay, Low-to-High	0MHZ < f ≤ 200MHz	2.3		3.6	ns
tpHL	Propagation Delay, High-to-Low	0MHZ < f ≤ 200MHz	2.3		3.6	ns
tsk(b)	Bank Skew; NOTE 2	Measured on rising edge at VDDO/2			150	ps
tsk(o)	Output Skew; NOTE 3	Measured on rising edge at VDDO/2			200	ps
tsk(ω)	Multiple Frequency Skew; NOTE 4	Measured on rising edge at VDDO/2			250	ps
tsk(pp)	Part to Part Skew; NOTE 5	Measured on rising edge at VDDO/2			700	ps
tR	Output Rise Time; NOTE 6	30% to 70%	280		850	ps
tF	Output Fall Time; NOTE 6	30% to 70%	280		850	ps
tPW	Output Pulse Width	0MHZ < f < 200MHz	tCYCLE/2 - 0.5	tCYCLE/2	tCYCLE/2 + 0.5	ns
		f = 200MHz	2	2.5	3	ns
tEN	Output Enable Time; NOTE 6	f = 10MHz			6	ns
tDIS	Output Disable Time; NOTE 6	f = 10MHz			6	ns

NOTE 1: All parameters measured at fIN = 200MHz and VPP = 300mV unless noted otherwise. All outputs terminated with 50Ω to VDDO/2.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.
NOTE 5: Defined as the skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

FIGURE 1A, 1B - TIMING DIAGRAMS

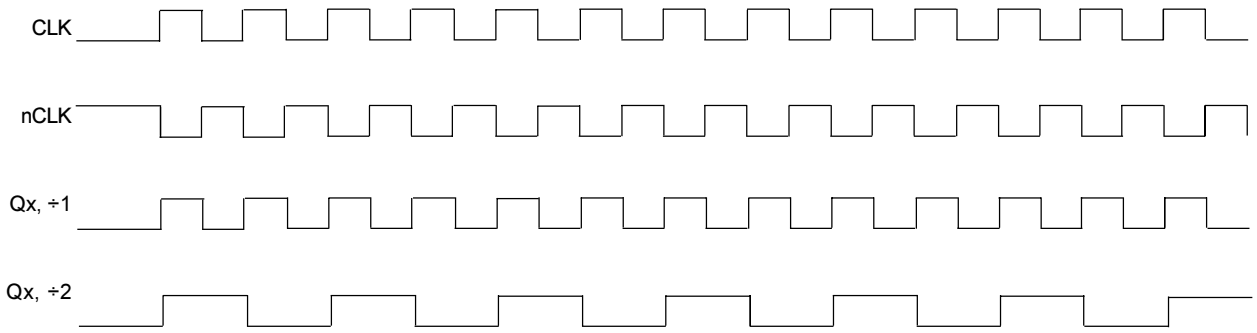


FIGURE 1A - ACTIVE, ÷1, ÷2

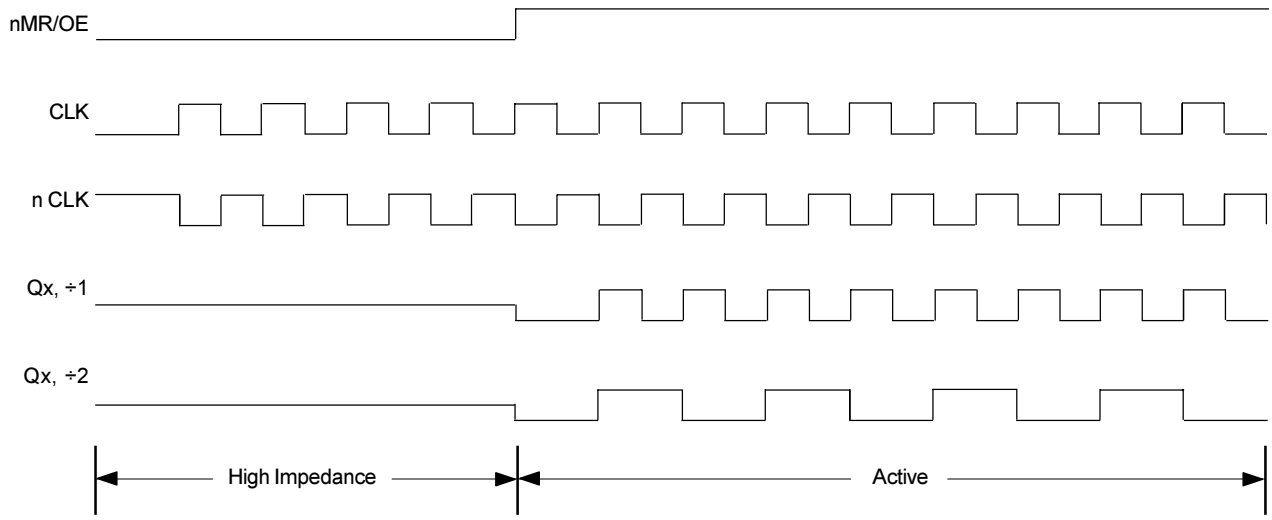


FIGURE 1B - RESET TO ACTIVE, ÷1, ÷2

FIGURE 2A, 2B, 2C - INPUT CLOCK WAVEFORMS

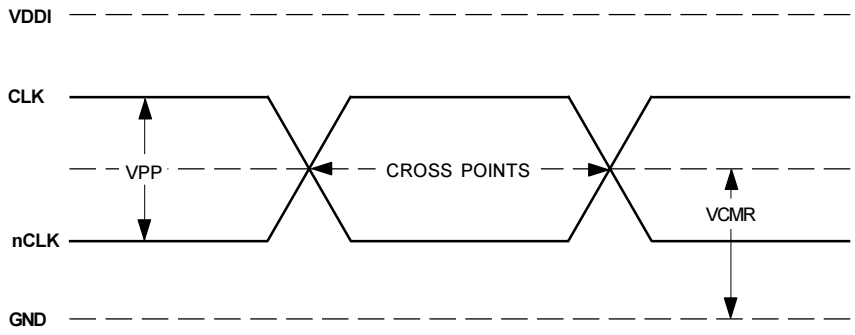


FIGURE 2A - DCM, HSTL, LVDS, SSTL DIFFERENTIAL INPUT LEVELS

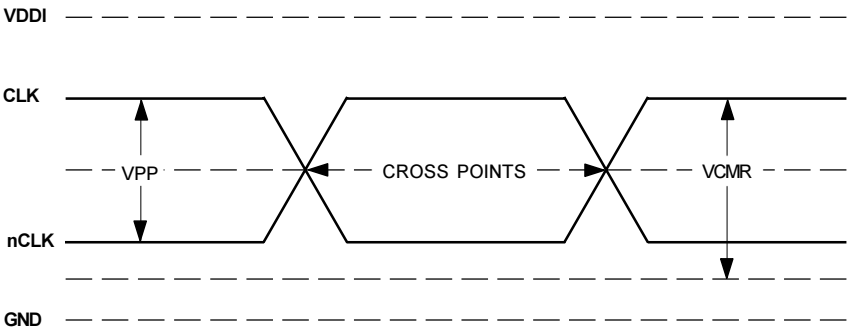


FIGURE 2B - LVPECL DIFFERENTIAL INPUT LEVEL

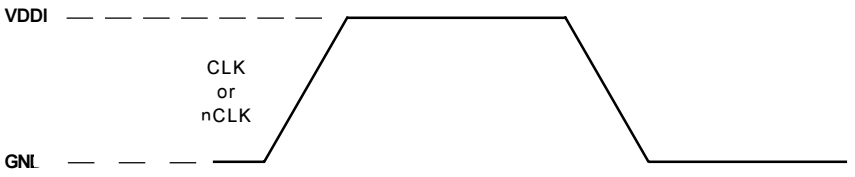


FIGURE 2C- LVCMOS AND LVTTL SINGLE ENDED INPUT LEVEL

FIGURE 3A, 3B - TIMING WAVEFORMS

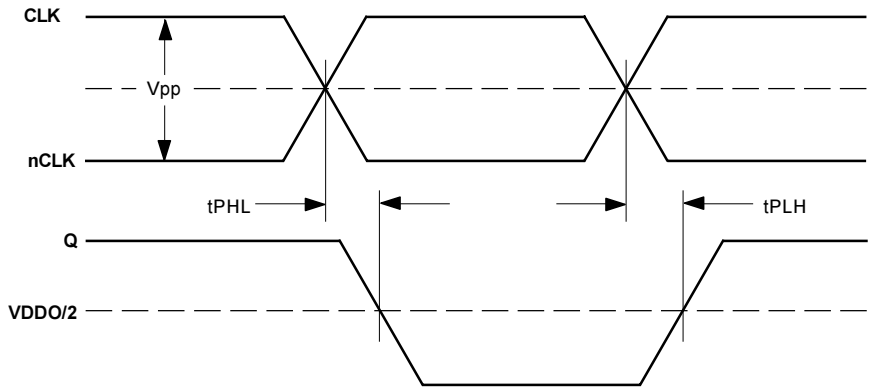


FIGURE 3A - PROPAGATION DELAYS

fin = 200MHz, Vpp = 300mV, tr = tf = 200ps

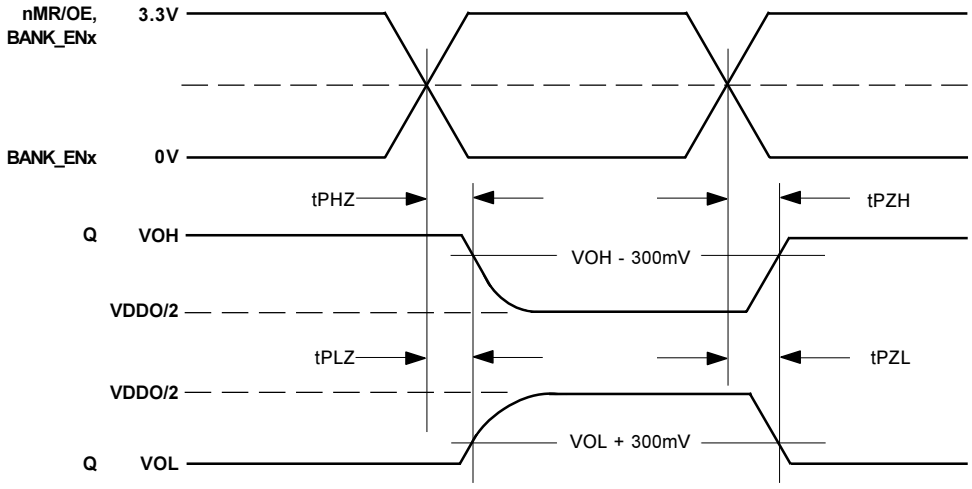


FIGURE 3B - DISABLE AND ENABLE TIMES

fin = 10MHz, Vamp = 3.3V, tr = tf = 600ps

FIGURE 4A, 4B- SKEW DEFINITIONS & WAVEFORMS

Bank Skew - Skew between outputs within a bank. Outputs operating at the same temperature, supply voltages and with equal load conditions.

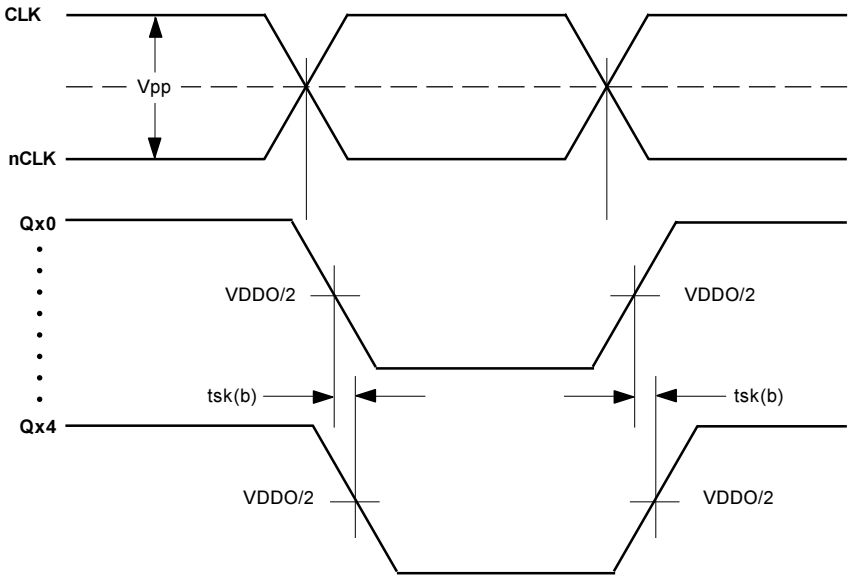


FIGURE 4A - BANK SKEW

fin = 200MHz, Vpp = 300mV, tr = tf = 200ps

Output Skew - Skew between outputs of any bank. Outputs operating at the same temperature, supply voltages and with equal load conditions.

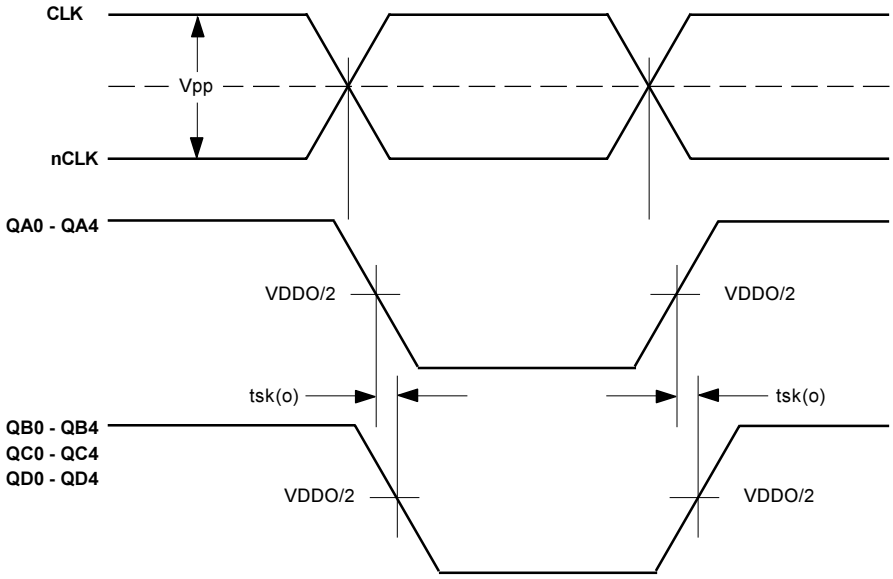


FIGURE 4B - OUTPUT SKEW

fin = 200MHz, Vpp = 300mV, tr = tf = 200ps

FIGURE 4C, 4D- SKEW DEFINITIONS & WAVEFORMS

Multiple Frequency Skew - Skew between banks of outputs operating at different frequencies. Outputs operating at the same temperature, supply voltages and with equal load conditions.

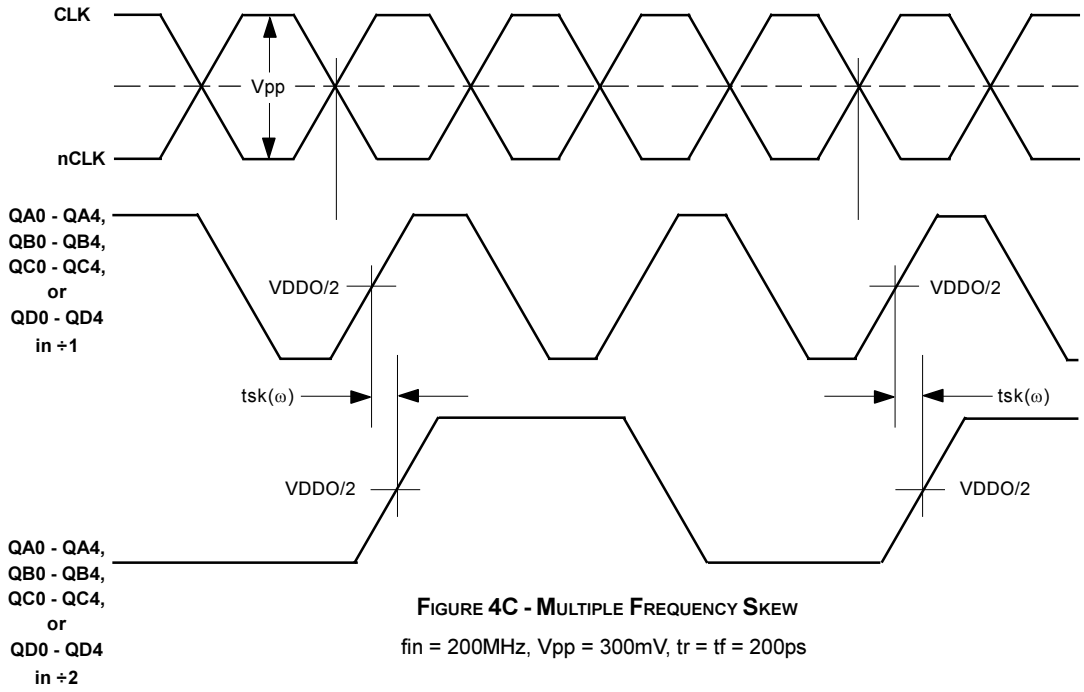


FIGURE 4C - MULTIPLE FREQUENCY SKEW

fin = 200MHz, Vpp = 300mV, tr = tf = 200ps

Part to Part Skew - Skew between outputs of any bank on different parts. Outputs operating at the same temperature, supply voltages and with equal load conditions.

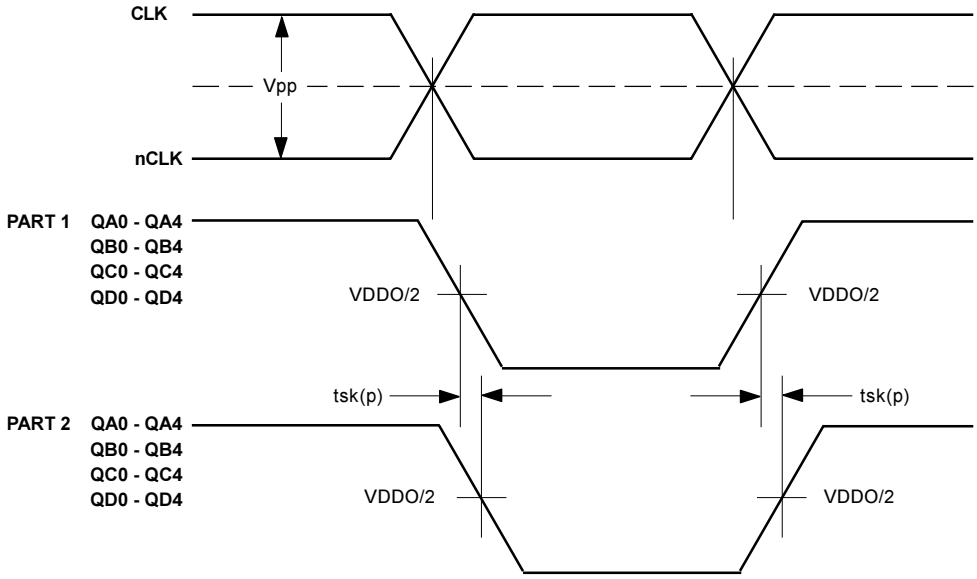
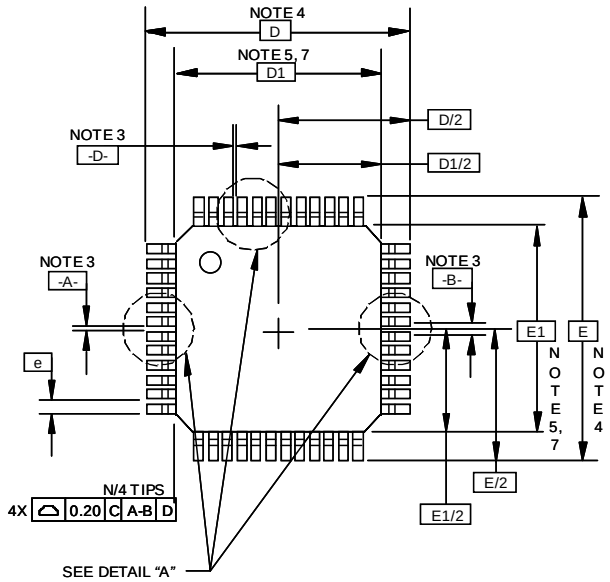
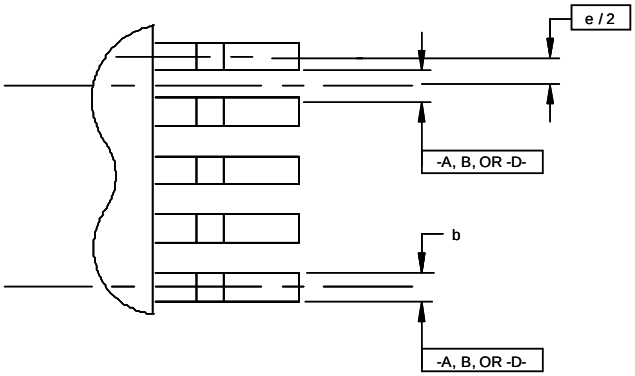


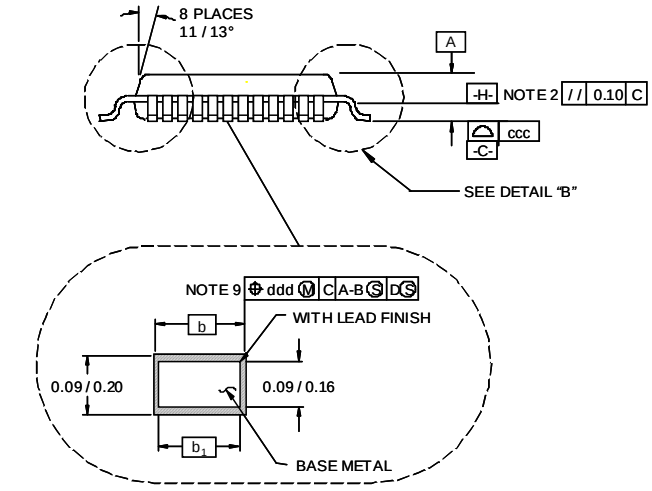
FIGURE 4B - OUTPUT SKEW

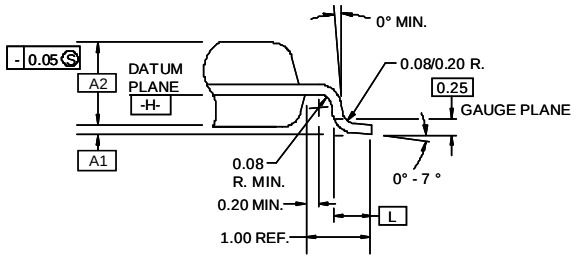
fin = 200MHz, Vpp = 300mV, tr = tf = 200ps

PACKAGE OUTLINE AND DIMENSIONS - Y SUFFIX









NOTES:

1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLACE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETEREMINED AT DATUM PLANE -H-.
8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
10. CONTROLLING DIMENSION: MILLIMETER.
11. THIS OUTLINE CONFORMS TO JEDEC PUBLIBCATION 95 REGISTRATION MS-026, VARIATION BBC.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			NOTE
	BBC			
	MIN.	NOM.	MAX.	
A			1.60	
A_1	0.05		0.15	12
A_2	1.35	1.40	1.45	
D	9.00 BSC.			4
D_1	7.00 BSC.			7, 8
E	9.00 BSC.			4
E_1	7.00 BSC.			7, 8
L	0.45	0.60	0.75	
N		48		
e	0.5 BSC.			
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8702BY	ICS8702BY	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8702BYT	ICS8702BY	48 Lead LQFP on Tape and Reel	2000	0°C to 70°C