



GENERAL DESCRIPTION

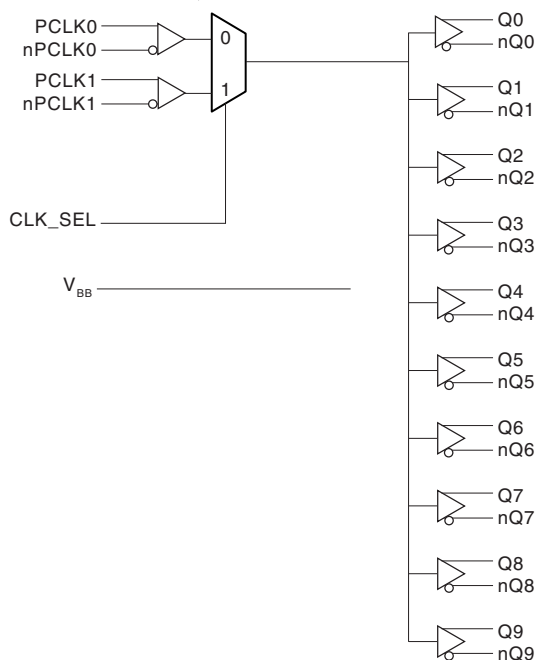


The ICS853111-02 is a low skew, high performance 1-to-10 Differential-to-2.5V/3.3V LVPECL/ECL Fanout Buffer and a member of the HiPerClockSTM family of High Performance Clock Solutions from ICS. The ICS853111-02 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS853111-02 ideal for those clock distribution applications demanding well defined performance and repeatability.

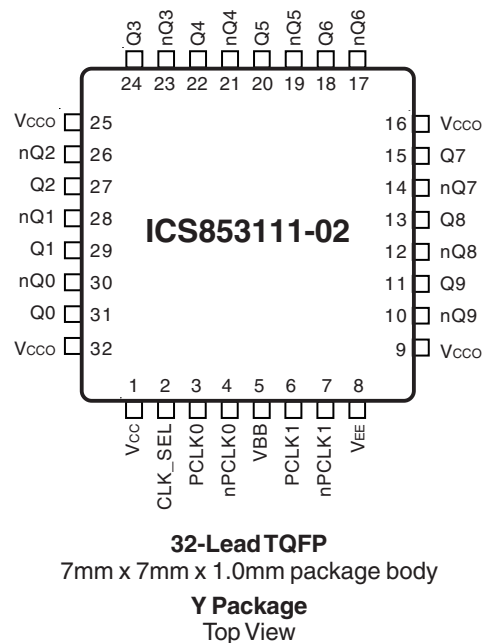
FEATURES

- Ten differential 2.5V/3.3V LVPECL / ECL outputs
- Two selectable differential input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 3.2GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- Output skew: 25ps (typical)
- Part-to-part skew: 85ps (typical)
- Propagation delay: 680ps (typical)
- Jitter, RMS: < 0.03ps (typical)
- LVPECL mode operating voltage supply range: $V_{CC} = 2.375V$ to $3.8V$, $V_{EE} = 0V$
- ECL mode operating voltage supply range: $V_{CC} = 0V$, $V_{EE} = -3.8V$ to $-2.375V$
- $-40^{\circ}C$ to $85^{\circ}C$ ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V _{CC}	Power		Core supply pin.
2	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK1, nPCLK1 inputs. When LOW, selects PCLK0, nPCLK0 inputs. LVCMOS / LVTTTL interface levels.
3	PCLK0	Input	Pulldown	Non-inverting differential clock input.
4	nPCLK0	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. V _{CC} /2 default when left floating.
5	V _{BB}	Output		Bias voltage.
6	PCLK1	Input	Pulldown	Non-inverting differential clock input.
7	nPCLK1	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. V _{CC} /2 default when left floating.
8	V _{EE}	Power		Negative supply pin.
9, 16, 25, 32	V _{CCO}	Power		Output supply pins.
10, 11	nQ9, Q9	Output		Differential output pair. LVPECL interface levels.
12, 13	nQ8, Q8	Output		Differential output pair. LVPECL interface levels.
14, 15	nQ7, Q7	Output		Differential output pair. LVPECL interface levels.
17, 18	nQ6, Q6	Output		Differential output pair. LVPECL interface levels.
19, 20	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
26, 27	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
28, 29	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
30, 31	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R _{PULLDOWN}	Input Pulldown Resistor			75		kΩ
R _{VCC/2}	Pullup/Pulldown Resistors			50		kΩ

TABLE 3A. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
PCLKx	nPCLKx	Q0:Q9	nQ0:Q9		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information, "Wiring the Differential Input to Accept Single Ended Levels".

TABLE 3B. CONTROL INPUT FUNCTION TABLE

Inputs	
CLK_SEL	Selected Source
0	PCLK0, nPCLK0
1	PCLK1, nPCLK1



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, $V_{EE} = 0$)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, $V_{CC} = 0$)
Inputs, V_I (LVPECL mode)	-0.5V to $V_{CC} + 0.5V$
Inputs, V_I (ECL mode)	0.5V to $V_{EE} - 0.5V$
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
V_{BB} Sink/Source, I_{BB}	$\pm 0.5mA$
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	49.5°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = 2.375$ TO $3.8V$; $V_{EE} = 0V$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.8	V
I_{EE}	Power Supply Current				85	mA

TABLE 4B. LVPECL DC CHARACTERISTICS, $V_{CC} = 3.3V$; $V_{EE} = 0V$

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1	2.175	2.275	2.38	2.225	2.295	2.37	2.295	2.33	2.365	V
V_{OL}	Output Low Voltage; NOTE 1	1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{IH}	Input High Voltage(Single-Ended)	2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage(Single-Ended)	1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference; NOTE 2	1.86		1.98	1.86		1.98	1.86		1.98	V
V_{PP}	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1		150			150			150	μA
I_{IL}	Input Low Current	PCLK0, PCLK1 nPCLK0, nPCLK1		-150			-150			-150	μA

Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

NOTE 2: Single-ended input operation is limited $V_{CC} \geq 3V$ in LVPECL mode.

NOTE 3: Common mode voltage is defined as V_{IH} .

NOTE 4: For single-ended applications, the maximum input voltage for PCLK0, nPCLK0 and PCLK1, nPCLK1 is $V_{CC} + 0.3V$.



TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{CC} = 2.5V$; $V_{EE} = 0V$

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1	1.375	1.475	1.58	1.425	1.495	1.57	1.495	1.53	1.565	V
V_{OL}	Output Low Voltage; NOTE 1	0.605	0.745	0.88	0.625	0.72	0.815	0.64	0.735	0.83	V
V_{IH}	Input High Voltage(Single-Ended)	1.275		1.56	1.275		1.56	1.275		-0.8	V
V_{IL}	Input Low Voltage(Single-Ended)	0.63		0.965	0.63		0.965	0.63		0.965	V
V_{PP}	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1		150			150			150	μA
I_{IL}	Input Low Current	PCLK0, PCLK1 nPCLK0, nPCLK1		-150			-150			-150	μA

Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.125V to -1.3V.

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

NOTE 2: Common mode voltage is defined as V_{IH} .

NOTE 3: For single-ended applications, the maximum input voltage for PCLK0, nPCLK0 and PCLK1, nPCLK1 is $V_{CC} + 0.3V$.

TABLE 4D. ECL DC CHARACTERISTICS, $V_{CC} = 0V$; $V_{EE} = -3.8V$ TO $-2.375V$

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1	-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.005	-0.97	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1	-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{IH}	Input High Voltage(Single-Ended)	-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage(Single-Ended)	-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference; NOTE 2	-1.486		-1.386	-1.486		-1.386	-1.486		-1.386	V
V_{PP}	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4	$V_{EE}+1.2V$		0	$V_{EE}+1.2V$		0	$V_{EE}+1.2V$		0	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1		150			150			150	μA
I_{IL}	Input Low Current	PCLK0, PCLK1 nPCLK0, nPCLK1		-150			-150			-150	μA

Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

NOTE 2: Single-ended input operation is limited $V_{CC} \geq 3V$ in LVPECL mode.

NOTE 3: Common mode voltage is defined as V_{IH} .

NOTE 4: For single-ended applications, the maximum input voltage for PCLK0, nPCLK0 and PCLK1, nPCLK1 is $V_{CC} + 0.3V$.



TABLE 5. AC CHARACTERISTICS, $V_{CC} = 0V$; $V_{EE} = -3.8V$ TO $-2.375V$ OR $V_{CC} = 2.375$ TO $3.8V$; $V_{EE} = 0V$

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency			3.2			3.2			3.2	GHz
t_{PD}	Propagation Delay; NOTE 1	600	680	750	650	725	790	690	790	890	ps
$tsk(o)$	Output Skew; NOTE 2, 4		25	37		25	37		25	37	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 4		85	225		85	225		85	225	ps
f_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section		0.03			0.03			0.03		ps
t_R/t_F	Output Rise/Fall Time 20% to 80%	60	200	325	100	200	280	130	200	270	ps

All parameters are measured ≤ 1 GHz unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

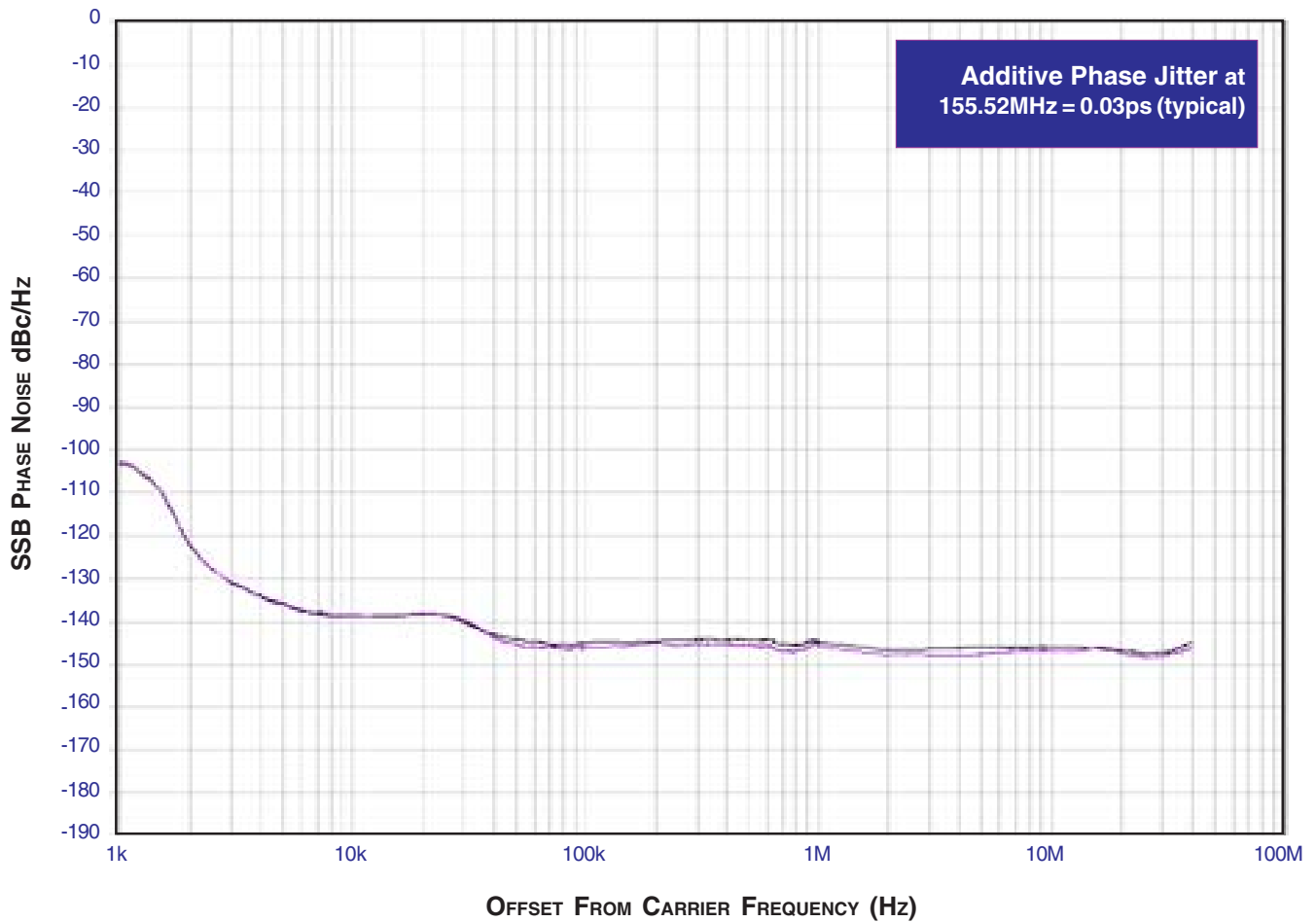
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in

the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

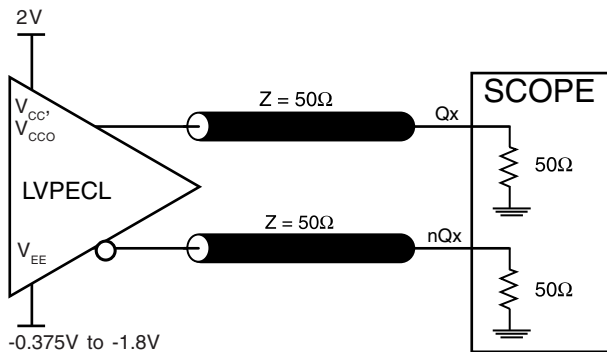


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The de-

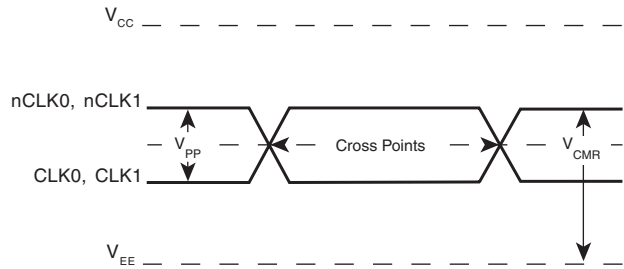
vice meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.



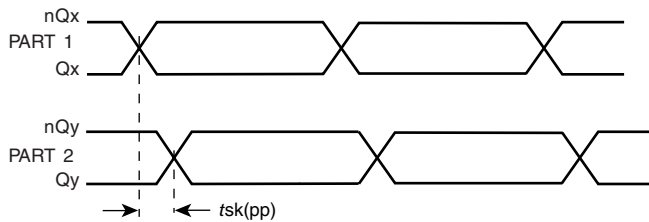
PARAMETER MEASUREMENT INFORMATION



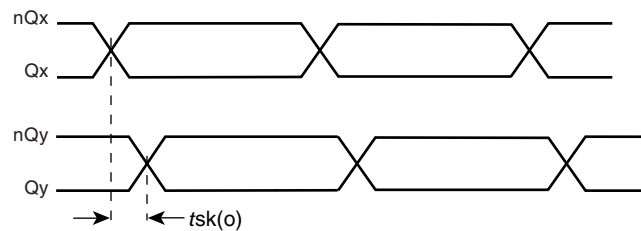
3.3V OUTPUT LOAD AC TEST CIRCUIT



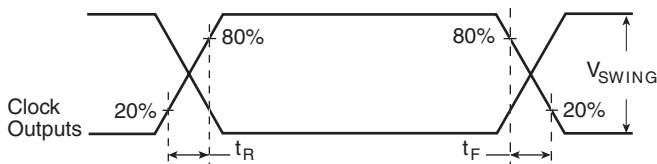
DIFFERENTIAL INPUT LEVEL



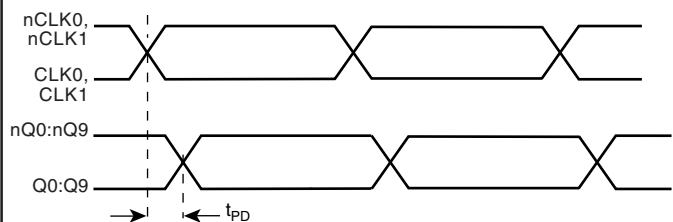
PART-TO-PART SKEW



OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY

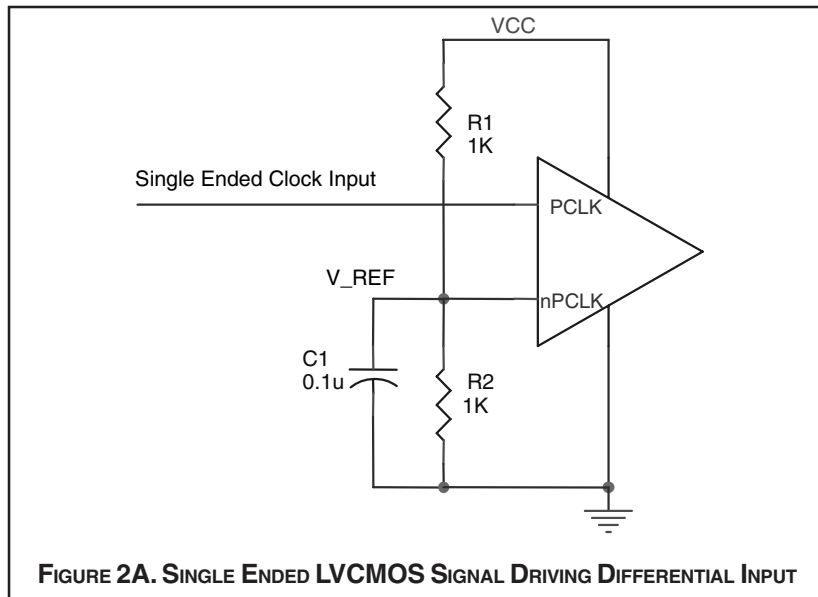


APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVCMOS LEVELS

Figure 2A shows an example of the differential input that can be wired to accept single ended LVCMOS levels. The reference voltage level V_{BB} generated from the device is

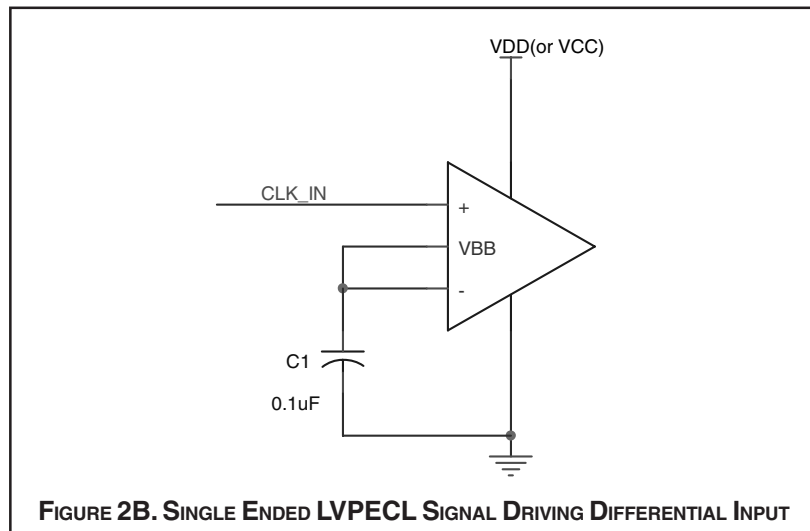
connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.



WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVPECL LEVELS

Figure 2B shows an example of the differential input that can be wired to accept single ended LVPECL levels. The reference voltage level V_{BB} generated from the device is

connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.





LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces sug-

gested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

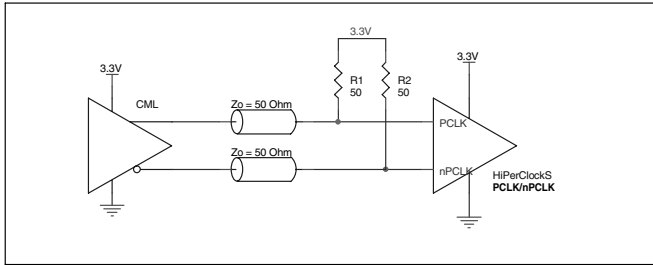


FIGURE 3A. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A CML DRIVER

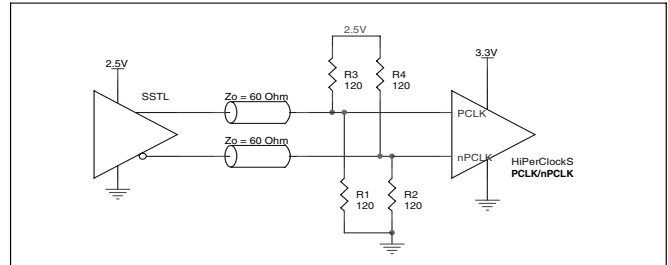


FIGURE 3B. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER

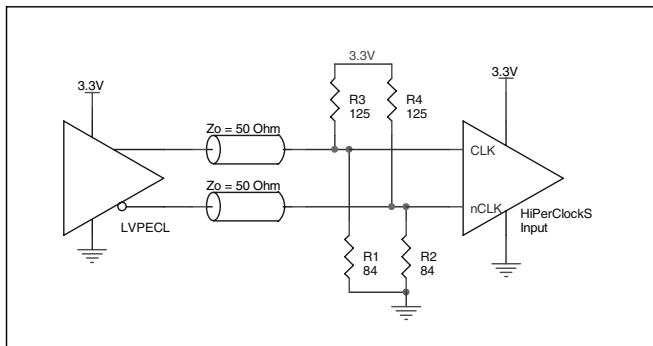


FIGURE 3C. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

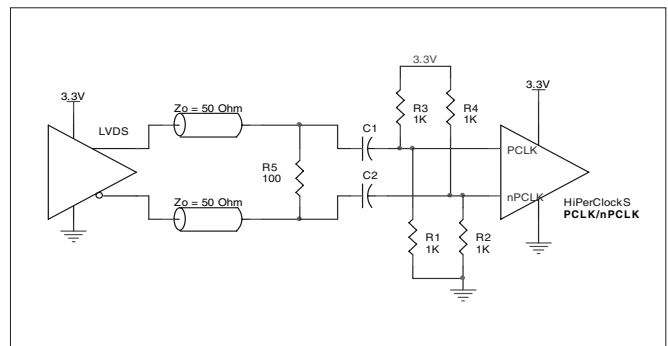


FIGURE 3D. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

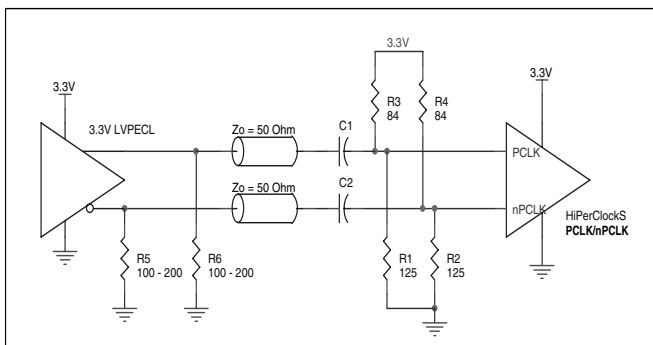


FIGURE 3E. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE



RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

PCLK/nPCLK INPUT:

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched imped-

ance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

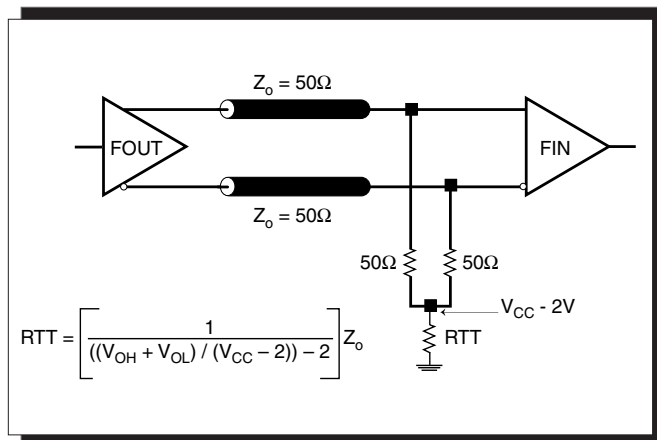


FIGURE 4A. LVPECL OUTPUT TERMINATION

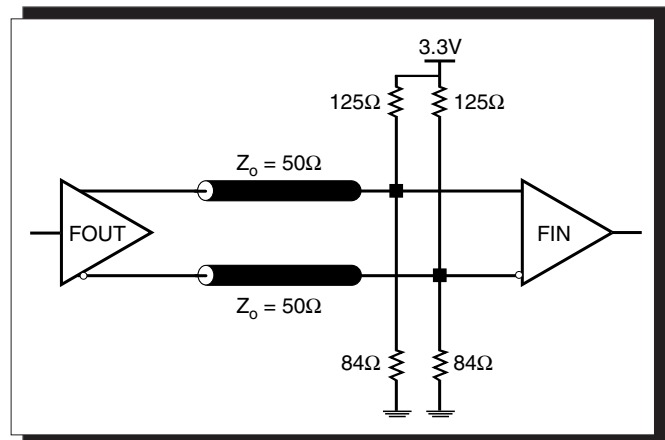


FIGURE 4B. LVPECL OUTPUT TERMINATION



TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very

close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

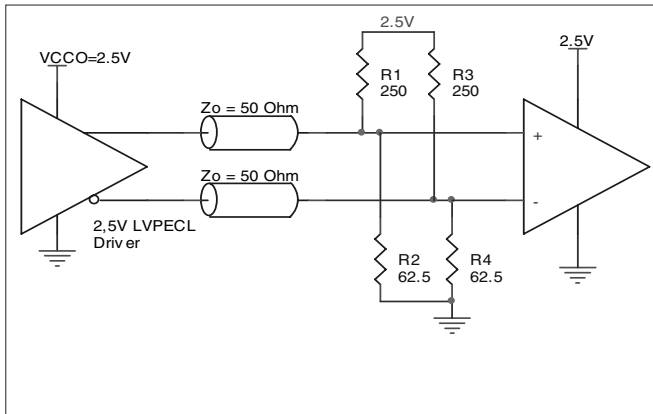


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

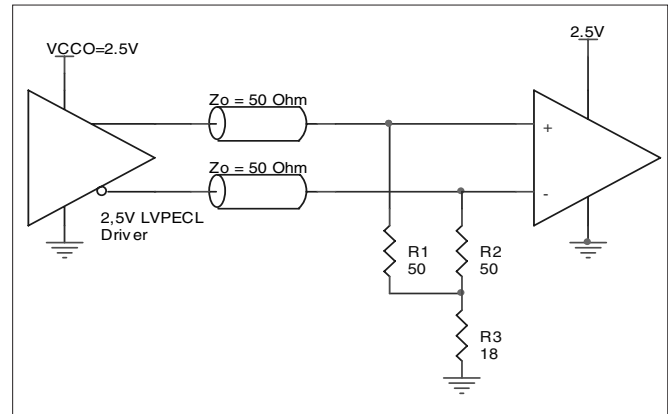


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

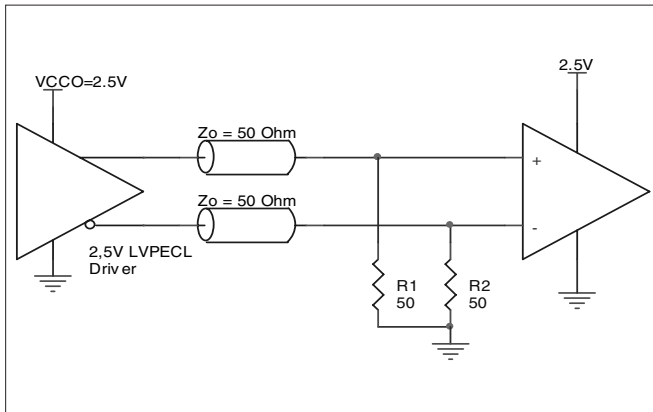


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE



SCHEMATIC EXAMPLE

This application note provides general design guide using ICS853111-02 LVPECL buffer. *Figure 6* shows a schematic example of the ICS853111-02 LVPECL clock buffer. In this ex-

ample, the input is driven by an LVPECL driver. CLK_SEL is set at logic high to select PCLK0/nPCLK0 input.

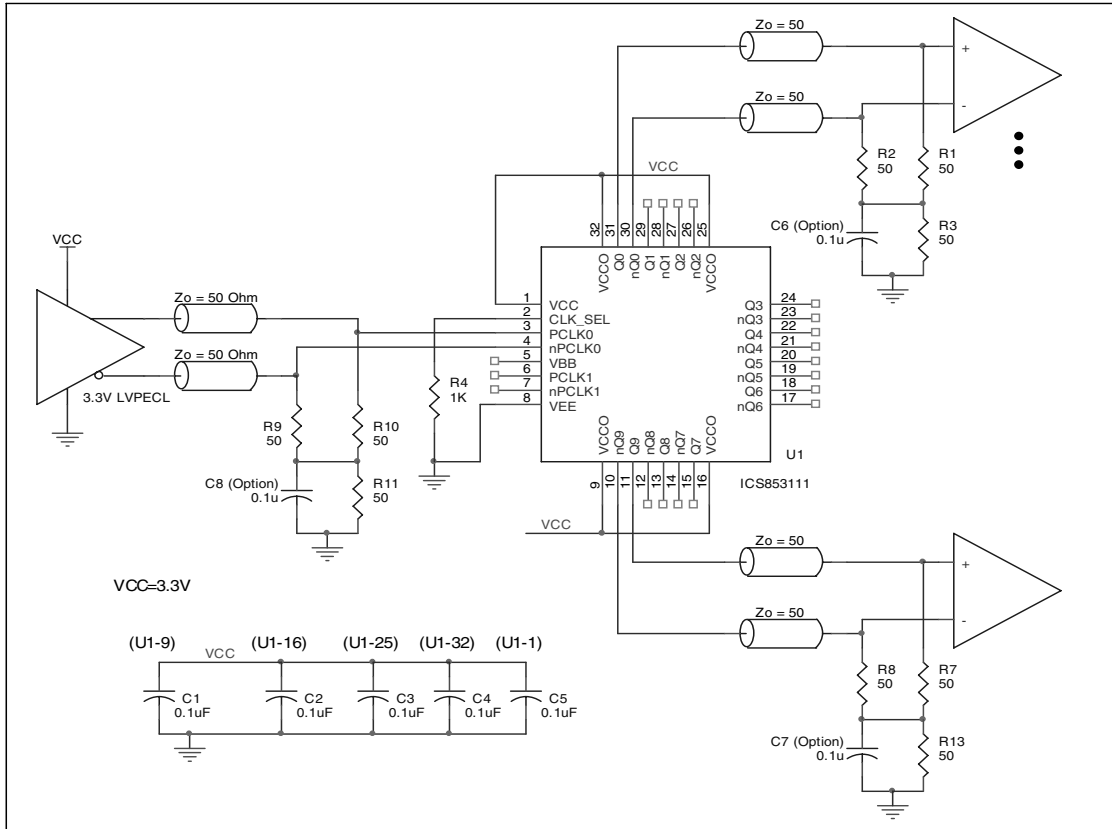


FIGURE 6. EXAMPLE ICS853111-02 LVPECL CLOCK OUTPUT BUFFER SCHEMATIC

THERMAL RELEASE PATH

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through

solder as shown in *Figure 7*. For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

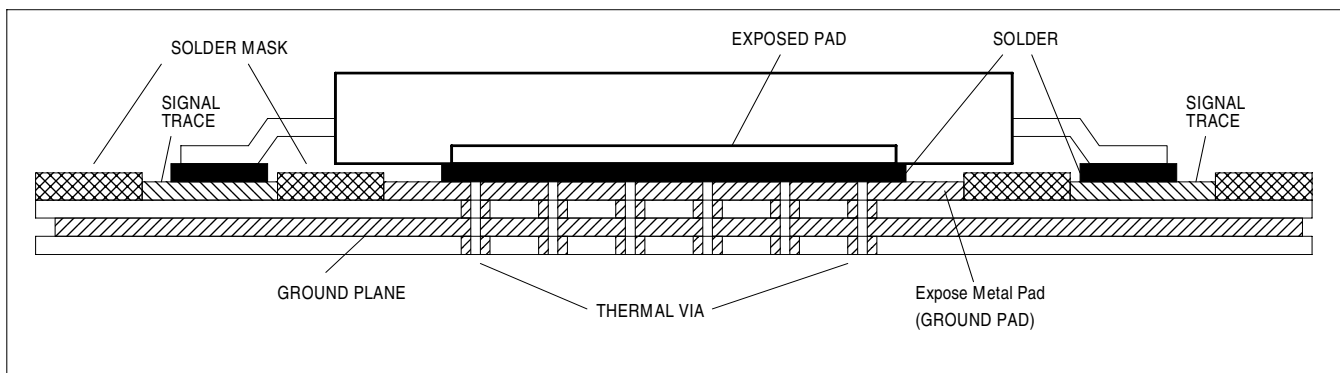


FIGURE 7. P.C. BOARD FOR EXPOSED PAD THERMAL RELEASE PATH EXAMPLE



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853111-02. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS853111-02 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.8V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.8V * 85mA = 323mW$
- Power (outputs)_{MAX} = **30.94mW/Loaded Output pair**
If all outputs are loaded, the total power is $10 * 30.94mW = 309.4mW$

Total Power_{MAX} (3.8V, with all outputs switching) = $323mW + 309.4mW = 632.4mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 43.8°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85°C + 0.632W * 43.8°C/W = 112.7°C$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 32-PIN TQFP, E-PAD, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	69.3°C/W	57.8°C/W	52.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.8°C/W	41.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 8.

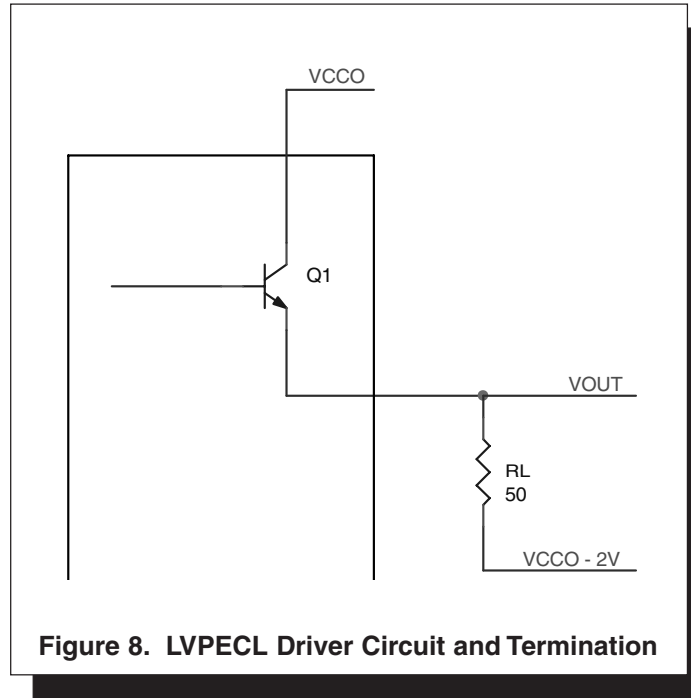


Figure 8. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.935V$

$$(V_{CC_MAX} - V_{OH_MAX}) = 0.935V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.67V$

$$(V_{CCO_MAX} - V_{OL_MAX}) = 1.67V$$

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.67V)/50\Omega] * 1.67V = 11.02mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30.94mW$$



RELIABILITY INFORMATION

TABLE 7. θ_{JA} vs. AIR FLOW TABLE FOR 32 LEAD TQFP, E-PAD

	θ_{JA} by Velocity (Linear Feet per Minute)		
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	69.3°C/W	57.8°C/W	52.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.8°C/W	41.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS853111-02 is: 1340

Pin compatible with MC100EP111 and MC100LVEP111



TQFP PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD TQFP, E-PAD

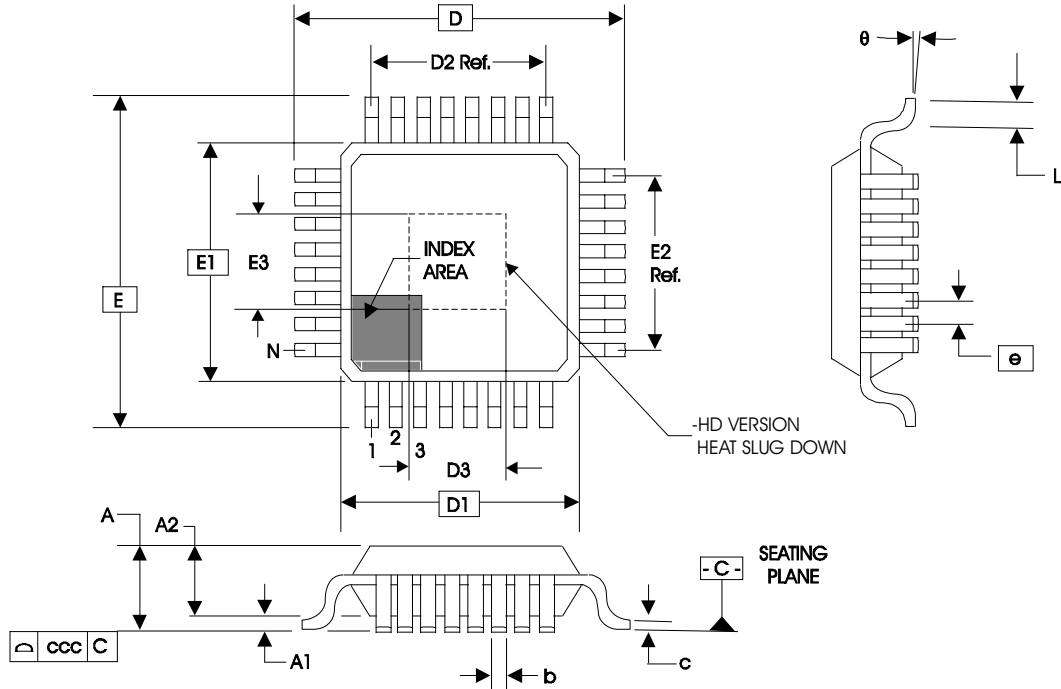


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	ABA-HD		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.20
A1	0.05	0.10	0.15
A2	0.95	1.0	1.05
b	0.30	0.35	0.40
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
D3	4.00 BASIC		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
E3	4.00 BASIC		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026



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ICS853111-02

LOW SKEW, 1-TO-10 DIFFERENTIAL-TO-2.5V/3.3V LVPECL/ECL FANOUT BUFFER

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS853111AY-02	ICS853111A02	32 lead, E-Pad TQFP	tray	-40°C to 85°C
ICS853111AY-02T	ICS853111A02	32 lead, E-Pad TQFP	1000 tape & reel	-40°C to 85°C
ICS853111AY-02LF	ICS853111A02L	32 lead "Lead-Free," E-Pad TQFP	tray	-40°C to 85°C
ICS853111AY-02LFT	ICS853111A02L	32 lead "Lead-Free," E-Pad TQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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LOW SKEW, 1-TO-10

DIFFERENTIAL-TO-2.5V/3.3V LVPECL/ECL FANOUT BUFFER

REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
A	T9	10 17	Added <i>Recommendations for Unused Input and Output Pins.</i> Ordering Information Table - added Lead-Free marking.	1/10/06