# CMOS Image Sensor
# with Image Signal Processing

# HV7131GP

V2.4

# Revision History

| Revision | Script Date | Comments |
|---|---|---|
| V1.0 | 2001/11/08/Thu – 2001/11/14/Thu | - HV7131GP Preliminary is released |
| V1.1 | 2001/12/21/Fri | - Gamma slope table of Knee/De-Knee is added, and some misprints are corrected |
| V1.2 | 2002/03/25/Mon | - Knee/De-Knee function is abandoned, instead 10bit ADC is implemented.<br>- Register descriptions are revised<br>- Frame timing is revised. |
| V1.3 | 2002/04/25/Thu | - register information is updated |
| V1.4 | 2002/05/06/Mon | - Data output timing & interface is added |
| V1.5 | 2002/05/13/Tue | - Chip layout information is revised, and miscellaneous typo errors are corrected |
| V1.6 | 2002/05/28/Tue | - chip layout information is omitted for confidentiality, and power consumption information is added. |
| V1.7 | 2002/06/14/Fri | - CLCC 40 Pin Diagram added |
| V1.8 | 2002/12/26/Thu. | - PKG Drawing Added |
| V1.9 | 2003/01/17/Fri. | - Register Description Revision |
| V2.0 | 2003/06/04/Wed. | - 40 pin diagram revision |
| V2.1 | 2003/07/10/Thu.. | - ENB Setting guide information is added |
| V2.2 | 2003/12/11/Thu.. | - C[7:0] PAD information is added. |
| V2.3 | 2004/06/26/Sat | -I2C Data Hold Time Revision<br>- External pull-up/ pull-down resistance is added |
| V2.4 | 2004/10/29/Fri | - Value of SNR, Dynamic Range, Sensitivity is added at Features. |



# Disclaimer

This document is a general product description and is subject to change without notice. MagnaChip Semiconductor Ltd., assumes no responsibility or liability arising from use of circuit described, and no patent licenses are implied.

# CONTENTS

## General Description

HV7131GP is a highly integrated single chip CMOS color image sensor implemented by proprietary MagnaChip 0.35um CMOS sensor process realizing high sensitivity and wide dynamic range. Total pixel array size is 652x492, and 652x488 pixels are active. Each active pixel composed of 4 transistors has a micro-lens to enhance sensitivity, and converts photon energy to analog pixel voltage. On-chip 10bit Analog to Digital Converter (ADC) digitizes analog pixel voltage, and on-chip Correlated Double Sampling (CDS) scheme reduces Fixed Pattern Noise (FPN) dramatically. General image processing functions such as gamma correction, color interpolation, color correction, color space conversion, auto exposure, and auto white balance are implemented to diversify its applications, and various output formats are supported for the sensor to easily interface with different video codec chips. The integration of sensor function and image processing functions make HV7131GP especially very suitable for mobile imaging systems such as IMT-2000 phone's video part that requires very low power and system compactness.

## Features

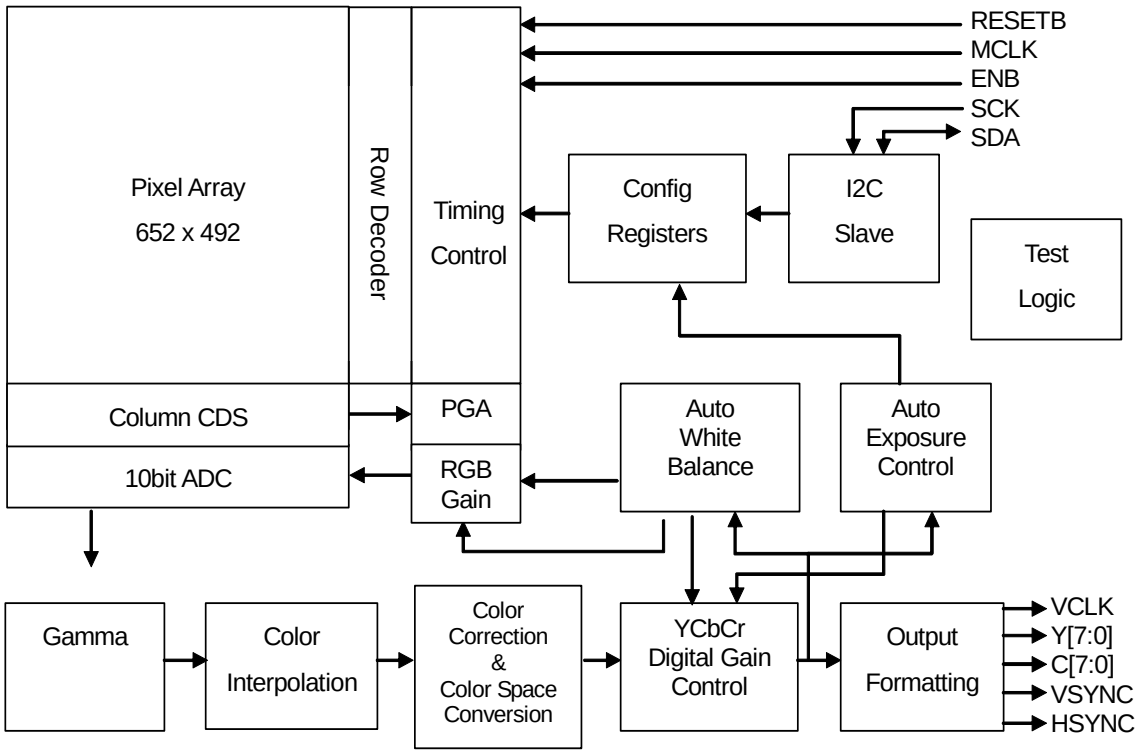
- 1/4 inch optical format
- Total pixel : 652 x 492 / Active pixel : 652x488
- 5.6um x 5.6um active square pixel
- Micro-lens for high sensitivity
- RGB mosaic color filter array
- On-chip 10 bit ADC
- Correlated double sampling for reduction of Fixed Pattern Noise
- Black Level Compensation
- Gamma correction by programmable piecewise linear approximation
- 3x3 Color interpolation
- Color correction by programmable 3x3 matrix operation
- Color space conversion from RGB to YCbCr
- Sub-sampling Modes : 1/4, 1/16
- Various output formats : YCbCr 4:2:2, YCbCr 4:4:4, RGB 4:4:4, Bayer
- 8bit / 16bit Data Bus Mode
- Automatic Exposure Control
- Automatic White Balance Control
- Frame Rate : 30 f/s at 25Mhz, HBLANK = 208, VBLANK = 8
- Power Consumption: 86mW @ 30f/s and 2.8V, 68mW @ 15f/s and 2.8V, 336uW @ power down
- Operation Voltage Range : 2.6V ~ 3.0V, Operation Temperature : -10 ~ +50 degrees Celsius

- Package Types : CLCC 40 PIN, COB(Chip-on-Board), COF(Chip-on-Flex)

  * To the matter concerning package, Wafer business companies are unrelated contents.

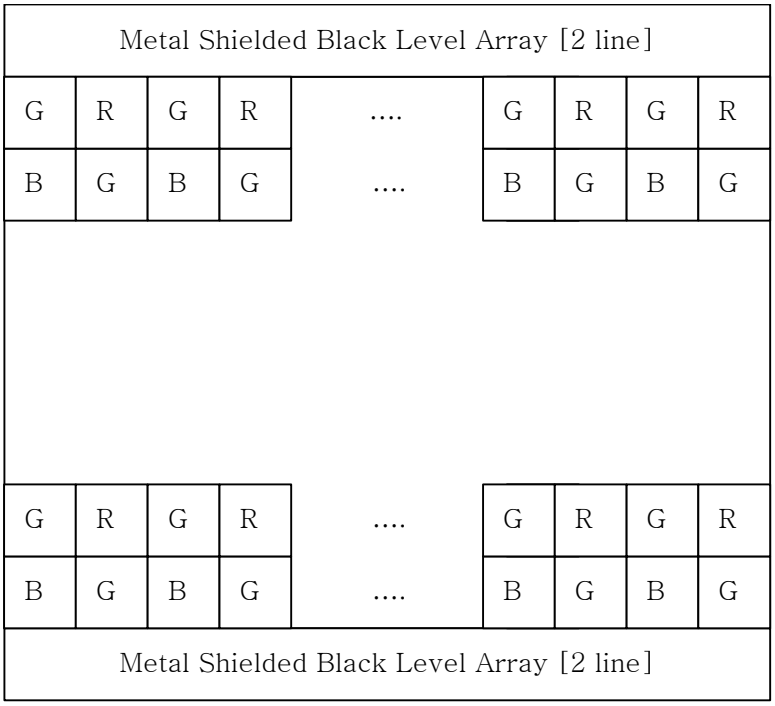
- Dynamic Range : 52 dB
- $SNR_{MAX}$ : 42 dB
- Sensitivity : 3000 mV / lux·sec (Green Pixel)

## Block Diagram



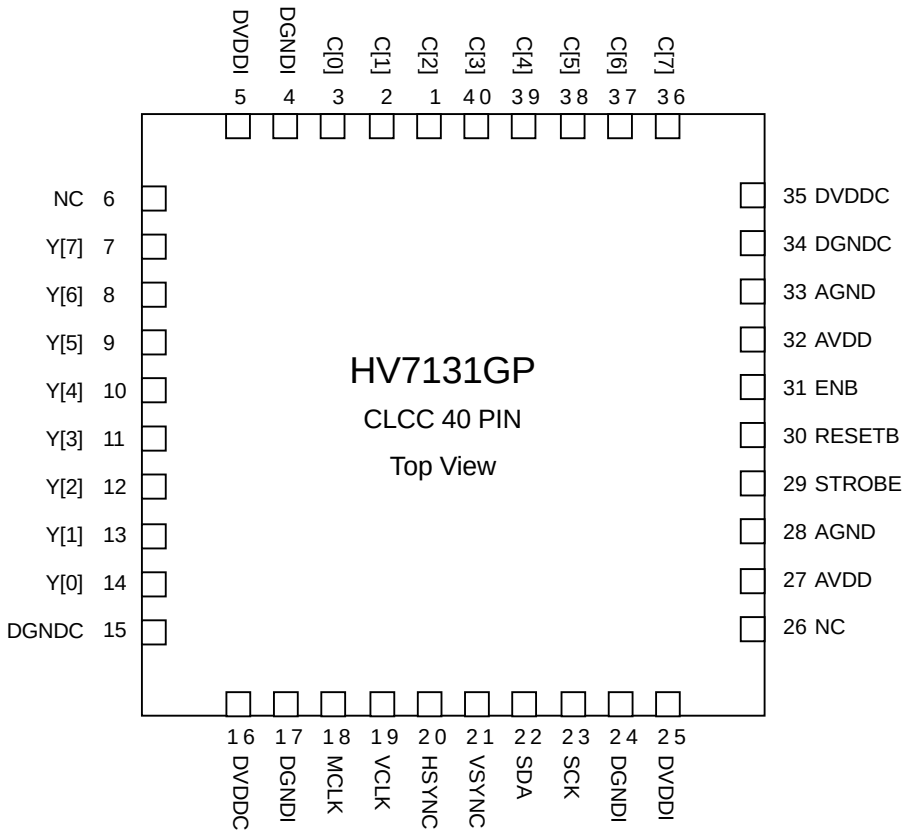

1. PGA : Programmable Gain Amplifier
2. Color Correction and Color Space Conversion are merged into one matrix operation for hardware simplification

**Pixel Array Structure**




Note: If black level data output is enabled(SCTRC[1] set to high) with Bayer mode set(SCTRA[1:0] == 2'b00), data output in the areas of Metal Shielded Black Level Array can be monitored during 4 line period of HSYNC right after VSYNC goes from high state to low state.

## Pin Diagram




* To the matter concerning package, Wafer business companies are unrelated contents.

## Pin Description

The input mode of HSYNC/VSYNC/Y[7:0]/C[7:0] is used to test internal image processing function in mass production so that it should be not assumed about slave mode operation. The device does not support slave mode operation. When 8bit output mode is used, we recommend that C[7:0] be set up as pull-up or pull-down according to I2C regulation. Although there is no pull-up or pull-down, it is no influence on function operation and leakage current does not become a problem after stabilization of chip. In case of application with C[7:0] without pull-up or pull-down, any problems were not generated.

| Pin | Type | Symbol | Description |
|---|---|---|---|
| 1-3 | B | C[2:0] | Video Chrominance Data[2:0] |
| 4 | G | DGNDI | Digital Ground for I/O Buffer |
| 5 | P | DVDDI | Digital Power for I/O Buffer |
| 6 | N | NC | No Connection |
| 7-14 | O | Y[7:0] | Video Luminance Data[7:0] |
| 15 | G | DGNDC | Ground for Internal Digital Block |
| 16 | P | DVDDC | Power for Internal Digital Block |
| 17 | G | DGNDI | Digital Ground for I/O Buffer |
| 18 | I | MCLK | Master Input Clock |
| 19 | O | VCLK | Video Output Clock |
| 20 | O | HSYNC | Video Horizontal Line Synchronization signal. Image data is valid, when HSYNC is high. |
| 21 | O | VSYNC | Video Frame Synchronization signal. VSYNC is active at start of image data frame. |
| 22 | B | SDA | I2C Standard data I/O port |
| 23 | I | SCK | I2C Clock Input |
| 24 | G | DGNDI | Digital Ground for I/O Buffer |
| 25 | P | DVDDI | Digital Power for I/O Buffer |
| 26 | N | NC | No Connection |
| 27 | P | AVDD | Power for Analog Block |
| 28 | G | AGND | Ground for Analog Block |
| 29 | O | STROBE | Strobe Signal Output |
| 30 | I | RESETB | Sensor Reset, Low Active |
| 31 | I | ENB | Sensor sleep mode is controlled externally by this pin when sleep mode register bit SCTRB[4] is low.<br>ENB low : sleep mode, ENB high : normal mode |
| 32 | P | AVDD | Power for Analog Block |
| 33 | G | AGND | Ground for Analog Block |
| 34 | G | DGNDC | Ground for Internal Digital Block |
| 35 | P | DVDDC | Power for Internal Digital Block |
| 36-40 | B | C[7:3] | Video Chrominance Data[7:3] |

* To the matter concerning package, Wafer business companies are unrelated contents.

Note) B: bi-direction pin, P: power pin, G: ground pin, O: output pin, I: Input pin

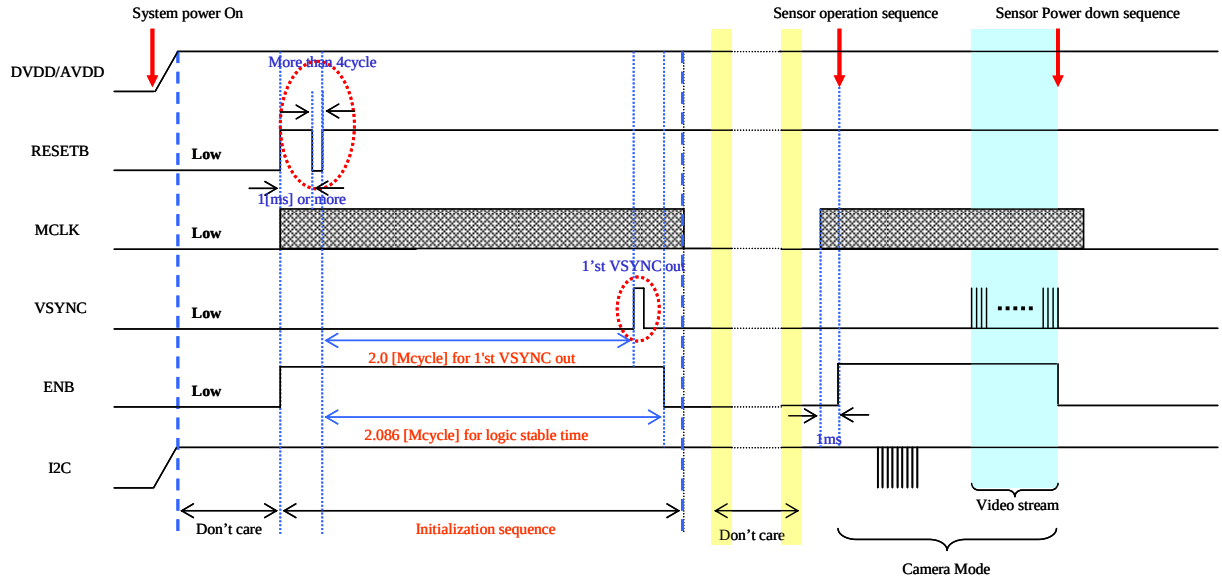
# Functional Description

## Pixel Architecture

Pixel architecture is a 4 transistor NMOS pixel design. The additional use of a dedicated transfer transistor in the architecture reduces most of reset level noise so that fixed pattern noise is not visible. Furthermore, micro-lens is placed upon each pixel in order to increase fill factor so that high pixel sensitivity is achieved.

## ENB Setting guide information for normal stand-by mode

It is necessary that this kind of initialization sequence for the normal stand-by mode of HV7131GP after system power on



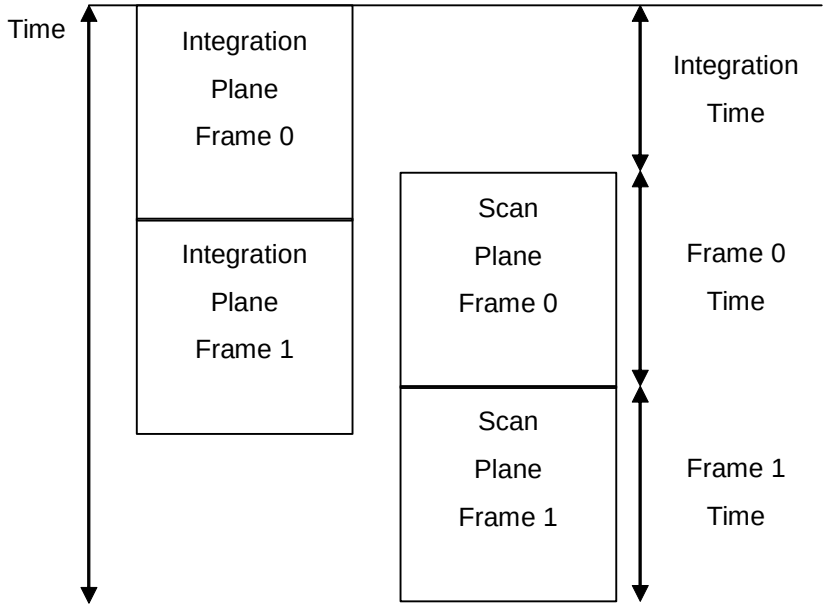

ex) If MCLK = 25[Mhz]

=> 2.086[Mcycle] / 25[MHz] = 83.44 ms

The time period of ENB high value have to keep for 83.44[ms] or more

## Sensor Imaging Operation

Imaging operation is implemented by the offset mechanism of integration domain and scan domain(rolling shutter scheme). First integration plane is initiated, and after the programmed integration time is elapsed, scan plane is initiated, then image data start being produced.



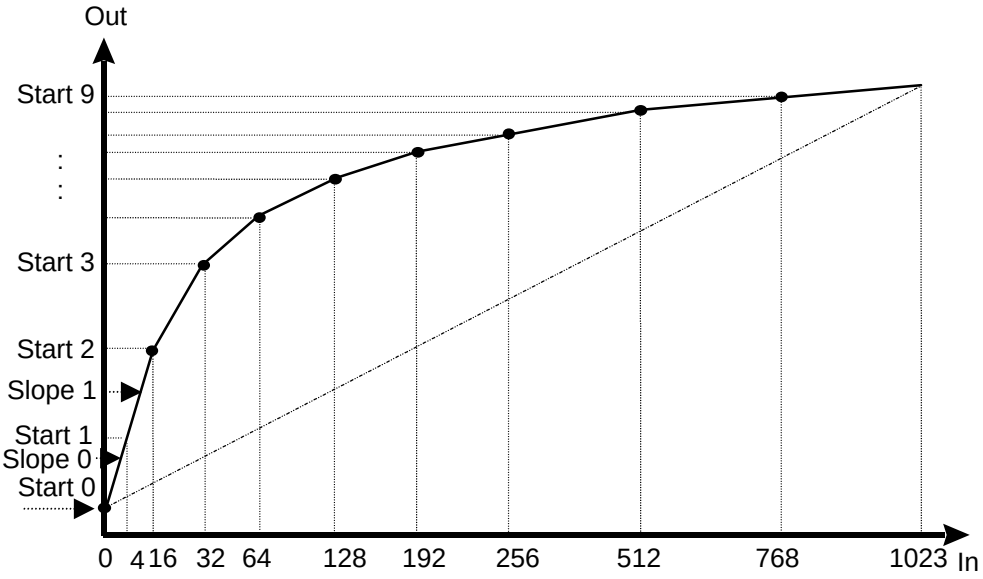

## 10bit on-chip ADC

On-chip ADC converts analog pixel voltage to 10bit digital data.

## Gamma Correction

Piecewise linear gamma approximation method is implemented. Ten piece linear segments are supported and user-programmable.

Gamma Slope Registers are programmed as the integer value of real slope value that is multiplied by 64.




Gamma Transfer Function

## Color Interpolation

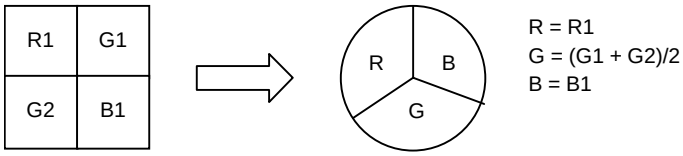
Three methods are supported to interpolate missing R, G, or B for mosaic image data from pixel array as follows.

a) 3x3 linear color interpolation

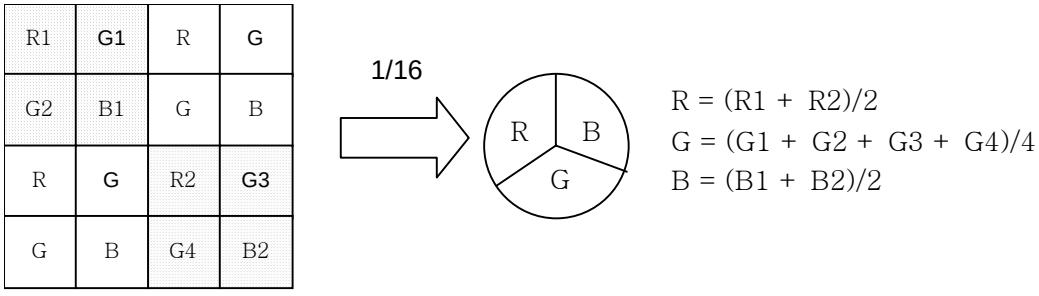
Interpolation is done by moving 3x3 interpolation window by one pixel horizontally and vertically

b) 1/4 subsampling color interpolation

Interpolation is done by moving 2x2 interpolation window by two pixels each time horizontally and vertically. The equation for color interpolation in each 2x2 window is simple as follows.




c) 1/16 subsampling color interpolation



## Color Correction & Color Space Conversion

Both of Color Correction and Color Space conversion are implemented by 3x3 matrix operation, so that two stages may be merged into one matrix stage.

Color correction matrix may be resolved by measuring sensor's color spread characteristics for primary color source and calculating the inverse matrix of color spread matrix. For color space conversion matrix, the equation from CCIR-601 standard is normally used. Therefore, the intended single matrix for color correction and color space conversion may be resolved as below.

*Intended single matrix = Color Space Conversion Matrix * Color Correction Matrix*

Intended single matrix coefficients are programmable from –127/64 to 127/64. Programming register value for intended single matrix coefficients should be resolved by the following equations.

For positive values, CMAxx = Integer (Real Coefficient Value x 64);

For negative values, CMAxx = Two Complement(Integer (Real Coefficient Value x 64));

Real Coefficient Value values from –127/64 to 127/64 can be programmed.

CCIR-601 YCbCr color space conversion equation

< Conversion Equation >
Y = (77R + 150G + 29B)/256 Range: 16 ~ 235
Cb = (-44R –87G + 131B)/256 + 128 Range: 16 ~ 240
Cr = (131R – 110G – 21B)/256 + 128 Range: 16 ~ 240

< Reverse Conversion >
R = Y + 1.371(Cr – 128)
G = Y – 0.698(Cr – 128) – 0.336(Cb – 128)
B = Y + 1.732(Cb – 128)

In the above equations, R, G, and B are gamma-corrected values.

## Digital Gain Control

Y, Cb, and Cr digital channels are scaled by this block that receives scaling values from Auto Exposure and Auto White Balance blocks. Scaling resolution is 1/128 and value range is 1.9 ~ 0.1.

## Output Formatting

The output formats such as Bayer Raw Data, RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 are supported. Possible output bus widths are 8 bits and 16bits, and the sequence of Cb and Cr are programmable.

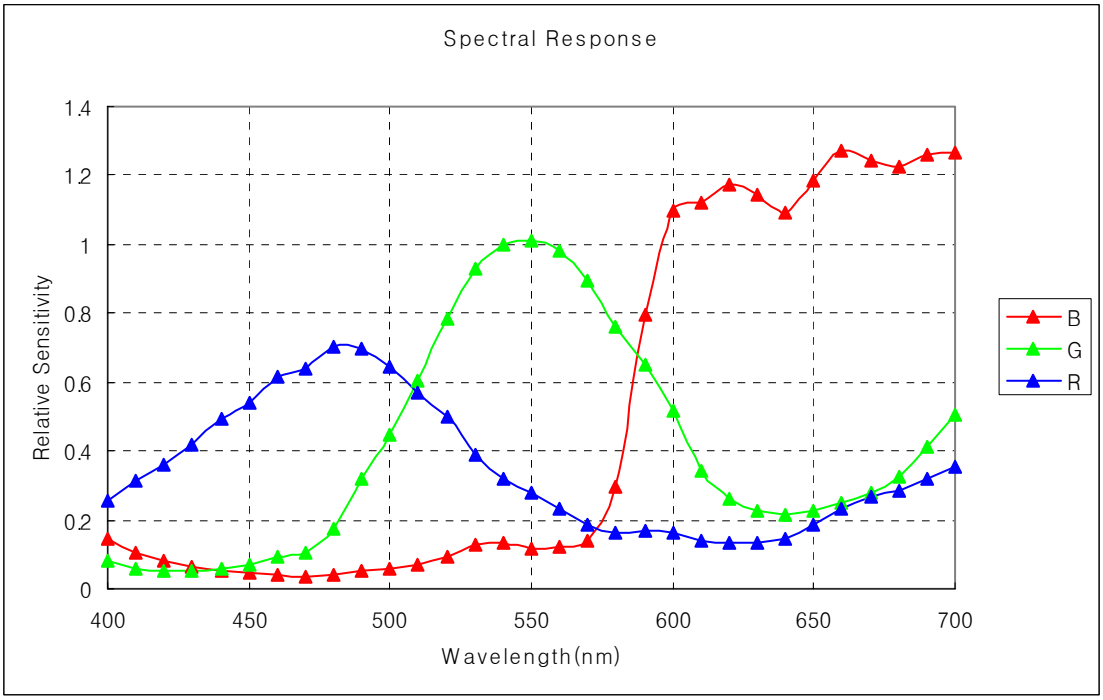
## Auto Exposure Control

Y mean value is continuously calculated every frame, and the integration time value is increased or decreased according to difference between target Y mean value and current frame Y mean value.

### Auto White Balance

Cb/Cr frame mean value is calculated every frame and according to Cb/Cr frame mean values' displacement from Cb/Cr white target point, R/B scaling values for R/B data are resolved.

### Spectral Characteristics




## Register Description

| Register | Symbol | Address (Hex) | Default (Hex) | Description |
|---|---|---|---|---|
| Device ID | DEVID | 00 | 40 | Product ID, Revision No. |
| Sensor Control A | SCTRA | 01 | 0b | Operation mode, X/Y flip, Image size |
| Sensor Control B | SCTRB | 02 | 00 | Power down, Clock division |
| Sensor Control C | SCTRC | 03 | 01 | Sensor Internal control Register |
| Row Start Address High | RSAH | 08 | 00 | Row Start Address[8] |
| Row Start Address Low | RSAL | 09 | 02 | Row Start Address[7:0] |
| Column Start Address High | CSAH | 0a | 00 | Column Start Address[9:8] |
| Column Start Address Low | CSAL | 0b | 02 | Column Start Address[7:0] |
| Window Height High | WIHH | 0c | 01 | Window Height Address[8] |
| Window Height Low | WIHL | 0d | e0 | Window Height Address[7:0] |

| | | | | |
|---|---|---|---|---|
| Window Width High | WIWH | 0e | 02 | Window Width Address[9:8] |
| Window Width Low | WIWL | 0f | 80 | Window Width Address[7:0] |
| HBLANK Time High | HBLANKH | 10 | 00 | HBLANK Time [15:8] |
| HBLANK Time Low | HBLANKL | 11 | d0 | HBLANK Time [7:0] |
| VBLANK Time High | VBLANKH | 12 | 00 | VBLANK Time [15:8] |
| VBLANK Time Low | VBLANKL | 13 | 08 | VBLANK Time [7:0] |
| Red Color Gain | RCG | 14 | 10 | Gain for Red Pixel Output |
| Green Color Gain | GCG | 15 | 10 | Gain for Green Pixel Output |
| Blue Color Gain | BCG | 16 | 10 | Gain for Blue Pixel Output |
| Preamp Gain | PREAMP | 17 | 10 | Preamp Gain for Pixel Output |
| Preamp Gain Min | PREMIN | 18 | 00 | Preamp Gain Min Value for AE |
| Preamp Gain Max | PREMAX | 19 | 3f | Preamp Gain Max Value for AE |
| Preamp Gain Nominal | PRENOM | 1a | 10 | Preamp Gain Normal Value for AE |
| ASP Bias | ASPBIAS | 1b | 13 | Amp Bias, Pixel Bias |
| Reset Clamp | RSTCLMP | 1c | 07 | Reset Level Clamping Value |
| ADC Bias | ADCBIAS | 20 | 0f | ADC Bias |
| Red Pixel Black Offset | OREDI | 21 | 7f | ADC Offset Value for Light-shielded Red Pixel |
| Green Pixel Black Offset | OGRNI | 22 | 7f | ADC Offset Value for Light-shielded Green Pixel |
| Blue Pixel Black Offset | OBLUI | 23 | 7f | ADC Offset Value for Light-shielded Blue Pixel |
| Red Pixel Active Offset | OREDU | 24 | RO | ADC Offset Value for Active Red Pixel |
| Green Pixel Active Offset | OGRNU | 25 | RO | ADC Offset Value for Active Green Pixel |
| Blue Pixel Active Offset | OBLUU | 26 | RO | ADC Offset Value for Active Blue Pixel |
| Black Level Threshold | BLCTH | 27 | ff | Black Level Threshold Value |
| ISP Function Enable | ISPFEN | 30 | 0f | Image processing functions enable |
| ISP Output Format | OUTFMT | 31 | 39 | Image data output format control |
| ISP Output Polarity | OUTINV | 32 | 00 | Output signal polarity control |
| Green Edge Threshold | EDGETH | 33 | 00 | Green pixel edge threshold for 3x3 color interpolation |
| Color Matrix Coefficient 11 | CMA11 | 34 | 2e | Color matrix coefficient 11 |
| Color Matrix Coefficient 12 | CMA12 | 35 | c5 | Color matrix coefficient 12 |
| Color Matrix Coefficient 13 | CMA13 | 36 | 0c | Color matrix coefficient 13 |
| Color Matrix Coefficient 21 | CMA21 | 37 | 0d | Color matrix coefficient 21 |

| | | | | |
|---|---|---|---|---|
| Color Matrix Coefficient 22 | CMA22 | 38 | 3c | Color matrix coefficient 22 |
| Color Matrix Coefficient 23 | CMA23 | 39 | f7 | Color matrix coefficient 23 |
| Color Matrix Coefficient 31 | CMA31 | 3a | f8 | Color matrix coefficient 31 |
| Color Matrix Coefficient 32 | CMA32 | 3b | cf | Color matrix coefficient 32 |
| Color Matrix Coefficient 33 | CMA33 | 3c | 39 | Color matrix coefficient 33 |
| Gamma Segment Point 0 | GMAP0 | 40 | 00 | Start point for gamma line segment 0 |
| Gamma Segment Point 1 | GMAP1 | 41 | 04 | Start point for gamma line segment 1 |
| Gamma Segment Point 2 | GMAP2 | 42 | 1c | Start point for gamma line segment 2 |
| Gamma Segment Point 3 | GMAP3 | 43 | 34 | Start point for gamma line segment 3 |
| Gamma Segment Point 4 | GMAP4 | 44 | 54 | Start point for gamma line segment 4 |
| Gamma Segment Point 5 | GMAP5 | 45 | 78 | Start point for gamma line segment 5 |
| Gamma Segment Point 6 | GMAP6 | 46 | 90 | Start point for gamma line segment 6 |
| Gamma Segment Point 7 | GMAP7 | 47 | a4 | Start point for gamma line segment 7 |
| Gamma Segment Point 8 | GMAP8 | 48 | e0 | Start point for gamma line segment 8 |
| Gamma Segment Point 9 | GMAP9 | 49 | f4 | Start point for gamma line segment 9 |
| Gamma Segment Slope 0 | GMAS0 | 50 | 40 | Slope value for gamma line segment 0 |
| Gamma Segment Slope 1 | GMAS1 | 51 | 80 | Slope value for gamma line segment 1 |
| Gamma Segment Slope 2 | GMAS2 | 52 | 60 | Slope value for gamma line segment 2 |
| Gamma Segment Slope 3 | GMAS3 | 53 | 40 | Slope value for gamma line segment 3 |
| Gamma Segment Slope 4 | GMAS4 | 54 | 24 | Slope value for gamma line segment 4 |
| Gamma Segment Slope 5 | GMAS5 | 55 | 18 | Slope value for gamma line segment 5 |
| Gamma Segment Slope 6 | GMAS6 | 56 | 14 | Slope value for gamma line segment 6 |
| Gamma Segment Slope 7 | GMAS7 | 57 | 0f | Slope value for gamma line segment 7 |
| Gamma Segment Slope 8 | GMAS8 | 58 | 05 | Slope value for gamma line segment 8 |
| Gamma Segment Slope 9 | GMAS9 | 59 | 02 | Slope value for gamma line segment 9 |
| AE Mode 1 | AEM1 | 60 | 39 | Auto exposure mode selection 1 |
| AE Mode 2 | AEM2 | 61 | ba | Auto exposure mode selection 2 |
| Integration Time High | INTH | 63 | 07 | Integration Time [23:16] |
| Integration Time Middle | INTM | 64 | a1 | Integration Time [15:8] |
| Integration Time Low | INTL | 65 | 20 | Integration Time [7:0] |
| AE Target | AETGT | 66 | 70 | Frame Luminance Target Value |
| AE Lock & Fine Tune Boundary | AELBND | 67 | a2 | Y frame mean value displacement boundary from AE target where AE goes into Lock state. Fine tuning boundary is also specified. |

| | | | | |
|---|---|---|---|---|
| AE Unlock Boundary | AEUNLCK | 68 | 2a | Y frame mean value displacement from AE target where AE update speed transits from 2x integration unit speed to 1x integration unit speed |
| AE Integration Step High | AEINCH | 6a | 1 | Integration Increment Step Unit [17:16] |
| AE Integration Step Middle | AEINCM | 6b | e8 | Integration Increment Step Unit [15:8] |
| AE Integration Step Low | AEINCL | 6c | 48 | Integration Increment Step Unit [7:0] |
| AE Integration Limit High | AELMH | 6d | 17 | Integration Time Limit [23:16] |
| AE Integration Limit Middle | AELMM | 6e | d7 | Integration Time Limit [15:8] |
| AE Integration Limit Low | AELML | 6f | 84 | Integration Time Limit [7:0]] |
| AWB Mode 1 | AWBM1 | 70 | 41 | AWB mode selection 1 |
| AWB Mode 2 | AWBM2 | 71 | 2 | AWB mode selection 2 |
| Cb Target | CBTGT | 73 | 80 | Cb Plane Target Frame Mean Value. Normal white point is 80h. |
| Cr Target | CRTGT | 74 | 80 | Cr Plane Target Frame Mean Value. Normal white point is 80h. |
| AWB Lock Boundary | AWBLB | 75 | 2 | Cb/Cr Frame Mean Displacement from Cb Target and Cr Target where AWB goes into LOCK state |
| AWB Unlock Boundary | AWBULB | 76 | 06 | Displacement from ideal white pixel where AWB release from LOCK state |
| AWB White Pixel Boundary | AWBWPB | 77 | 30 | Displacement from ideal white pixel where AWB recognizes a pixel as a white pixel affected by light source |
| Y Digital Gain | YGAIN | 78 | 40 | Y digital gain for Auto Exposure Control |
| Cb Digital Gain | CBGAIN | 79 | 40 | Cb digital gain for Auto White Balance control |
| Cr Digital Gain | CRGAIN | 7a | 40 | Cr digital gain for Auto White Balance control |
| AE Status | AEST | 7b | RO | AE operation status |
| AWB Status | AWBST | 7c | RO | AWB operation status |
| Y Frame Mean | YFMEAN | 7d | RO | Y Frame Mean Value |

| | | | | |
|---|---|---|---|---|
| Cb Frame Mean | CBFMEAN | 7e | RO | Cb Frame Mean Value |
| Cr Frame Mean | CRFMEAN | 7f | RO | Cr Frame Mean Value |
| Minimum Anti-Banding Gain | BNDGMIN | 80 | 08 | Minimum gain value with Anti-Banding enabled |
| Maximum Anti-Banding Gain | BNDGMAX | 81 | 18 | Maximum gain value with Anti-Banding enabled |
| Integration-Scan Plane Offset High | ISOFSH | 82 | RO | Integration-Scan Plane Offset[23:16] |
| Integration-Scan Plane Offset Middle | ISOFSM | 83 | RO | Integration-Scan Plane Offset[16:8] |
| Integration-Scan Plane Offset Low | ISOFSL | 84 | RO | Integration-Scan Plane Offset[7:0] |
| AWB Luminance High Boundary | AWBLUHI | 8a | C8 | During CbCr frame mean value calculation, AWB discards pixel of which luminance is larger than this register value. |
| AWB Luminance Low Boundary | AWBLULO | 8b | 0a | During CbCr frame mean value calculation, AWB discards pixel of which luminance is smaller than this register value. |
| AWB Valid Number | AWBNO | 8c | 02 | AWB update when the number of valid color pixel is larger than (this minimum value x 64) |
| Dark Bad Pixel Concealment Mode | DPCMODE | 90 | 0 | Dark Bad Pixel Concealment Mode selection |
| Dark Bad Integration Time High | DPCINTH | 91 | 13 | Integration Time Value High Byte where filtering operation gets active when dark bad pixel filtering mode is enabled. |
| Dark Bad Integration Time Middle | DPCINTM | 92 | 12 | Integration Time Value Middle Byte where filtering operation gets active when dark bad pixel filtering mode is enabled. |
| Dark Bad Integration Time Low | DPCINTL | 93 | D0 | Integration Time Value Low Byte where filtering operation gets active when dark bad pixel filtering mode is enabled. |
| Dark Bad G Threshold | DPCGTH | 94 | 0c | Neighbor-differential threshold value that specify G dark bad pixel |
| Dark Bad R/B Threshold | DPCCTH | 95 | 0c | Neighbor-differential threshold value that specify R/B dark bad pixel |

**Device ID [DEVID : 00h : 40h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Product ID | | | | Revision Number | | | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

High nibble represents Sensor Array Resolution, Low Nibble represents Revision Number.

**Sensor Control A [SCTRA : 01h : 0bh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Operation Mode | | | | X-Flip | Y-Flip | Video Mode | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

| Category | Operation Mode | Note |
|---|---|---|
| TestC | 1111 | At CDS operation, reset and image bit-lines are all written to high. This mode is just for monitoring purpose. |
| | 1110 | At CDS operation, image bit-line is written to high. In this mode, all Bayer data output are 8'h00. |
| | 1101 | At CDS operation, reset bit-line is written to high. In this mode, all Bayer data output are 8'hff. |
| | 1100 | Reserved |
| TestA | 10x1 | ADC overflow test with CDS output disconnected. In this mode, all Bayer data output are 8'hff. |
| | 10x0 | ADC underflow test with CDS output disconnected. In this mode, all Bayer data output are 8'h00. |
| TestI | 011x | Image processing function test |
| TestB | 0101 | I2C state machine test |
| | 0100 | Sensor operation state machine test |
| Normal | 0000 | Normal imaging operation |

| | |
|---|---|
| X-Flip | Image is horizontally flipped |
| Y-Flip | Image is vertically flipped |
| Video Mode | 11 3x3 color interpolation<br>10 1/4 subsampling mode<br>01 1/16 subsampling mode<br>00 Bayer output mode |

**Sensor Control B [SCTRB : 02h : 00h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AE/AWB Block Sleep | Datapath Block Sleep | Analog Block Sleep | Sleep Mode | Strobe Enable | Clock Division | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**< Clock Acronym Definition >**

| | |
|---|---|
| MCF : Master Clock Frequency | DCF : Divided Clock Frequency |
| SCF : Sensor Clock Frequency | ICF : Image Processing Clock Frequency |
| VCF : Video Clock Frequency | LCF : Line Clock Frequency |

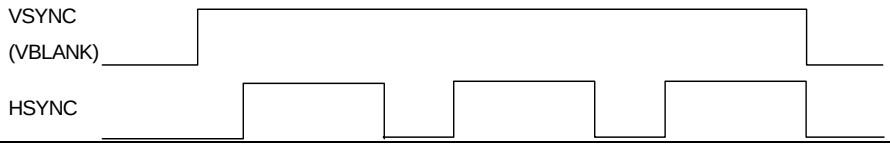
**< Clock Frequency Relation >**

| | | |
|---|---|---|
| MCF : MCF | DCF : MCF/Clock Division | |
| SCF : DCF/2 | ICF | SCF for 3x3 interpolation,<br>SCF/2 for 1/4 subsampling mode<br>SCF/4 for 1/16 subsampling mode |
| VCF : ICF for 16bit output, ICF*2 for 8bit output | LCF : 1/(HBLANK Period + HSYNC Period) | |

| | |
|---|---|
| AE/AWB Block Sleep | AE/AWB block goes into sleep mode with this bit set to high. |
| Datapath Block Sleep | Image processing datapath block goes into sleep mode with this bit set to high. |
| Analog Block Sleep | all internal analog block goes into sleep mode with this bit set to high. With All Digital Block Sleep active, sensor goes into power down mode. |
| Sleep Mode | all internal digital and analog block goes into sleep with this bit set to high. |
| Strobe Enable | When strobe signal is enabled by this bit, STROBE pin will indicates when strobe light should be splashed in the dark environment to get adequate lighted image. |
| Clock Division | divides input master clock(IMC) for internal use. Internal divided clock frequency(DCF) is defined as master clock frequency(MCF) divided by specified clock divisor. Internal divided clock frequency(DCF) is as follows.<br>000 : MCF, 001 : MCF/2, 010 : MCF/4, 011 : MCF/8<br>100 : MCF/16, 101 : MCF/32, 110 : MCF/64, 111 : MCF/128 |

**Sensor Control C [SCTRC : 03h : 01h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Black Level Average Output | Y[7:0] Pad Output with HSYNC high | C[7:0] Pad Output with 8bit mode | HSYNC in VBLANK | reserved | Unified Gain | Black Level Data Enable | Black Level Compens-ation |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|---|---|
| Black Level Average Output | This bit enable R/G/B Active Offset registers[24h-26h] to represent black level average value, instead of updated active offset values |
| Y[7:0] Pad Output with HSYNC high | With this bit set to high, Y[7:0] pads go into tri-state when HSYNC is inactive. |
| C[7:0] Pad Output with 8bit mode | With this bit set to high, C[7:0] pads go into zero driving state with 8bit output mode enabled. Otherwise, these pads go into tri-state. |
| HSYNC in VBLANK | VBLANK is equivalent to VSYNC, and HSYNC is the inversion of HBLANK, and this bit control whether HSYNC is active or not when VBLANK unit is LCF.   |
| Unified Gain | G gain is used for R, G, and B analog gain |
| Black Level Data Enable | HSYNC is generated for light-shielded pixels in 4 lines. |
| Black Level Compensation | Black level average values of light-shielded pixels are compensated when active image data is produced. |

**Row Start Address High [RSAH : 08h : 0h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | | | | | | Row Start Address High |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Row Start Address Low [RSAL : 09h : 02h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Row Start Address Low | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

Row Start Address register defines the row start address of image read out operation.

**Column Start Address High [CSAH : 0ah : 0h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | | | | | Column Start Address High | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Column Start Address Low [CSAL : 0bh : 02h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Column Start Address Low | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

Column Start Address register defines the column start address of image read out operation.

**Window Height High [WIHH : 0ch : 1h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | | | | | | Window Height High |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Window Height Low [WIHL : 0dh : e0h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Window Height Low | | | | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

Window Height register defines the height of image to be read out.

**Window Width High [WIWH : 0eh : 2h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | | | | | Window Width High | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**Window Width Low [WIWL : 0fh : 80h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Window Width Low | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Window Width Address register defines the width of image to be read out.

**HBLANK Time High [HBLANKH : 10h : 00h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HBLANK Time High | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**HBLANK Time Low [HBLANKL : 11h : d0h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HBLANK Time Low | | | | | | | |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

HBLANK Time register defines data blank time between current line and next line by using Sensor Clock Period unit (1/SCF), and should be larger than 208(d0h).

**VBLANK Time High[VBLANK : 12h : 00h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VBLANK Time High | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**VBLANK Time Low[VBLANK : 13h : 08h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VBLANK Time Low | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

VBLANK Time register defines active high duration of VSYNC output. Active high VSYNC indicates frame boundary between continuous frames. For VSYNC-HSYNC timing relation in the frame transition, please refer to Frame Timing section.

Each sensor has a little different photo-diode characteristics so that the sensor provides internal adjustment registers that calibrate internal sensing circuit in order to get optimal performance. Sensor characteristics adjustment registers are as below.

**R Color Gain [RCG : 14h : 10h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | R Color Gain | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

**G Color Gain [GCG : 15h : 10h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | G Color Gain | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

**B Color Gain [BCG : 16h : 10h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | B Color Gain | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

There are three color gain registers for R, G, B pixels, respectively. Programmable range is from 0.5X ~ 2.5X. Effective Gain = 0.5 + B<5:0>/32. These registers may be used for white balance and color effect with independent R,G,B color control. Default gain is 1X.

**Preamp Gain [PREAMP : 17h : 10h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Preamp Gain | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

Preamp Gain is common gain for R, G, B channel and used for auto exposure control. Programmable range is from 0.5X ~ 16.5X. Default gain is 1.5X.
Gain = 0.5 + B<7:0>/16

**Preamp Gain Min [PREMIN : 18h : 00h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Preamp Gain Min | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Preamp Gain Min is minimum value of preamp gain when sensor adjusts pre-amplifier gain for auto exposure control. Programmable range is same as preamp gain. Recommended value is 0.5X.

**Preamp Gain Max [PREMAX : 19h : 3fh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Preamp Gain Max | | | | | | | |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

Preamp Gain Max is maximum value of preamp gain when sensor adjusts preamp gain for auto

exposure control. Programmable range is same as preamp gain. Recommended value is 16.5X.

**Preamp Gain Normal [PRENOR : 1ah : 10h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Preamp Gain Normal | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

Preamp Gain Normal is reference value of preamp gain when sensor adjusts preamp gain for auto exposure control. First, sensor controls integration time before adjusting preamp gain for auto exposure control. After integration time is changed to the minimum or maximum value, sensor adjusts preamp gain from this register value. Refer to figure of AE mode1 register(60H).

Programmable range is same as preamp gain. Recommended value is 1.5X.

**ASP Bias [ASPBIAS : 1bh : 13h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | Pixel Bias | | | Amp Bias | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

| | |
|---|---|
| Pixel Bias | controls the amount of current in internal pixel bias circuit to amplify pixel output effectively. The larger register value increases the amount of current. |
| Amplifier Bias | controls the amount of current in internal amplifier bias circuit to amplify pixel output effectively. The larger register value increases the amount of current. |

**Reset Level Clamp [RSTCLMP : 1ch : 07h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | Reset Level Clamp | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

Because extremely bright image like sun affects reset data voltage of pixel to lower, bright image is captured as black image in image sensor regardless of correlated double sampling. To solve this extraordinary phenomenon, we adopt the method to clamp reset data voltage. Reset Level Clamp controls the reset data voltage to prevent inversion of extremely bright image. The larger register value clamps the reset data level at highest voltage level. Default value is 7 to clamp the reset data level at appropriate voltage level.

**ADC Bias [ADCBIAS : 20h : 0fh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | ADC Bias | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

ADC Bias controls the amount of current in ADC bias circuit to operate ADC effectively. The larger register value increases the amount of current.

**Red Pixel Black Offset [OREDI : 21h : 7fh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Red Pixel Black Offset | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Green Pixel Black Offset [OGRNI : 22h : 7fh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Green Pixel Black Offset | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Blue Pixel Black Offset [OBLUI : 23h : 7fh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Blue Pixel Black Offset | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

These registers control the offset voltage of ADC that changes the black level value for light-shielded pixels, red, green and blue pixel respectively. Register bit functions are composed as follows.

| | |
|---|---|
| Pixel Black Offset[7] | The bit specifies whether to subtract or add offset voltage in ADC input for light-shielded pixels. |
| Pixel Black Offset[6:0] | This value specifies the amount of offset voltage for light-shielded pixels. |

**Red Pixel Active Offset [OREDU : 24h : RO]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Red Pixel Active Offset | | | | | | | |
| RO | RO | RO | RO | RO | RO | RO | RO |

**Green Pixel Active Offset [OGRNU : 25h : RO]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

| Green Pixel Active Offset | | | | | | | |
|---|---|---|---|---|---|---|---|
| RO | RO | RO | RO | RO | RO | RO | RO |

**Blue Pixel Active Offset [OBLUU : 26h : RO]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Blue Pixel Active Offset | | | | | | | |
| RO | RO | RO | RO | RO | RO | RO | RO |

These registers control the offset voltage of ADC that changes the black level value for active pixels, red, green and blue pixel respectively. The registers are internally updated by black level compensation logic, and are read-only registers. Register bit functions are composed as follows.

| | |
|---|---|
| Pixel Active Offset[7] | The bit specifies whether to subtract or add offset voltage in ADC input for active pixels. |
| Pixel Active Offset[6:0] | This value specifies the amount of offset voltage for active pixels. |

**Black Level Threshold [BLCTH : 27h : ffh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Black Level Threshold | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The register specifies the maximum value which determines whether light-shielded pixel output is valid. When light-shielded pixel output exceeds this limit, the pixel is not accounted for black level calculation.

**ISP Function Enable [ISPFEN : 30h : 0fh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | Matrix Operation | Color Interpolation | Gamma Correction | reserved |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

| | |
|---|---|
| Matrix Conversion | In HV7131GP, two matrix operations of color correction & color space conversion are merged into one matrix operation. With this bit set to high, the matrix operation is enabled, and otherwise R/G/B data is output through output formatter. |
| Color Interpolation | With SCTRA[1:0] set to 3x3 color interpolation, this bit control the final channel between color interpolated R/G/B and Bayer data. With this bit set |

| | |
|---|---|
| | to low, R/G/B channels for one pixel are fed with the same one Bayer value so that image similar to black & white is produced. |
| Gamma Correction | With this bit set to high, 10 segments piecewise approximate gamma is enabled. |

**Output Format [OUTFMT : 31h : 39h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma-corrected Bayer | Bayer 8bit output | Cb First | Y First | 8 Bit Output | reserved | YCbCr 4:4:4 | YCbCr 4:2:2 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

| | |
|---|---|
| Gamma-corrected Bayer | Bayer data that are gamma corrected is output when Bayer mode is set in SCTRA register. |
| Bayer 8bit output | Bayer data is output with 8bit mode. two LSB of 10 bit Bayer data is stripped out. |
| Cb First | Cb pixel in front of Cr pixel in 16bit or 8bit video data output modes |
| Y First | Y pixel in front of Cb and Cr pixels in 8bit video output mode. This option is meaningful only with 8bit output mode. |
| 8 Bit Output | Image Data is produced only in Y[7:0]. C[7:0] should be discarded |
| YCbCr 4:4:4 | YCbCr 24bit data for a pixel is produced with 16bit output mode. With color space conversion disabled, RGB 24bit data for a pixel is produced in this mode. This mode is meaningful only with 16bit output mode. |
| YCbCr 4:2:2 | YCbCr data for a pixel is produced with 8/16 output mode |

**Output Inversion[OUTINV : 32h : 0h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | | | Clocked HSYNC | VSYNC inversion | HSYNC inversion | VCLK inversion |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| Clocked HSYNC | In HSYNC, VCLK is embedded, that is, HSYNC is toggling at VCLK rate during normal HSYNC time |
| VSYNC inversion | VSYNC output polarity is inverted |
| HSYNC inversion | HSYNC output polarity is inverted |

| | |
|---|---|
| VCLK inversion | VCLK output polarity is inverted |

**Green Edge Threshold[EDGETH : 33h : 00h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Green Edge Threshold | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

In 3x3 color interpolation mode, missing G pixel is interpolated with edge detection considering neighbor G pixels, and this register controls edge threshold to select edge direction. The smaller value means that the more patterns are recognized as edge, and image may get sharper, but not always.

**Color Matrix Coefficients**

Both of Color Correction and Color Space conversion are implemented by 3x3 matrix operation, so that two stages may be merged into one matrix stage.

Color correction matrix may be resolved by measuring sensor's color spread characteristics for primary color source and calculating the inverse matrix of color spread matrix. For color space conversion matrix, the equation from CCIR-601 standard is normally used. Therefore, the intended single matrix for color correction and color space conversion may be resolved as below.

*Intended single matrix = Color Space Conversion Matrix * Color Correction Matrix*

Intended single matrix coefficients are programmable from –127/64 to 127/64. Programming register value for intended single matrix coefficients should be resolved by the following equations.

For positive values, CMAxx = Integer(RealCoefficientValue x 64);

For negative values, CMAxx = TwoComplement(Integer(RealCoefficientValue x 64));

RealCoefficientValue values from –127/64 to 127/64 can be programmed.

CCIR-601 YCbCr color space conversion equation

< Conversion Equation >
Y = (77R + 150G + 29B)/256 Range: 16 ~ 235
Cb = (-44R –87G + 131B)/256 + 128 Range: 16 ~ 240
Cr = (131R – 110G – 21B)/256 + 128 Range: 16 ~ 240

< Reverse Conversion >
R = Y + 1.371(Cr – 128)
G = Y – 0.698(Cr – 128) – 0.336(Cb – 128)
B = Y + 1.732(Cb – 128)

In the above equations, R, G, and B are gamma-corrected values

**Color Matrix Coefficient 11 [CMA11 : 34h : 2eh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

| Color Matrix Coefficient 11 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |

**Color Matrix Coefficient 12 [CMA12 : 35h : c5h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Color Matrix Coefficient 12 | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |

**Color Matrix Coefficient 13 [CMA13 : 36h : 0ch]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Color Matrix Coefficient 13 | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

**Color Matrix Coefficient 21 [CMA21 : 37h : 0dh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Color Matrix Coefficient 21 | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

**Color Matrix Coefficient 22 [CMA22 : 38h : 3ch]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Color Matrix Coefficient 22 | | | | | | | |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |

**Color Matrix Coefficient 23 [CMA23 : 39h : f7h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Color Matrix Coefficient 23 | | | | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

**Color Matrix Coefficient 31 [CMA31 : 3ah : f8h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Color Matrix Coefficient 31 | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

**Color Matrix Coefficient 32 [CMA32 : 3bh : cfh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

| Color Matrix Coefficient 32 | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |

**Color Matrix Coefficient 33 [CMA33 : 3ch : 39h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Color Matrix Coefficient 33 | | | | | | | |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

**Gamma Segment Start Points**

Gamma Segment Start Points specify the start points of nine line segments for piecewise gamma approximation. Current default gamma curve is very selected for optimum gray gradation.

**Gamma Point 0 [GAMP0 : 40h : 00h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Point 0 | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Gamma Point 1 [GMAP1 : 41h : 04h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Point 1 | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**Gamma Point 2 [GMAP2 : 42h : 1ch]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Point 2 | | | | | | | |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

**Gamma Point 3 [GMAP3 : 43h : 34h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Point 3 | | | | | | | |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

**Gamma Point 4 [GMAP4 : 44h : 54h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Point 4 | | | | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |

**Gamma Point 5 [GMAP5 : 45h : 78h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Point 5 | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

**Gamma Point 6 [GMAP6 : 46h : 90h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Point 6 | | | | | | | |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

**Gamma Point 7 [GMAP7 : 47h : a4h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Point 7 | | | | | | | |
| 1 | 0- | 1 | 0 | 0 | 1 | 0 | 0 |

**Gamma Point 8 [GMAP8 : 48h : e0h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Point 8 | | | | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

**Gamma Point 9 [GMAP9 : 49h : f4h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Point 9 | | | | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

**Gamma Slope Values**

Gamma Slope Registers are programmed as the integer value of real slope value that is multiplied by 64.

**Gamma Slope 0 [GMAS0 : 50h : 40h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Slope 0 | | | | | | | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Gamma Slope 1 [GMAS1 : 51h : 80h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Slope 1 | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Gamma Slope 2 [GMAS2 : 52h : 60h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Slope 1 | | | | | | | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

**Gamma Slope 3 [GMAS3 : 53h : 40h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Slope 3 | | | | | | | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Gamma Slope 4 [GMAS4 : 54h : 24h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Slope 4 | | | | | | | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |

**Gamma Slope 5 [GMAS5 : 55h : 18h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Slope 5 | | | | | | | |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

**Gamma Slope 6 [GMAS6 : 56h : 14h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Slope 6 | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

**Gamma Slope 7 [GMAS7 : 57h : 0fh]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Slope 7 | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Gamma Slope 8 [GMAS8 : 58h : 05h]**

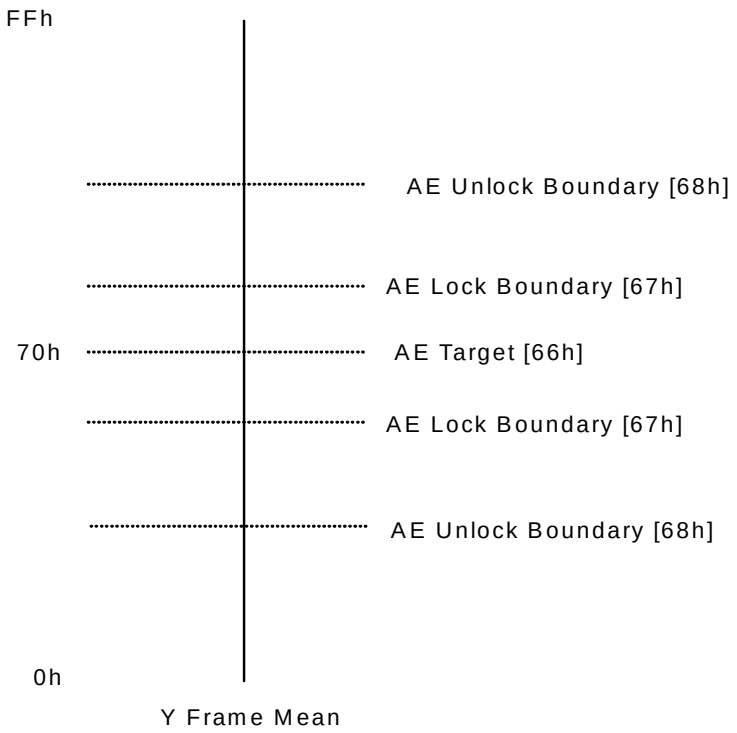
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Slope 8 | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Gamma Slope 9 [GMAS9 : 59h : 02h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gamma Slope 9 | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

## Auto Exposure

Y mean value is continuously calculated every frame, and the integration time value is increased or decreased according to the displacement between current frame Y mean value and target Y mean value.




**AE Mode Control 1 [AEM1 : 60h : 39h]**

| 7 | 6 | 5 4 | 3 2 | 1 0 |
|---|---|---|---|---|
| Anti – Banding Enable | Full Window | Window Mode | AE speed | AE Mode |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

| | | |
|---|---|---|
| Anti-Banding Enable | When Anti-Banding is enabled, AE initializes Integration Time registers[63h-65h] to 4 x Anti-Banding Step value[6ah-6ch], and integration increment/decrement amount is set to Anti-Banding Step value in order to remove banding noise caused by intrinsic energy waveform of light sources. Banding noise is inherent in CMOS image sensor that adopts rolling shutter scheme for image acquisition. In this mode, AE operates with very large unit, typically a reciprocal of (2 x power line frequency), so that minute integration time tuning is not liable. Therefore, this mode is recommended for only indoor use. | |
| Full Window | With this bit set to high, window mode is discarded and full image data is accounted for AE Y frame mean evaluation | |
| Window Mode | 11 | 1/8 center weighted window mode. Weighting ratio is 8:1 for inside area vs. outside area |
| | 10 | 1/8 center only window mode. |
| | 01 | 1/4 center weighted window mode. Weighting ratio is 4:1 for inside area vs. outside area |
| | 00 | 1/4 center only window mode. |
| AE Speed | (fast)11 - 10 - 01 - 00(slow) | |
| AE Mode | 11 | Gain-Only control mode. Only preamp gain is controlled to get optimum exposure state. |
| | 10 | Time-Only control mode. Only integration time is controlled to get optimum exposure state. |
| | 01 | Time-Gain control mode. integration time and preamp gain are controlled to get optimum exposure state. |
| | 00 | AE function is disabled |

**AE Mode Control 2 [AEM2 : 61h : bah]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Gain Speed | | Integration Time Fine Tune | Preamp Gain Fine Tune | Anti-Banding Minimum Break | AE Subsampli-ng mode | AE Analog Gain Control | AE Digital Gain control |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |

| | |
|---|---|
| Gain Speed | Gain update speed is specified as follows.<br>(fast)11 - 10 - 01 - 00(slow) |
| Integration Time Fine Tune | Integration time fine tuning is performed when AE arrive around AE Fine Tune Boundary to settle into AE lock state smoothly. |
| Preamp Gain Fine Tune | Preamp gain fine tuning is performed when AE arrive around AE Fine Tune Boundary to settle into AE lock state smoothly. |
| Anti-Banding Minimum Break | When AE is still of out lock state despite that AE preamp analog gain update value exceeds preamp minimum gain value(18h) and integration time(63h-65h) is reached to AE Anti-Banding Step(6ah-6ch), integration time(63h-65h) is broken to less than AE Anti-Banding Step(6ah-6ch). |
| AE Subsampling Mode | AE statistics is executed on 1/4 of original image data to save power consumption |
| AE Analog Gain Control | AE updates preamp gain register(17h) in order to reach optimum exposure state |
| AE Digital Gain Control | AE updates Y digital gain register(78h) in order to reach optimum exposure state |

**Integration Time High [INTH: 63h : 07h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Integration Time High [23:16] | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

**Integration Time Middle [INTM: 64h: a1h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Integration Time Middle[15:8] | | | | | | | |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

**Integration Time Low [INTL: 65h: 20h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Integration Time Low[7:0] | | | | | | | |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

Integration time value register defines the time during which active pixel element evaluates photon energy that is converted to digital data output by internal ADC processing. Integration time is equivalent to exposure time of general camera so that integration time need to be increased in dark environment

and decreased according to lighting condition. Maximum integration time is register maximum value($2^{24}$-1) x sensor clock period(80ns, SCF 12.5Mhz @ DCF 25Mhz) = 1.34sec.

**AE Target [AETGT : 66h : 70h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AE Target | | | | | | | |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

This register defines the target luminance value for AE operation.

**AE Lock Boundary [AELBND : 67h : a2h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AE Fine Boundary | | | | AE Lock Boundary | | | |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

AE Lock Boundary specifies the displacement of Y Frame Mean value(7dh) from AE Target in which AE goes into LOCK state. With Anti-Banding is enabled, this displacement condition is discarded, and instead AE Unlock Boundary is used as Lock boundary.

AE Fine Boundary specifies the displacement of Y Frame Mean value(7dh) from AE Target in which AE start to tune fine integration time or preamp gain in order to goes into lock state smoothly.

**AE Unlock Boundary [AEUNLCK : 68h : 2ah]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AE Unlock Boundary | | | | | | | |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

AE Unlock Boundary 0 specifies Y Frame Mean displacement from AE Target where integration time increment/decrement speed changes from 2x (integration unit step) to 1x (integration unit step). In anti-banding mode, this boundary is used as lock boundary for exposure control.

**AE Anti-Banding Step High [AEANTH : 6ah : 1h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | | | | | | AE Anti-Banding Step High | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**AE Anti-Banding Step Middle [AEANTM : 6bh : e8h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

| AE Anti-Banding Step High | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |

**AE Anti-Banding Step Low [AEANTL : 6ch : 48h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AE Anti-Banding Step Low | | | | | | | |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

AE Anti-Banding Step specifies integration time unit value that AE uses when Anti-Banding is enabled. Anti-Banding Step value is resolved by the following equation.

Anti-Banding Step Value = Sensor Operation Frequency (SCF) / (2x power line frequency)

The default value is set with SCF 12.5Mhz, 50Hz power line, that is,

Anti-Banding Step Value = 12.5Mhz / (2 x 50) = 125000d = 1e848h

**AE Integration Time Limit High [AELMH : 6dh : 17h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AE Integration Time Limit High | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

**AE Integration Time Limit Middle [AELMM : 6eh : d7h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AE Integration Time Limit Middle | | | | | | | |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |

**AE Integration Time Limit Low [AELML : 6fh : 84h]**

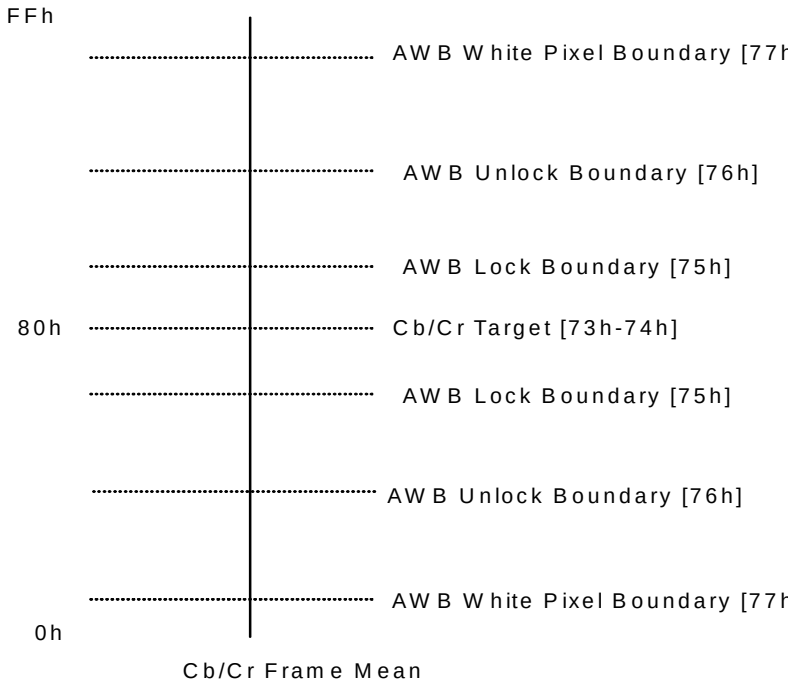
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AE Integration Time Limit Low | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

These three registers define the maximum integration time value that is allowed to sensor operation. It is desirable to set the value to multiples of AE Anti-Banding Step to easily operate with Anti-banding mode enabled. The default value is set to 1/8sec with SCF set to 25Mhz

12.5Mhz / 8 = 1,562,500 = 17d784

## Auto White Balance

Cb/Cr frame mean value is calculated every frame and according to Cb/Cr frame mean values' displacement from Cb/Cr white target point, R/B scaling values for R/B data are resolved.




**AWB Mode Control 1 [AWBM : 70h : 41h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | Full Window | Window Mode | | AWB speed | | reserved | AWB On |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

| | | |
|---|---|---|
| Full Window | With this bit set to high, window mode is discarded and full image data is accounted for AE Y frame mean evaluation | |
| Window Mode | 11 | 1/8 center weighted window mode. Weighting ratio is 8:1 for inside area vs. outside area |
| | 10 | 1/8 center only window mode. |
| | 01 | 1/4 center weighted window mode. Weighting ratio is 4:1 for inside area vs. outside area |
| | 00 | 1/4 center only window mode. |

| | |
|---|---|
| AWB Speed | (Fast)11 - 10 - 01 - 00(slow) |
| AWB On | Auto White Balance Control Enabled |

**AWB Mode Control 2 [AEM2 : 71h : 02h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | AWB Low Speed | AWB Subsampli-ng mode | AWB Analog Gain Control | AWB Digital Gain control |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| | |
|---|---|
| AWB Low Speed | With this bit set to high, analog gain speed is decreased to 1/4 of the normal speed. |
| AWB Subsampling Mode | AWB statistics is executed on 1/4 of original image data to save power consumption |
| AWB Analog Gain Control | AWB updates R/B gain registers(14h,16h) in order to reach optimum white balance state |
| AWB Digital Gain Control | AWB updates Cb/Cr digital gain registers(79h,7ah) in order to reach optimum white balance state |

**Cb Target [CBTGT : 73h : 80h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Cb Target | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register defines Cb target frame mean value for AWB operation.

**Cr Target [CRTGT : 74h : 80h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Cr Target | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register defines Cr target frame mean value for AWB operation.

**AWB Lock Boundary [AWBLB : 75h : 2h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | AWB Lock Boundary | | | |

| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
|---|---|---|---|---|---|---|---|

It specifies Cb/Cr frame mean values' displacement from Cb/Cr Target (73h-74h) value where AWB goes into LOCK state.

**AWB Unlock Boundary [AWBUB : 76h : 06h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AWB Unlock Boundary | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

It specifies Cb/Cr frame mean values' displacement from Cb/Cr Target (73h-74h) where AWB is released from LOCK state. AWB operation retains LOCK state unless Cb/Cr frame mean values' displacement value exceeds this boundary. The value should be larger AWB Lock Boundary.

**AWB White Pixel Boundary [AWBWPB : 77h : 30h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AWB White Pixel Boundary | | | | | | | |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

When Cb/Cr frame mean values' displacement from Cb/Cr Target exceeds AWB White Pixel Boundary value, AWB accept frame color as it is and does not try to correct white balance deviation.

**Y Digital Gain [YGAIN : 78h : 40h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Y Digital Gain | | | | | | | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

The register represents the current Y digital gain value (1/64 resolution) in Digital Gain block, and is updated every frame by AE logic when AE digital gain update mode is active.

**Cb Digital Gain [CBGAIN : 79h : 40]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Cb Digital Gain | | | | | | | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

The register represents the current Cb digital gain value (1/64 resolution) in Digital Gain block, and is updated every frame by AWB logic when AWB digital gain update mode is active.

**Cr Digital Gain [AWBSCLB : 7ah : 40h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Cr Digital Gain | | | | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

The register represents the current Cr scaling value(1/64 resolution) in Digital Gain block, and is updated every frame by AWB logic when AWB digital gain update mode is active.

**AE Status [AEST : 7bh : RO]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AE Mode State | | | | AE Lock state | | | |
| RO | RO | RO | RO | RO | RO | RO | RO |

| | |
|---|---|
| AE Mode State | This nibble represents the mode where internal Y plane FSM is currently placed among time-gain control, time-only control, or gain-only control modes. |
| AE Lock State | Y channel FSM status, “0000” means that AE Y plane is in lock state |

**AWB Status [AWBST : 7ch : RO]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | AE/AWB Lock | Cb Lock State | | Cr Lock State | |
| RO | RO | RO | RO | RO | RO | RO | RO |

| | |
|---|---|
| AE/AWB Lock | This single status bit indicates that AE and AWB are in lock state for optimum still image capture. |
| Cb Lock State | Cb channel FSM status. “00” means that AWB Cb plane is in lock state |
| Cr Lock State | Cr channel FSM status. “00” means that AWB Cr plane is in lock state |

**Y Frame Mean [YFMEAN : 7dh : RO]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Y Frame Mean | | | | | | | |
| RO | RO | RO | RO | RO | RO | RO | RO |

The register reports current Y plane frame mean value.

**Cb Frame Mean [CBFMEAN : 7eh : RO]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Cb Frame Mean | | | | | | | |
| RO | RO | RO | RO | RO | RO | RO | RO |

The register reports current Cb plane frame mean value.

**Cr Frame Mean [CRFMEAN : 7fh : RO]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Cr Frame Mean | | | | | | | |
| RO | RO | RO | RO | RO | RO | RO | RO |

The register reports current Cr plane frame mean value.

**Minimum Anti-Banding Gain [BNDGMIN : 80h : 08h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Minimum Anti-Banding Gain | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

The register specifies the minimum limit to which AE may decrease preamp gain or Y digital gain in order to get optimum exposure value while Anti-Banding Mode is enabled and the following condition is met.

*AE Lock Boundary < (Y Frame Mean - AE Target) < AE Unlock Boundary.*

**Maximum Anti-Banding Gain [BNDGMAX : 81h : 18h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Maximum Anti-Banding Gain | | | | | | | |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

The register specifies the maximum limit to which AE may increase preamp gain or Y digital gain in order to get optimum exposure value while Anti-Banding Mode is enabled and the following condition is met.

*AE Lock Boundary < (AE Target - Y Frame Mean) < AE Unlock Boundary.*

**Integration-Scan Offset High [ISOFSH : 82h : RO]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Integration-Scan Offset High | | | | | | | |
| RO | RO | RO | RO | RO | RO | RO | RO |

**Integration-Scan Offset Middle [ISOFSM : 83h : RO]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Integration-Scan Offset Middle | | | | | | | |
| RO | RO | RO | RO | RO | RO | RO | RO |

**Integration-Scan Offset Low [ISOFSH : 84h : RO]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Integration-Scan Offset Low | | | | | | | |
| RO | RO | RO | RO | RO | RO | RO | RO |

The register represents time offset between integration plane and scan plane. The value should be the same as the value specified by integration time register(63h – 65h).

**AWB Luminance High Boundary [AWBLUHI : 8ah : c8h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AWB Luminance High Boundary | | | | | | | |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

During Cb/Cr frame mean value calculation, AWB discards pixel of which luminance value is larger than this register value.

**AWB Luminance Low Boundary [AWBLULO : 8bh : 0ah]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AWB Luminance Low Boundary | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

During Cb/Cr frame mean value calculation, AWB discards pixel of which luminance value is smaller than this register value.

**AWB Valid Number [AWBNO : 8ch : 02h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AWB Valid Number | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

AWB update when the number of valid color pixel is larger than (this valid value x 64).

**Dark Bad Pixel Concealment Mode [DPCMODE : 90h : 0h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | Dark Bad Pixel Concealment Mode | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| Dark Bad Pixel Concealment | 10 | Dark Bad Pixel Concealment is always performed. |

| | | |
|---|---|---|
| Mode | 01 | Dark Bad Pixel Concealment is performed when Integration Time (63h-65h) exceeds Dark Bad Integration Time(91h-93h) |
| | 11, 00 | Dark Bad Pixel Concealment is turned off |

**Dark Bad Integration Time High [DPCINTH : 91h : 13h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Dark Bad Integration Time High | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

**Dark Bad Integration Time Middle [DPCINTM : 92h : 12h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Dark Bad Integration Time Middle | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

**Dark Bad Integration Time Low [DPCINTL : 93h : d0h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Dark Bad Integration Time Low | | | | | | | |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

Dark Bad Integration Time registers(91h-93h) specify minimum integration time value(63h-65h) where dark bad concealment operation is performed when dark bad pixel concealment mode is “01 (binary)”.

**Dark Bad G Threshold [DPCGTH : 94h : 0ch]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Dark Bad G Threshold | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

The register value specify the current G pixel’s differential value with neighboring G pixels, and is used to check whether current G pixel is dark bad pixel or not.

**Dark Bad C Threshold [DPCGTH : 95h : 0ch]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Dark Bad C Threshold | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

The register value specify the current R or B pixel's differential value with neighboring G pixels, and is used to check whether current R or B pixel is dark bad pixel or not.

## Frame Timing

For clear description of frame timing, clocks' acronym and relation are reminded in here again.

**< Clock Acronym Definition >**

| | |
|---|---|
| MCF : Master Clock Frequency | DCF : Divided Clock Frequency |
| SCF : Sensor Clock Frequency | ICF : Image Processing Clock Frequency |
| VCF : Video Clock Frequency | LCF : Line Clock Frequency |

**< Clock Frequency Relation >**

| | | |
|---|---|---|
| MCF : MCF | DCF : MCF/Clock Division | |
| SCF : DCF/2 | ICF | SCF for 3x3 interpolation,<br>SCF/2 for 1/4 subsampling mode<br>SCF/4 for 1/16 subsampling mode |
| VCF : ICF for 16bit output, ICF*2 for 8bit output | LCF : 1/(HBLANK Period + HSYNC Period) | |

HBLANK Period : HBLANK Time register value * (1/SCF)

HSYNC Period : HSYNC Active Time

**< Frame Time Calculation >**

Core Frame Time is

(IDLE SLOT + Video Height * LCP)

and Real Frame Time is resolved as follows.

When Integration Time > Core Frame Time, Real Frame Time is (Integration Time + VBLANK * LCP), otherwise is (Core Frame Time + VBLANK * LCP).

**1. 3x3 Color Interpolation Timing**

| **3x3 Color Interpolation Frame Timing Related Parameters** | | | |
|---|---|---|---|
| Master Clock Frequency(MCF) | 20Mhz | Divided Clock Frequency(DCF) | MCF/1 = 20Mhz |
| Sensor Clock Frequency(SCF) | DCF/2 = 10Mhz | Sensor Clock Period(SCP) | 1/10Mhz = 100ns |
| Window Width | 640 | Window Height | 480 |
| HBLANK Value | 208 | VBLANK Value | 8 |
| VSYNC Mode | Line Mode | Line Clock Period(LCP) | 848 SCPs |
| Output Bus Width | 8bit | VGA Video Output Frequency | SCF * 2 = 20Mhz |

| | | | |
|---|---|---|---|
| Final Video Output Size | 640x480 | . | . |

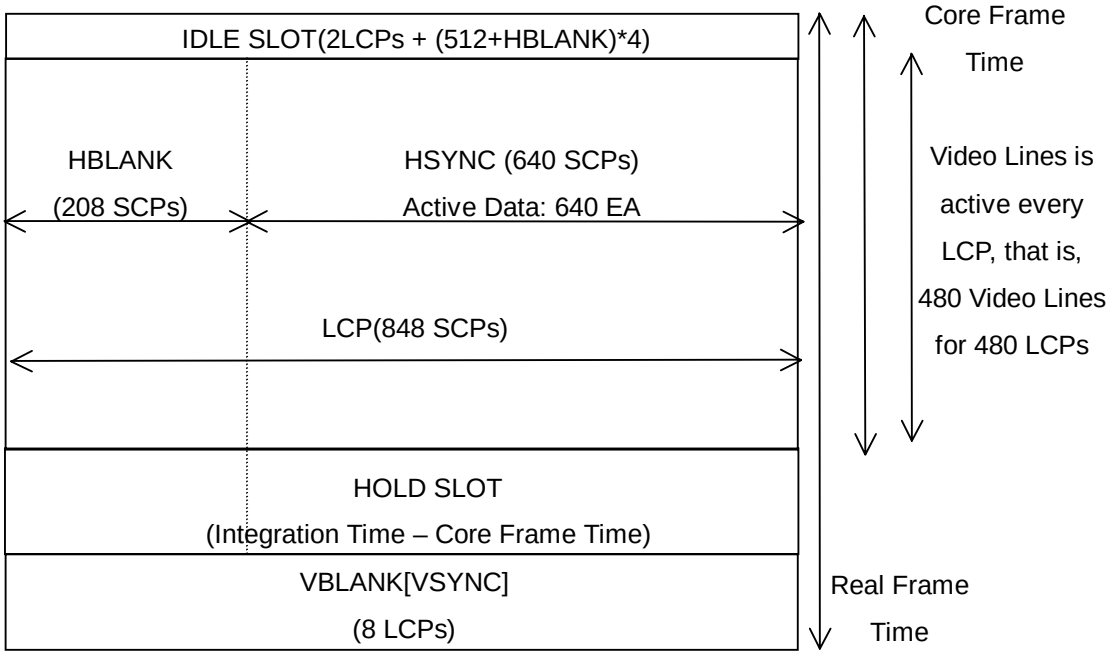
If Integration Time < Core Frame Time, Real Frame Time is

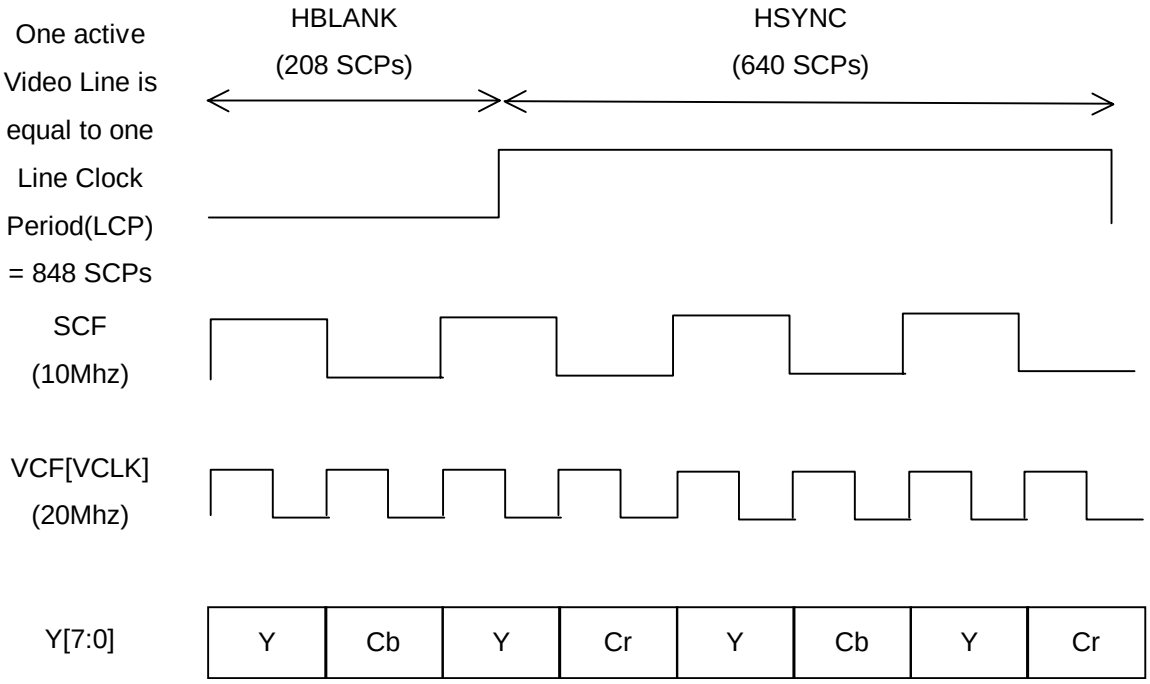
2 * (208 + 640) SCPs + 480 * (208 + 640) SCPs + 8 * (208 + 640) SCPs = 415520 SCPs = 0.041552sec

else Real Frame Time is

Integration Time * SCPs + 8 * (208 + 640) SCPs.

HOLD SLOT in frame timing appears only if integration time is larger than core frame time.

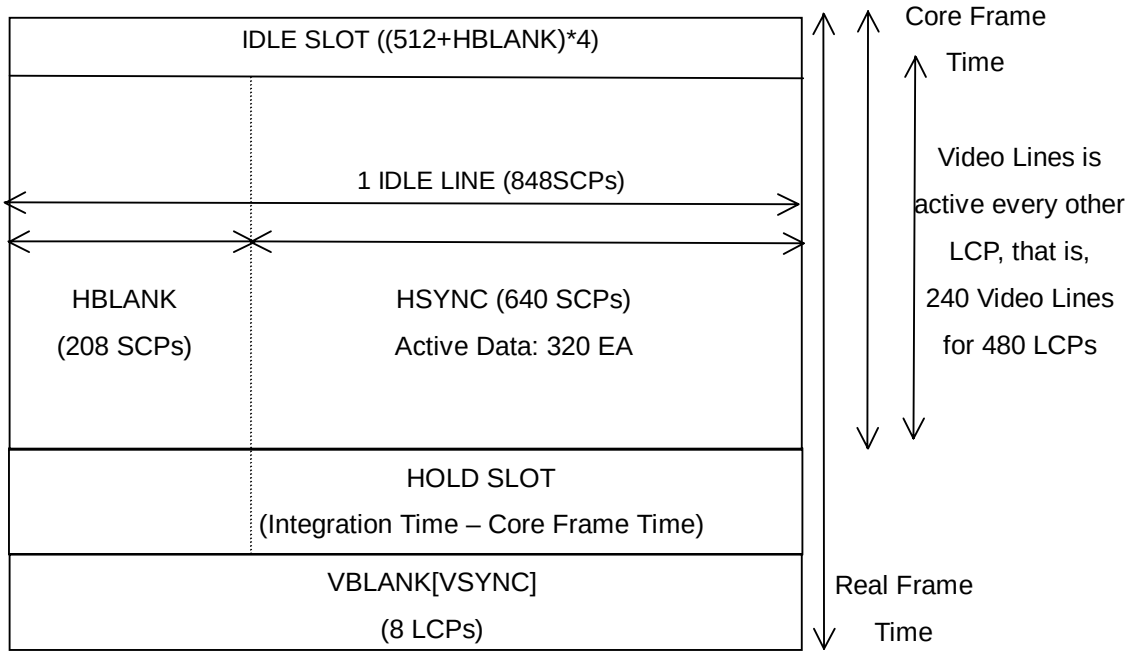


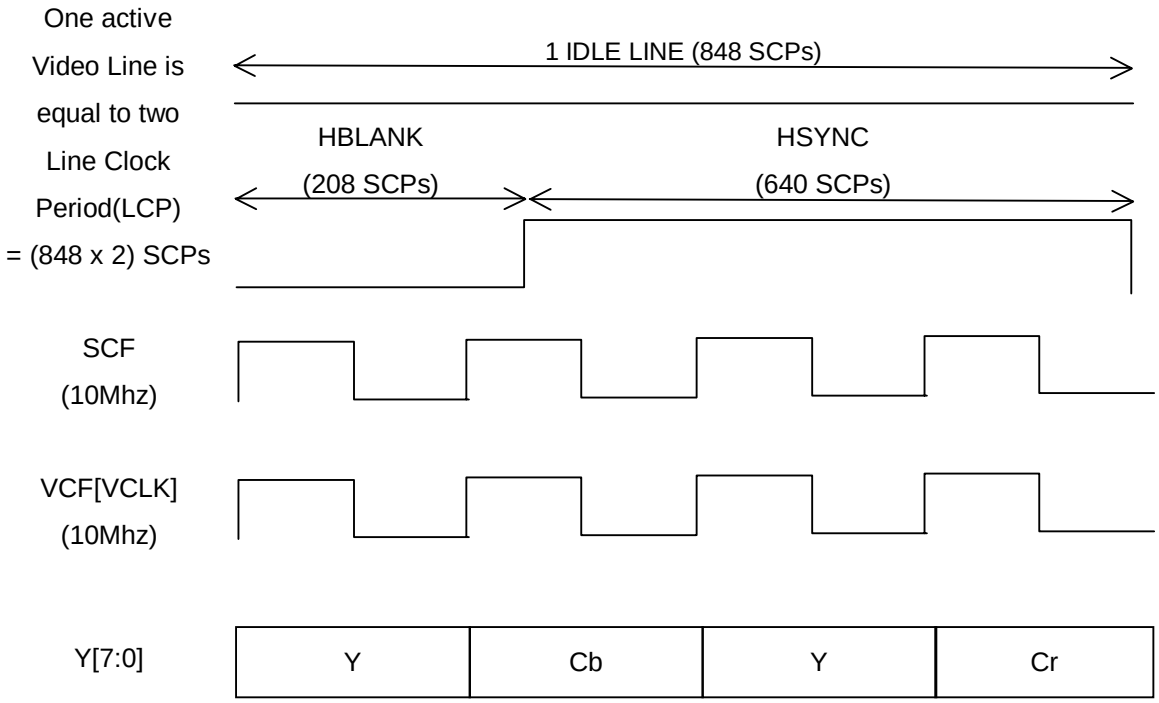



**2. 1/4 Subsampling Timing**

| 1/4 Subsampling Frame Timing Related Parameters | | | |
|---|---|---|---|
| Master Clock Frequency(MCF) | 20Mhz | Divided Clock Frequency(DCF) | MCF/1 = 20Mhz |
| Sensor Clock Frequency(SCF) | DCF/2 = 10Mhz | Sensor Clock Period(SCP) | 1/10Mhz = 100ns |
| Window Width | 640 | Window Height | 480 |
| HBLANK Value | 208 | VBLANK Value | 8 |
| VSYNC Mode | Line Mode | Line Clock Period(LCP) | 848 * 2 SCPs |
| Output Bus Width | 8bit | SIF Video Output Frequency | SCF * 1 = 10Mhz |
| Final Video Output Size | 320x240 | | |

In 1/4 subsampling mode, valid video data is produced every other line, i.e. for 480 LCPs, active video lines are 240. HSYNC active time is equal to HSYNC active time of 3x3 color interpolation mode, but video clock frequency is half of 3x3 color interpolation mode's to produce half size output in horizontal direction.



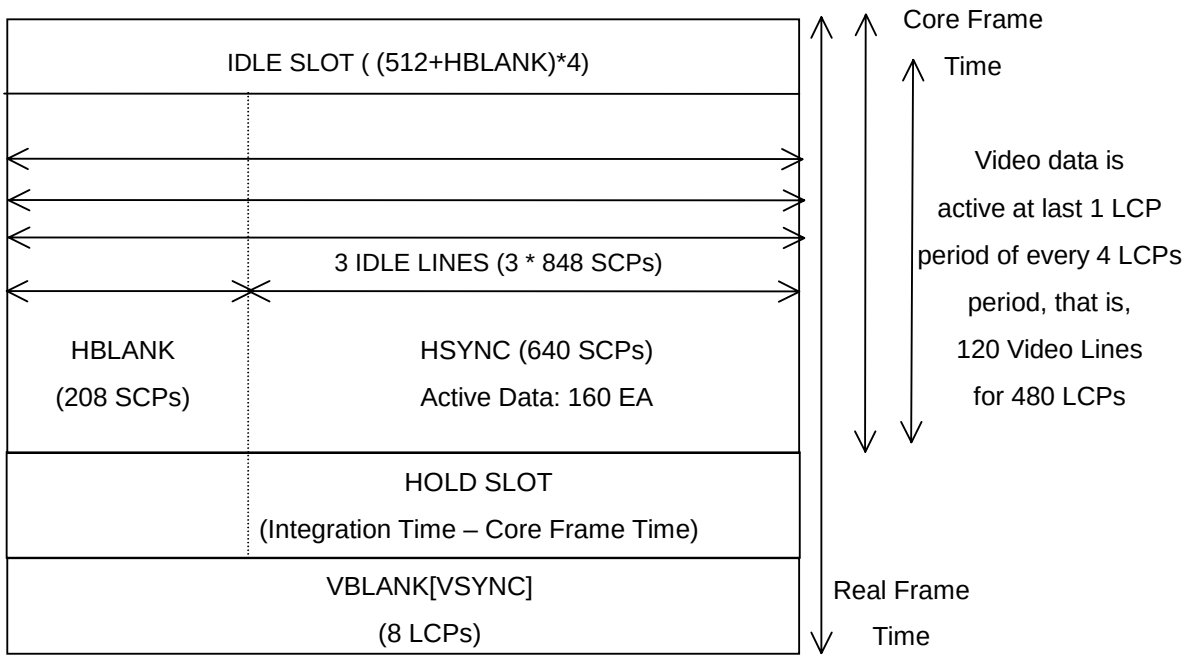



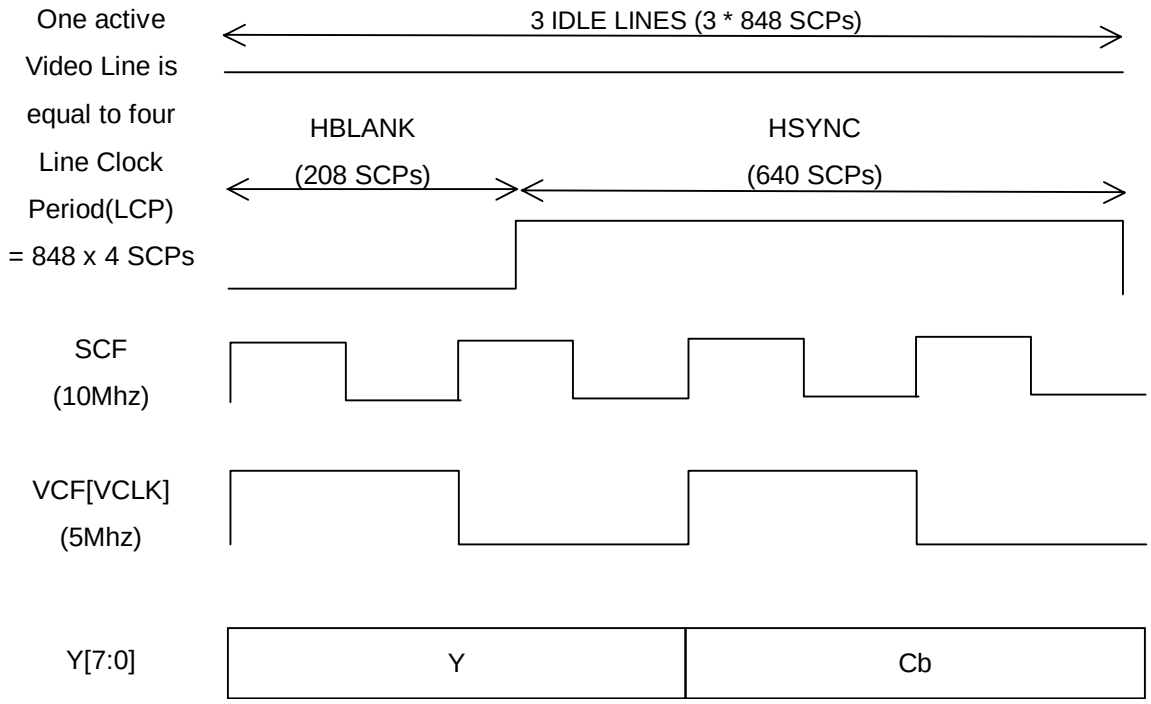

**3. 1/16 Subsampling Timing**

| 1/16 Subsampling Frame Timing Related Parameters | | | |
|---|---|---|---|
| Master Clock Frequency(MCF) | 20Mhz | Divided Clock Frequency(DCF) | MCF/1 = 20Mhz |
| Sensor Clock Frequency(SCF) | DCF/2 = 10Mhz | Sensor Clock Period(SCP) | 1/10Mhz = 100ns |

| | | | |
|---|---|---|---|
| Window Width | 640 | Window Height | 480 |
| HBLANK Value | 208 | VBLANK Value | 8 |
| VSYNC Mode | Line Mode | Line Clock Period(LCP) | 848 * 4 SCPs |
| Output Bus Width | 8bit | QSIF Video Output Frequency | SCF / 2 = 5Mhz |
| Final Video Output Size | 160x120 | | |

In 1/16 subsampling mode, valid video data is produced every four line, i.e. for 480 LCPs, active video lines are 120. HSYNC active time is equal to HSYNC active time of 3x3 color interpolation mode, but video clock frequency is a quarter of 3x3 color interpolation mode's to produce a quarter size output in horizontal direction.





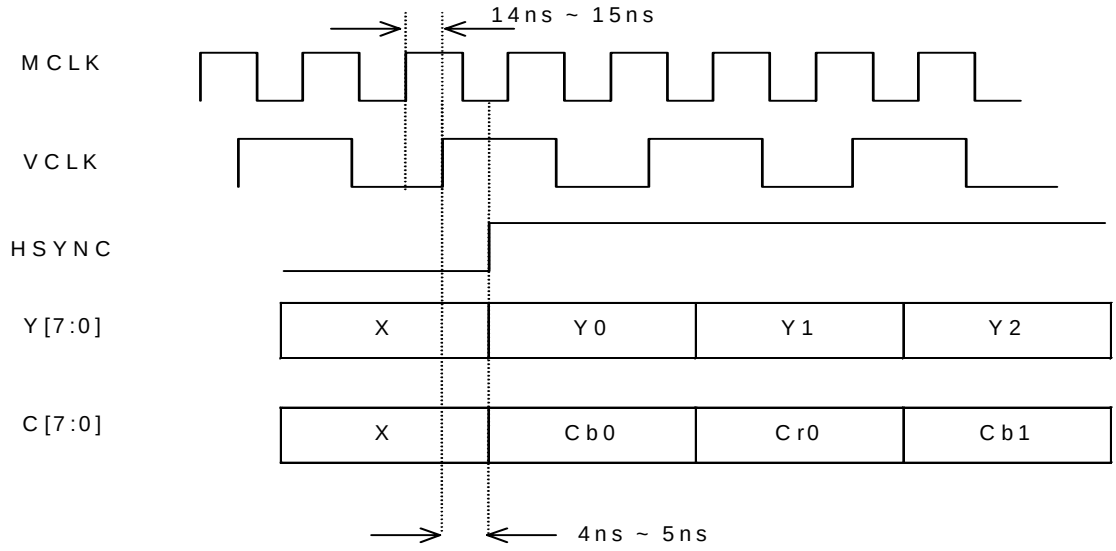

## Anti-Banding Configuration

For Anti-Banding mode to work correctly, the following registers should be configured to the appropriate values.

| | | |
|---|---|---|
| AE Mode | 60h | Anti-Banding Enable[7] |
| AE Anti-Banding Step | 6a-6ch | SCF / (2 x power line frequency) |
| AE Integration Time Limit | 6d-6fh | The value should be multiples of AE Anti-Banding Step |

When Anti-Banding is enabled, AE initializes Integration Time registers[63-65h] to 4 x Anti-Banding Step value[6a-6ch], and integration increment/decrement amount is set to Anti-Banding Step value in order to remove anti-banding noise caused by intrinsic energy waveform of light sources. Banding noise is inherent in CMOS image sensor that adopts rolling shutter scheme for image acquisition.

## Data Output Timing and Interface




As specified in the above data output timing diagram, the timing margin between video clock pin (VCLK) and data pins (Y[7:0] or C[7:0]) is about 4ns ~ 5ns. This margin may be sufficient or not according to how much video clock and data pins are delayed internally in the backend chip, respectively. To safely latch the data output in the backend chip, it is recommended that data be latched at negative edge of VCLK. The above timing margin diagram represents 16bit output interface, but is also valid for 8bit output interface.

## Output Data Format

Output Format is controlled by configuring Output Format register[31h]. Configurable options are specified again for your reference.

**Output Format [OUTFMT : 31h : 39h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| reserved | reserved | Cb First | Y First | 8 Bit Output | reserved | YCbCr 4:4:4 | YCbCr 4:2:2 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

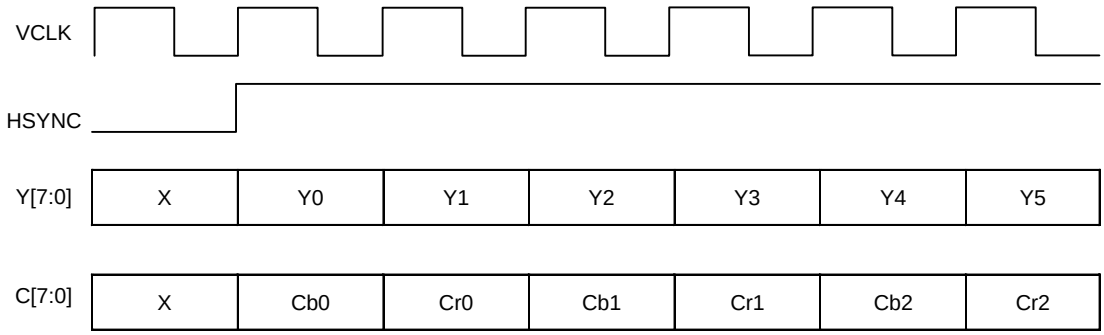
| | |
|---|---|
| Cb First | Cb pixel in front of Cr pixel in 16bit or 8bit video data output modes |
| Y First | Y pixel in front of Cb and Cr pixels in 8bit video output mode. This option is meaningful only with 8bit output mode. |
| 8 Bit Output | Image Data is produced only in Y[7:0]. C[7:0] should be discarded |

| | |
|---|---|
| YCbCr 4:4:4 | YCbCr 24bit data for a pixel is produced with 16bit output mode. With color space conversion disabled, RGB 24bit data for a pixel is produced in this mode. This mode is meaningful only with 16bit output mode. |
| YCbCr 4:2:2 | YCbCr data for a pixel is produced with 8/16 output mode |

Output timings for general configurations are described below. Slot named as “X” means that it is has no meaningful value and should be discarded.

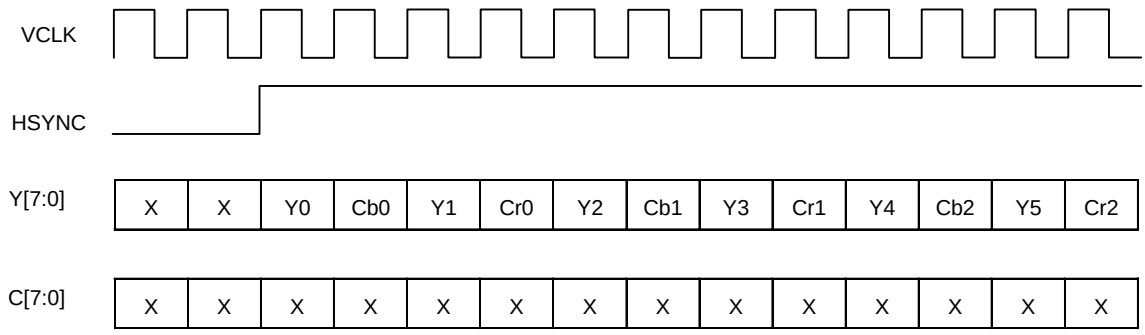
1. YCbCr 4:2:2 with 16bit output

Register bit configurations: 16bit output, Cb First, YCbCr 4:2:2



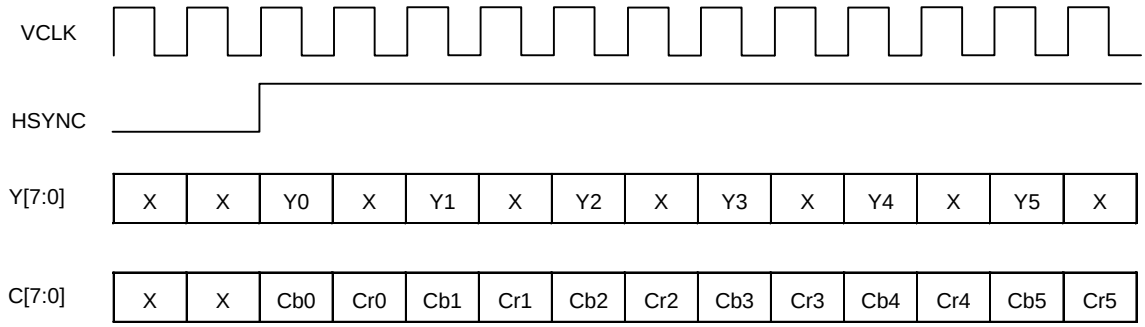

2. YCbCr 4:2:2 with 8bit output

Register bit configurations: 8bit output, Y First, Cb First, YCbCr 4:2:2



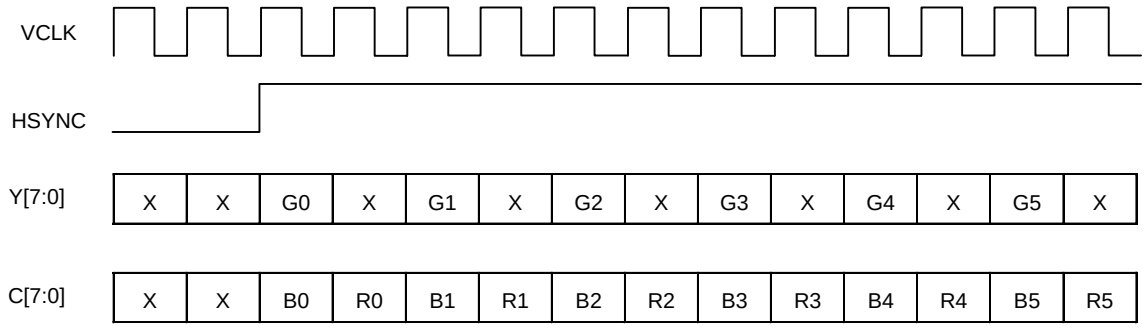

3. 24bit YCbCr 4:4:4 output

Register bit configurations : 8bit output, Y First, Cb First, YCbCr 4:4:4, and color space conversion enabled




4. 24bit RGB 4:4:4 output

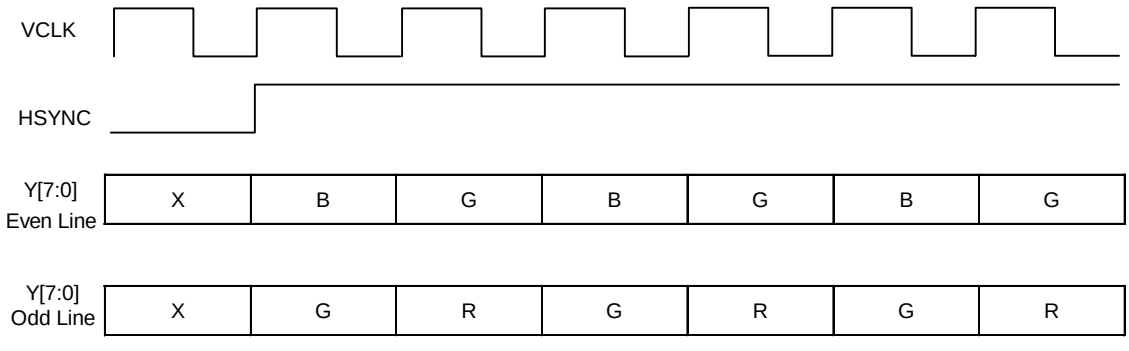
Register bit configurations : 8bit output, Y First, Cb First, YCbCr 4:4:4, and color space conversion disabled




## Bayer Data Format

SCTRA[1:0] is set to Bayer mode

- When Bayer output mode is selected, Window Width x Window Height raw image data are produced with the following sequence. After VSYNC goes low state, the first HSYNC line of a frame is activated with B pixel data appearing first when both of Column Start Address and Row Start Address are even.



# I2C Chip Interface

## Register Write Sequences

### One Byte Write

| S | 22H | A | 01H | A | 03H | A | P |
|---|---|---|---|---|---|---|---|
| *1 | *2 | *3 | *4 | *5 | *6 | *7 | *8 |

Set "Sensor Control A" register into Window mode

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 01H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 03H [Video Mode : CIF

*7. Read: acknowledge from sensor

*8. Drive: I2C stop condition

### Multiple Byte Write using Auto Address Increment

| S | 22H | A | 6aH | A | 51H | A | 61H | A | P |
|---|---|---|---|---|---|---|---|---|---|
| *1 | *2 | *3 | *4 | *5 | *6 | *7 | *8 | *9 | *10 |

Set "AE Integration Step High/Low" register as 5161H with auto address increment

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 6aH [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 51H [AE Integration Step High]

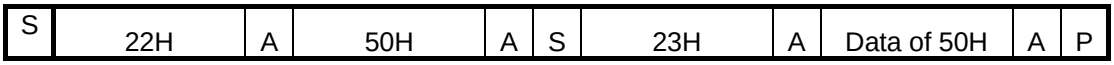
*7. Read: acknowledge from sensor

*8. Drive: 61H [AE Integration Step Low]

*9. Read: acknowledge from sensor

*10. Drive: I2C stop condition

### Register Read Sequence




Read "Reset Level Control" register from HV7131GP

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit(be careful. R/W=0)]

*3. Read: acknowledge from sensor

*4. Drive: 50H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: $I^2C$ start condition

*7. Drive: 23H(001_0001 + 1) [device address + R/W bit(be careful. R/W=1)]

*8. Read: acknowledge from sensor

*9. Read: Read “Reset Level Control Value” from sensor

*10. Drive: acknowledge to sensor. If there is more data bytes to read, SDA should be driven to low and data read states(*9, *10) is repeated. Otherwise SDA should be driven to high to prepare for the read transaction end.

*11. Drive: I2C stop condition

## AC/DC Characteristics

### Absolute Maximum Ratings

| Symbol | Parameter | Units | Min. | Max. |
|---|---|---|---|---|
| Vdpp | Digital supply voltage | Volts | -0.3 | 7.0 |
| Vapp | Analog supply voltage | Volts | -0.3 | 7.0 |
| Vipp | Input signal voltage | Volts | -0.3 | 7.0 |
| Top | Operating Temperature | °C | -30 | 70 |
| Tst | Storage Temperature | °C | -40 | 85 |

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

## DC Characteristic

| Symbol | Parameter | Units | Min. | Typical. | Max. | Conditions&Note |
|---|---|---|---|---|---|---|
| $V_{dd}$ | Internal operation supply voltage | Volt | 2.6 | - | 3.0 | - |
| $I_{dd}$ | Operating current consumption | mA | | - | 40 | At 15fps(12.5Mhz) |
| $HsI_{dd}$ | Hard Sleep Static current consumption | uA | | - | 48 | At 15fps(12.5Mhz) |
| $SsI_{dd}$ | Soft Sleep Static current consumption | uA | - | - | 276 | At 15fps(12.5Mhz) |
| $V_{ih}$ | Input voltage logic "1" | Volt | 2.0 | - | 3.0 | - |
| $V_{il}$ | Input voltage logic "0" | Volt | 0 | - | 0.8 | - |
| $V_{oh}$ | Output voltage logic "1" | Volt | 2 | - | - | at Ioh = -4mA |
| $V_{ol}$ | Output voltage logic "0" | Volt | - | - | 0.4 | at Iol = 4mA |
| Iih | Input High Current | uA | -10 | - | 10 | - |
| Iil | Input Low Current | uA | -10 | - | 10 | - |
| $T_a$ | Ambient operating temperature | Celsius | -10 | - | 50 | - |
| Cin | Input capacitance | pF | 5 | - | - | - |
| Cout | Output capacitance | pF | - | - | 30 | - |
| Cbid | Bi-directional buffer capacitance | pF | - | - | 30 | - |
| $R_{Epud}$ | External pull-up / pull-down resistance | Ohm | - | - | 20k | 1) |

Note.1) R Epud is just applied to SDA and SCK pin. And If R Epud is less than 20K Ohm, power consumption is increased.

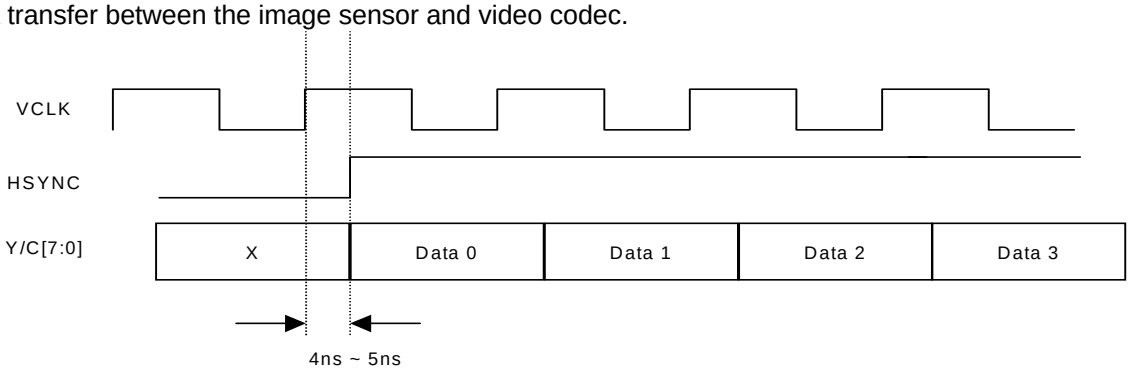
## AC Operating Conditions

| Symbol | Parameter | Max Operation Frequency | Units | Notes |
|---|---|---|---|---|
| MCLK | Main clock frequency | 25 | MHz | 1,2 |
| SCK | $I^2C$ clock frequency | 400 | KHz | 3 |

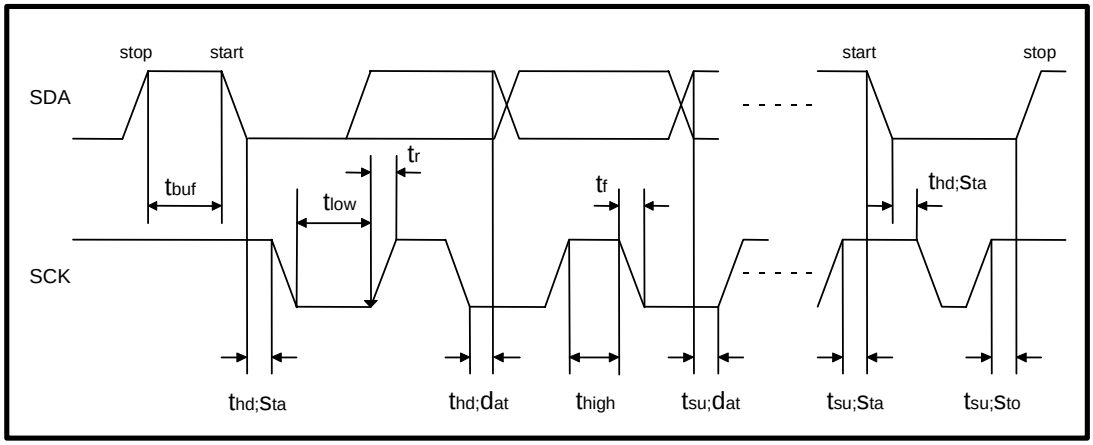
1. MCLK may be divided by internal clock division logic for easy integration with high speed video codec system.
2. Frame Rate : 30 frames/sec at 25Mhz, HBLANK = 208, VBLANK = 8
3. SCK is driven by host processor. For the detail serial bus timing, refer to I2C chip interface section

## Output AC Characteristics

All output timing delays are measured with output load 60[pF]. Output delay includes the internal clock path delay and output driving delay that changes in respect to the output load, the operating environment, and a board design. Due to the variable valid time delay of the output, video output signals Y[7:0], C[7:0], HSYNC, and VSYNC may be latched in the negative edge of VCLK for the stable data transfer between the image sensor and video codec.



## I2C Bus Timing




| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| SCK clock frequency | $f_{sck}$ | 0 | 400 | KHz |
| Time that $I^2C$ bus must be free before a new transmission can start | $t_{buf}$ | 1.2 | - | us |
| Hold time for a START | $t_{hd;sta}$ | 1.0 | - | us |
| LOW period of SCK | $t_{low}$ | 1.2 | - | us |
| HIGH period of SCK | $t_{high}$ | 1.0 | - | us |
| Setup time for START | $t_{su;sta}$ | 1.05 | - | us |
| Data hold time | $t_{hd;dat}$ | 0.1 | - | us |
| Data setup time | $t_{su;dat}$ | 250 | - | ns |
| Rise time of both SDA and SCK | $t_r$ | - | 250 | ns |
| Fall time of both SDA and SCK | $t_f$ | - | 300 | ns |
| Setup time for STOP | $t_{su;sto}$ | 1.05 | - | us |
| Capacitive load of SCK/SDA | $C_b$ | - | 30 | pf |

## Electro-Optical Characteristics

| Parameter | Units | Min. | Typical | Max. | Note |
|---|---|---|---|---|---|
| Sensitivity | mV / lux·sec | | 3000 | | Green Pixel |
| Dark Signal | mV | | 12 | | 1/10" , 60℃ |
| Output Saturation Signal | mV | | 1000 | | |

- Color temperature of light source: 3200K / IR cut-off filter (CM-500S, 1mm thickness) is used.

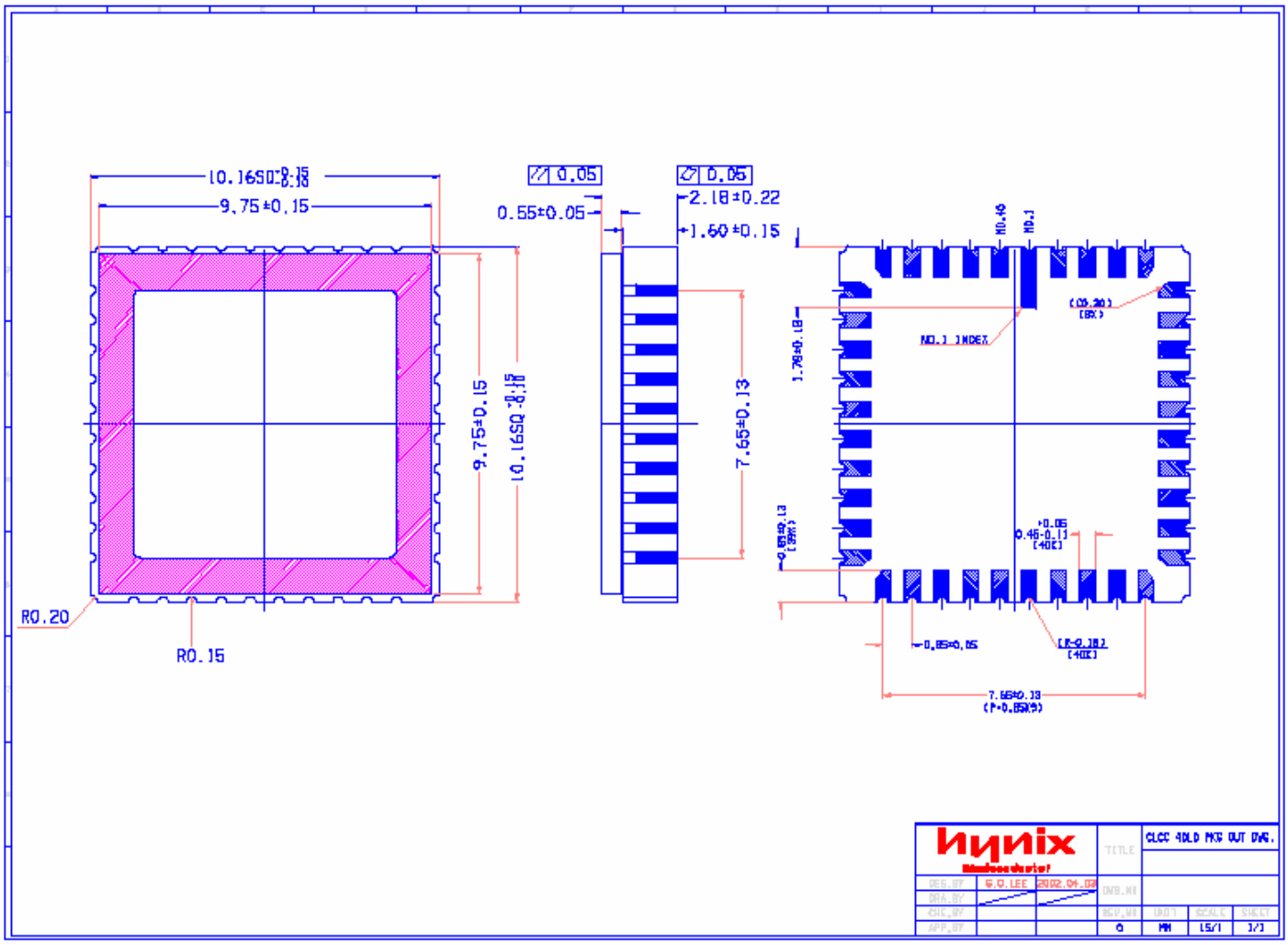
**Soldering**

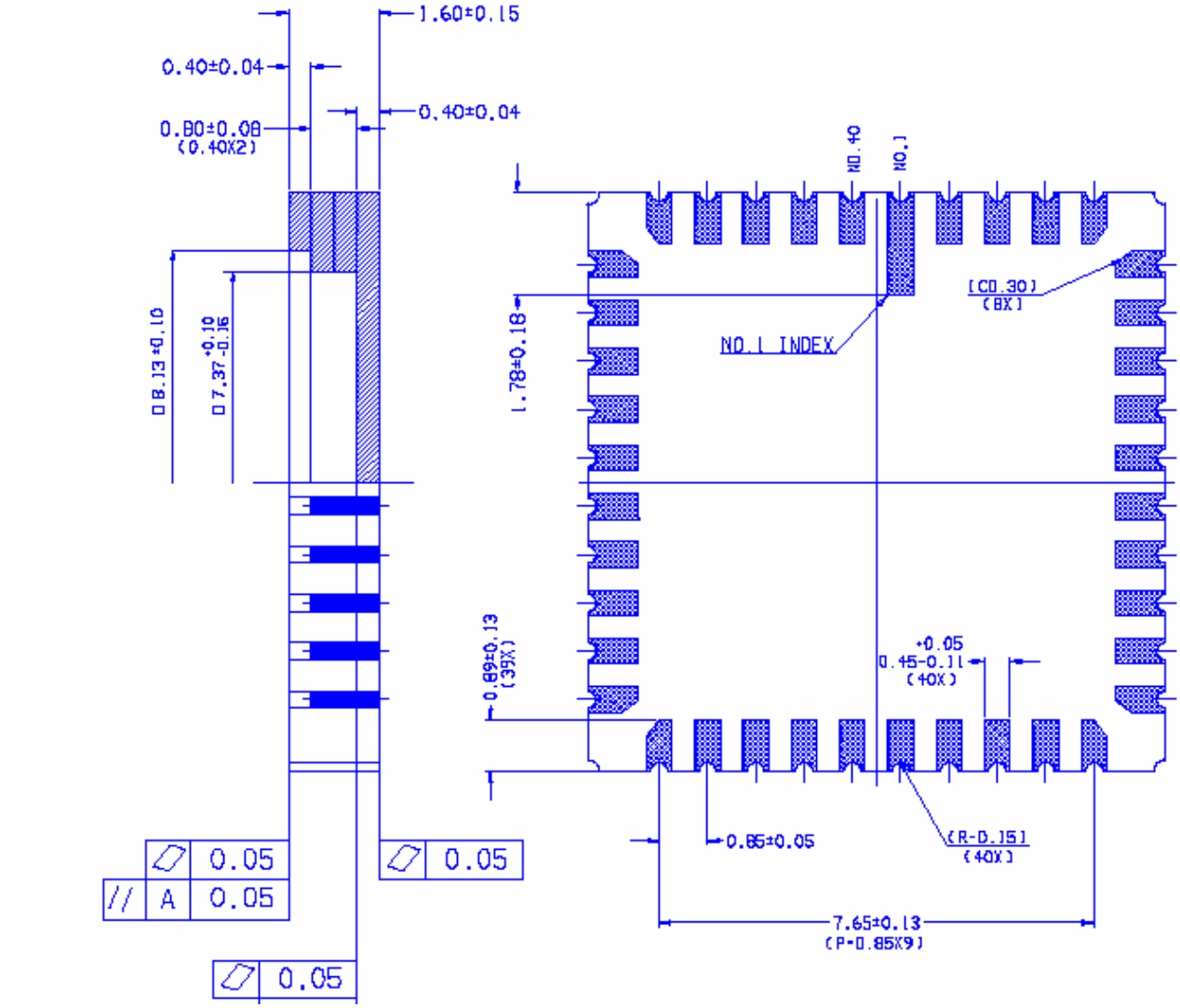
Infrared(IR) / Convection solder reflow condition

| Parameter | Units | Min. | Typical | Max. | Note |
|---|---|---|---|---|---|
| Peak Temperature Range | Celsius | - | 230 | 240 | 1) |

Note: 1) Time within 5 Celsius of actual peak temperature, 10sec

## CLCC Package Specification






* To the matter concerning package, Wafer business companies are unrelated contents.

# MagnaChip Semiconductor Ltd.

## * Contact Point *


### CIS Marketing Team

891 Daechi-dong Kangnam-Gu Seoul 135-738 Korea

Tel: 82-2-3459-5577

Fax: 82-2-3459-5580

E-mail : hanho1.lee@magnachip.com