HM10S801A

384CH TFT-LCD SOURCE DRIVER

PRELIMINARY

SPECIFICATION

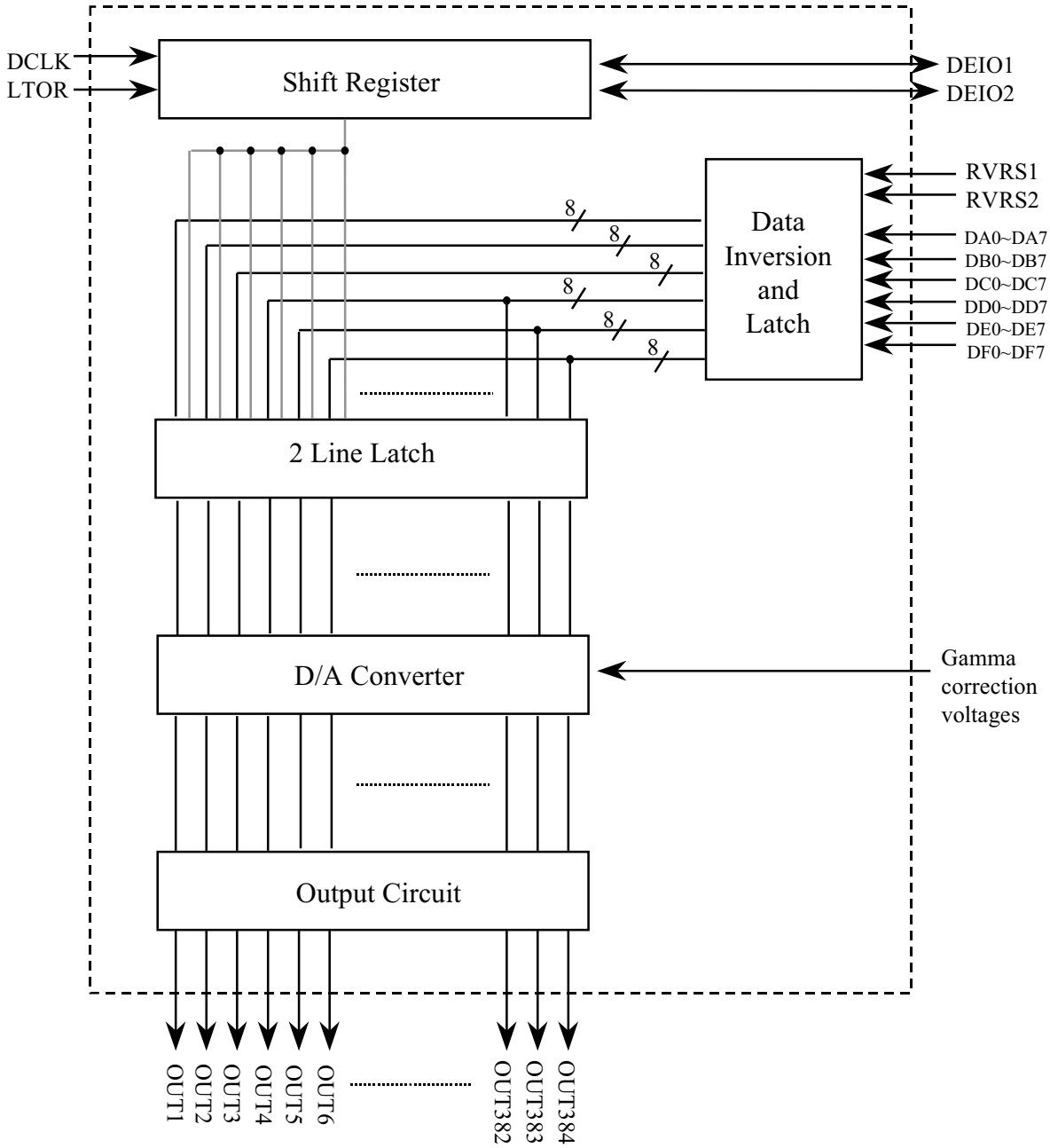
• Description

HM10S801A is a source driver for offering an ultra low power solution for pixel inversion LCD modules used in monitor or note PC applications. It accepts 8-bit × 6 dot digital data and provides direct drive, 512 voltage, 384 output, and full 12.6Vp-p dynamic range to drive 16,777,216 color TFT displays.

• Features

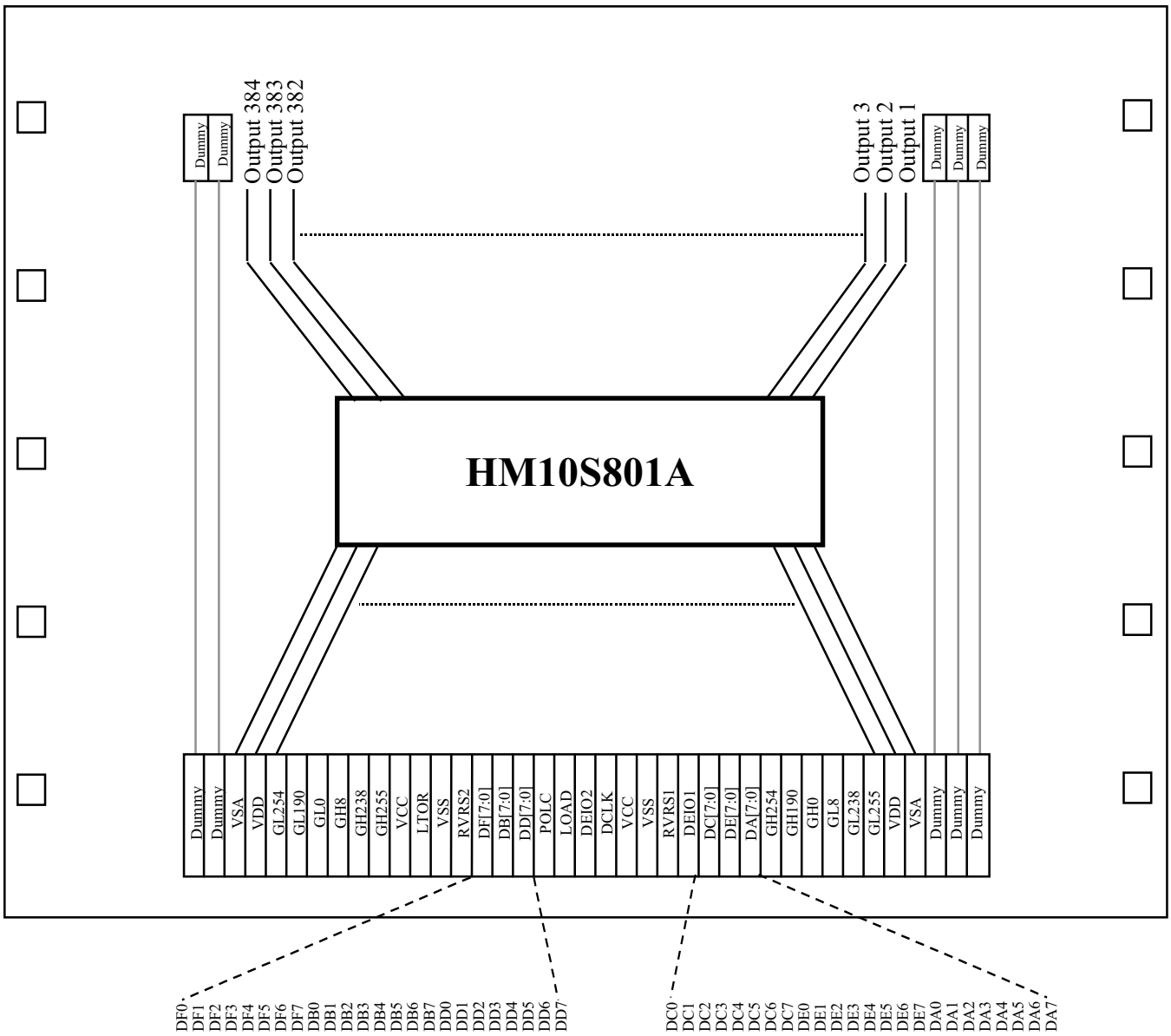
- Source driver LSI for active matrix LCD
- Ultra low power
  - ⇒ Low power driver amplifier
  - ⇒ Optimized for pixel inversion
- The number of LCD driving output is 384 Channel
- 512 Distinct voltages per output
  - ⇒ 256 Gray shade high colors on TFT_LCD
  - ⇒ 16,777,216 on TFT displays
- 12.6V Output dynamic range
- High speed data latch
  - ⇒ Up to 37.5Mhz Operation
  - ⇒ Supports 3.3V Data bus
  - ⇒ Dual ports : 6 Data busses
- High speed output drive
  - ⇒ Fast output transitions
  - ⇒ Transition time independent of other outputs
- Slim and fine pitch TCP (Tape Carrier Package)
- Adoption of LTOR port for easy LCD wiring

• **Block Diagram**



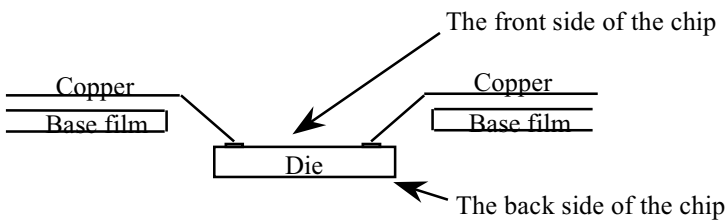
[Fig 1] Block diagram of HM10S801A

• TCP Pin Configuration



[Fig 2] TCP pin assignment of HM10S801A

NOTICE : This is seen from the front side of the TCP.
Inner lead bonding direction is Face Up as shown below.
The number of dummy pads could be changed according to the situation.



• Pin Description

<table>
<tr><th>PIN NAME</th><th>INPUT / OUTPUT</th><th>FUNCTION</th></tr>
<tr><td>DA[7:0]
DB[7:0]
DC[7:0]
DD[7:0]
DE[7:0]
DF[7:0]</td><td>Input</td><td>R,G,B 8bit digital video signals
Dx0 : LSB, Dx7 : MSB
Data inputs which select one of 256 reference voltages</td></tr>
<tr><td>DEIO1
DEIO2</td><td>Input / Output</td><td>Data latch enable.
Start pulse input port of internal shift register
<table>
<tr><th></th><th>LTOR = 1</th><th>LTOR = 0</th></tr>
<tr><td>DEIO1</td><td>Right shift input</td><td>Left shift output</td></tr>
<tr><td>DEIO2</td><td>Right shift output</td><td>Left shift input</td></tr>
</table>
[Table 1] Relation between LTOR and DEIOx</td></tr>
<tr><td>LTOR</td><td>Input</td><td>Shift direction pin (up/down select)
If LTOR = 1, then Right shift : Output 1 → Output 384
= 0, then Left shift : Output 384 → Output 1</td></tr>
<tr><td>DCLK</td><td>Input</td><td>Data clock pin
Data(Dx[7:0]), POLC, DEIOx input are latched on the rising edge of this clock.</td></tr>
<tr><td>VDD
VCC
VSA
VSS</td><td>Input</td><td>Analog block voltage source : typically 12 Volts above VSA.
Digital block voltage source : typically 3.3Volts above VSS.
Analog block reference voltage, typically 0.0Volts.
Digital block reference voltage, typically 0.0Volts.</td></tr>
<tr><td>Gxx</td><td>Input</td><td>High / Low voltage reference for the D/A converter
GH0 : The lowest voltage in high voltage region
GL0 : The highest voltage in low voltage region
GH255 : The highest voltage in high voltage region
GL255 : The lowest voltage in low voltage region
GH8, GH190, GH238, GH254, GL8, GL190, GL238, GL254 :
Intermediate D/A voltage references</td></tr>
<tr><td>LOAD</td><td>Input</td><td>Data transfer pin
After ‘tpdDZ’ from rising edge of this input, the latched Data will be transferred to buffers and drove to the outputs the previously acquired analog voltages.(see page 22)</td></tr>
</table>

<table>
<tr><th>PIN NAME</th><th>INPUT / OUTPUT</th><th>FUNCTION</th></tr>
<tr><td>POLC</td><td>Input</td><td>Polarity control pin.
This input pin is set to a digital high or a digital low state and will select the output polarity as shown below.

<table><tr><th>POLC</th><th>OUT $_{2N-1}$</th><th>OUT $_{2N}$</th></tr><tr><td>L</td><td>GH0 to GH255</td><td>GL0 to GL255</td></tr><tr><td>H</td><td>GL0 to GL255</td><td>GH0 to GH255</td></tr></table>OUT $_{2N-1}$: Odd number outputs
OUT $_{2N}$: Even number outputs
[Table 2] Relation between LTOR and DEIOx

The sampling of this pin begins with the rising edge of the DCLK when LOAD signal is HIGH.</td></tr>
<tr><td>RVRS1
RVRS2</td><td>Input</td><td>This pin is used to internally reverse the data busses whenever it is pulled to a logic high state. This results in reversed output gamma curves.

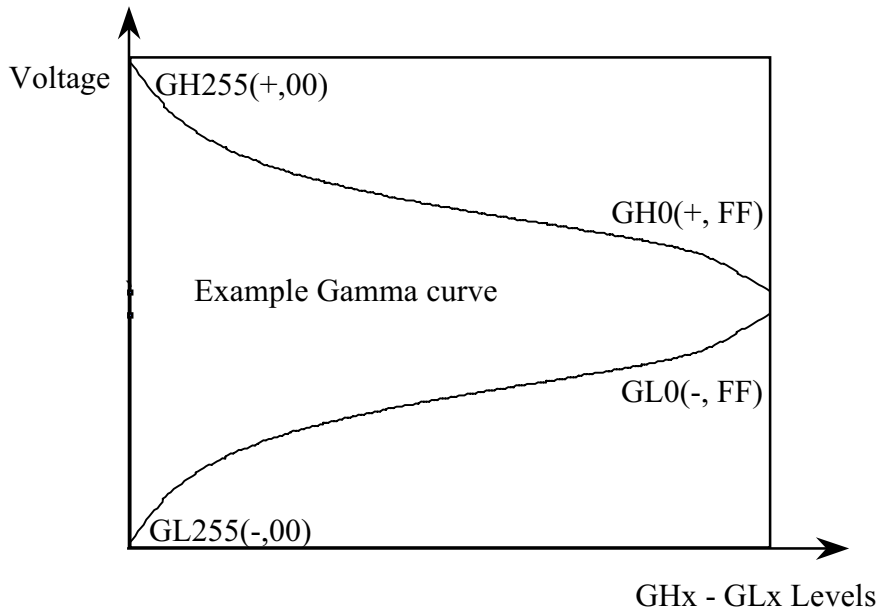
when RVRS1, 2 = High : data is inverted
when RVRS1, 2 = Low : data is not inverted

Data Bus (DA, DB, DC) XOR RVRS1 = Data used in D/A
Data Bus (DD, DE, DF) XOR RVRS2 = Data used in D/A</td></tr>
</table>

• Device Description

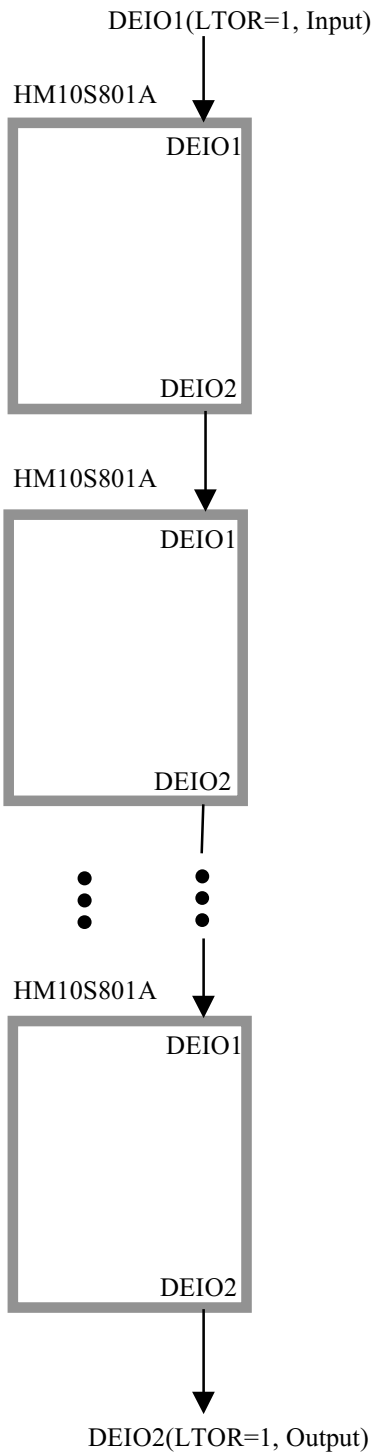
1) Operation description

HM10S801A device provides a full dynamic range of 12.6V from 13V supplies on 384 outputs. Full range output drive allows direct drive of TFT LCD displays, eliminating the need for Vcom or supply modulation electronics. This feature significantly reduces power consumption and component count.
In addition, the HM10S801A permits very low power consumption for panels using pixel inversion. Outputs are supported with individual high drive, high slew, operational amplifier style buffers. A 37.5MHz internal bi-directional shift registers allow use in single bank full motion video. A total of 512 voltages can be output for an active matrix display with variable increments between each voltage as shown below.



[Fig 3] Waveforms illustrating relationship between input data(Polarity, Dx[7:0])

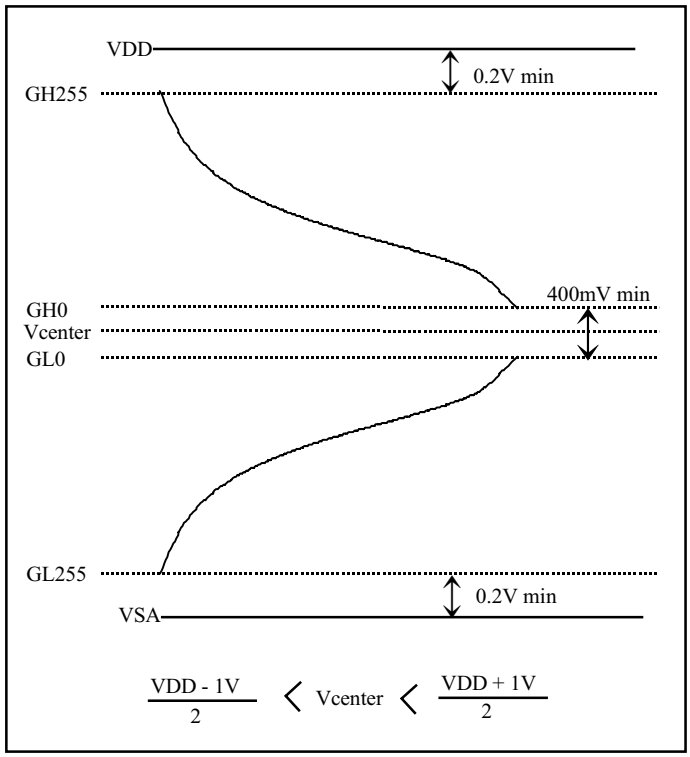
Digital data inputs to the chip are used to select one of the 512 voltages for driving an individual output. To implement variations of the existing characteristic curve, 12 external D/A voltage taps, six in the lower region and six in the higher region, are provided to allow the user to force voltages on several points in the D/A resistor string.



XGA system = 8 drivers

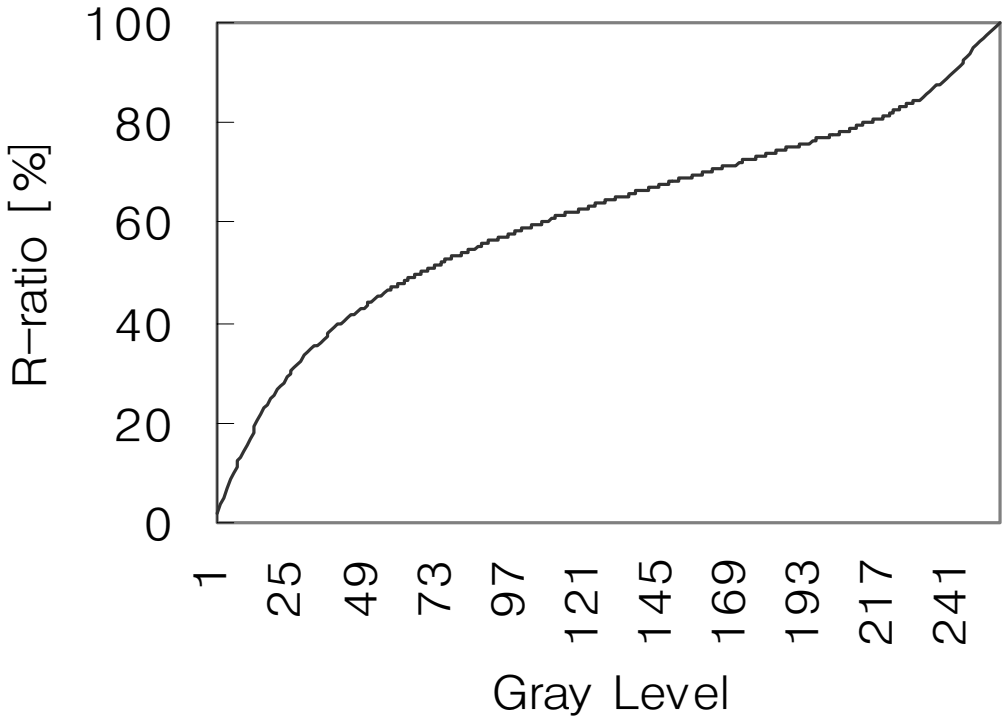
[Fig 4] Output driver control inputs

Output Range = VDD - 0.4V



[Fig 5] Reference voltage electrical characteristics

• **Characteristic Curve**



Notes :

1. Gamma correction curve is mirrored on the low voltage range extending from GL0 to GL255, ie.. the % voltage of full range is the same for GLx and GHx in the prototype. This does not have to be the case for a production device. Mask changes can be made to accommodate nearly any gamma curve for the upper and lower ranges individually.

• **R ratio for 256 gray**

DATAH	V node	VH	R (HIGH)	VL	R (LOW)
00H	255	9.400	0.000	0.200	
01H	254	9.354	170.318	0.246	139.429
02H	253	9.315	144.400	0.285	118.212
03H	252	9.276	144.400	0.324	118.212
04H	251	9.237	146.251	0.364	119.727
05H	250	9.197	146.251	0.403	119.727
06H	249	9.149	179.574	0.452	147.007
07H	248	9.100	179.574	0.500	147.007
08H	247	9.051	181.425	0.549	148.522
09H	246	9.002	181.425	0.598	148.522
0AH	245	8.956	172.169	0.645	140.945
0BH	244	8.909	172.169	0.691	140.945
0CH	243	8.866	159.210	0.734	130.336
0DH	242	8.823	159.210	0.777	130.336
0EH	241	8.783	148.102	0.817	121.243
0FH	240	8.743	148.102	0.857	121.243
10H	239	8.706	138.846	0.895	113.665
11H	238	8.668	138.846	0.932	113.665
12H	237	8.633	131.441	0.968	109.118
13H	236	8.597	131.441	1.004	109.118
14H	235	8.564	122.185	1.038	101.541
15H	234	8.531	122.185	1.071	101.541
16H	233	8.501	112.928	1.103	95.479
17H	232	8.470	112.928	1.134	95.479
18H	231	8.443	101.820	1.164	89.417
19H	230	8.415	101.820	1.193	89.417
1AH	229	8.390	94.415	1.220	81.839
1BH	228	8.364	94.415	1.247	81.839
1CH	227	8.341	85.159	1.272	75.777
1DH	226	8.318	85.159	1.297	75.777
1EH	225	8.296	81.456	1.321	72.746
1FH	224	8.274	81.456	1.345	72.746
20H	223	8.254	75.902	1.367	66.684
21H	222	8.233	75.902	1.389	66.684
22H	221	8.214	70.349	1.410	63.652
23H	220	8.195	70.349	1.431	63.652
24H	219	8.178	64.795	1.451	59.106
25H	218	8.160	64.795	1.470	59.106
26H	217	8.144	61.092	1.489	56.075
27H	216	8.127	61.092	1.507	56.075
28H	215	8.111	61.092	1.525	54.559
29H	214	8.094	61.092	1.543	54.559
2AH	213	8.079	57.390	1.561	53.044
2BH	212	8.063	57.390	1.578	53.044
2CH	211	8.048	55.538	1.595	51.528
2DH	210	8.033	55.538	1.612	51.528
2EH	209	8.019	53.687	1.628	48.497
2FH	208	8.004	53.687	1.644	48.497
30H	207	7.990	53.687	1.660	48.497
31H	206	7.975	53.687	1.676	48.497
32H	205	7.962	49.985	1.692	46.982
33H	204	7.948	49.985	1.707	46.982
34H	203	7.935	48.133	1.722	43.950
35H	202	7.922	48.133	1.736	43.950
36H	201	7.910	44.431	1.751	43.950
37H	200	7.898	44.431	1.765	43.950
38H	199	7.886	44.431	1.779	40.919
39H	198	7.874	44.431	1.792	40.919
3AH	197	7.863	42.579	1.806	40.919
3BH	196	7.851	42.579	1.819	40.919
3CH	195	7.840	40.728	1.832	39.404
3DH	194	7.829	40.728	1.845	39.404
3EH	193	7.819	38.877	1.857	36.373
3FH	192	7.808	38.877	1.869	36.373
40H	191	7.798	38.877	1.882	37.888
41H	190	7.787	38.877	1.894	37.888
42H	189	7.777	37.026	1.906	34.857
43H	188	7.767	37.026	1.917	34.857
44H	187	7.758	35.174	1.929	34.857
45H	186	7.748	35.174	1.940	34.857
46H	185	7.739	35.174	1.951	33.342
47H	184	7.729	35.174	1.962	33.342
48H	183	7.720	33.323	1.973	33.342
49H	182	7.711	33.323	1.984	33.342
4AH	181	7.702	33.323	1.995	33.342
4BH	180	7.693	33.323	2.006	33.342

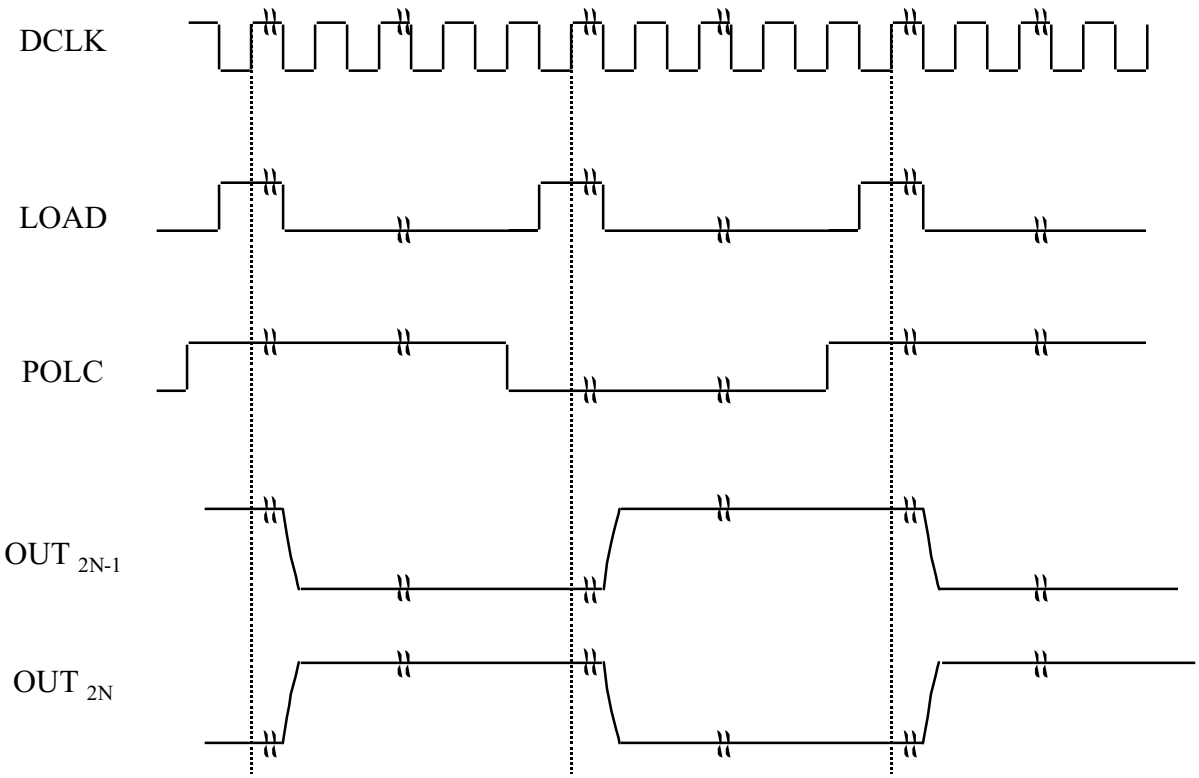
4CH	179	7.684	33.323	2.017	31.826
4DH	178	7.675	33.323	2.027	31.826
4EH	177	7.667	31.472	2.038	31.826
4FH	176	7.658	31.472	2.048	31.826
50H	175	7.650	29.620	2.058	30.311
51H	174	7.642	29.620	2.068	30.311
52H	173	7.634	31.472	2.078	30.311
53H	172	7.625	31.472	2.088	30.311
54H	171	7.617	29.620	2.098	30.311
55H	170	7.609	29.620	2.108	30.311
56H	169	7.602	27.769	2.118	28.795
57H	168	7.594	27.769	2.127	28.795
58H	167	7.586	29.620	2.137	28.795
59H	166	7.578	29.620	2.146	28.795
5AH	165	7.571	27.769	2.155	27.280
5BH	164	7.563	27.769	2.164	27.280
5CH	163	7.556	25.918	2.173	27.280
5DH	162	7.549	25.918	2.182	27.280
5EH	161	7.542	27.769	2.191	27.280
5FH	160	7.534	27.769	2.200	27.280
60H	159	7.527	25.918	2.209	27.280
61H	158	7.520	25.918	2.218	27.280
62H	157	7.513	25.918	2.227	25.764
63H	156	7.506	25.918	2.235	25.764
64H	155	7.500	24.067	2.244	27.280
65H	154	7.493	24.067	2.253	27.280
66H	153	7.486	25.918	2.261	24.249
67H	152	7.479	25.918	2.269	24.249
68H	151	7.473	24.067	2.278	25.764
69H	150	7.466	24.067	2.286	25.764
6AH	149	7.460	22.215	2.294	24.249
6BH	148	7.454	22.215	2.302	24.249
6CH	147	7.448	24.067	2.310	24.249
6DH	146	7.441	24.067	2.318	24.249
6EH	145	7.435	22.215	2.326	22.733
6FH	144	7.429	22.215	2.333	22.733
70H	143	7.423	22.215	2.341	24.249
71H	142	7.417	22.215	2.349	24.249
72H	141	7.411	22.215	2.357	22.733
73H	140	7.405	22.215	2.364	22.733
74H	139	7.399	22.215	2.372	22.733
75H	138	7.393	22.215	2.379	22.733
76H	137	7.387	22.215	2.387	22.733
77H	136	7.381	22.215	2.394	22.733
78H	135	7.376	20.364	2.402	22.733
79H	134	7.370	20.364	2.409	22.733
7AH	133	7.364	22.215	2.417	22.733
7BH	132	7.358	22.215	2.424	22.733
7CH	131	7.353	20.364	2.432	22.733
7DH	130	7.347	20.364	2.439	22.733
7EH	129	7.342	20.364	2.447	22.733
7FH	128	7.336	20.364	2.454	22.733
80H	127	7.330	22.215	2.461	21.217
81H	126	7.324	22.215	2.468	21.217
82H	125	7.319	20.364	2.476	22.733
83H	124	7.313	20.364	2.483	22.733
84H	123	7.308	20.364	2.491	22.733
85H	122	7.302	20.364	2.498	22.733
86H	121	7.297	20.364	2.505	21.217
87H	120	7.291	20.364	2.512	21.217
88H	119	7.286	18.513	2.520	22.733
89H	118	7.281	18.513	2.527	22.733
8AH	117	7.276	20.364	2.534	21.217
8BH	116	7.270	20.364	2.541	21.217
8CH	115	7.265	20.364	2.549	22.733
8DH	114	7.259	20.364	2.556	22.733
8EH	113	7.254	18.513	2.563	21.217
8FH	112	7.249	18.513	2.570	21.217
90H	111	7.244	20.364	2.577	21.217
91H	110	7.238	20.364	2.584	21.217
92H	109	7.233	18.513	2.592	22.733
93H	108	7.228	18.513	2.599	22.733
94H	107	7.223	20.364	2.606	21.217
95H	106	7.217	20.364	2.613	21.217
96H	105	7.212	18.513	2.620	21.217
97H	104	7.207	18.513	2.627	21.217
98H	103	7.202	18.513	2.634	21.217

99H	102	7.197	18.513	2.641	21.217
9AH	101	7.192	18.513	2.648	21.217
9BH	100	7.187	18.513	2.655	21.217
9CH	99	7.182	20.364	2.663	22.733
9DH	98	7.176	20.364	2.670	22.733
9EH	97	7.171	18.513	2.677	21.217
9FH	96	7.166	18.513	2.684	21.217
A0H	95	7.161	18.513	2.691	21.217
A1H	94	7.156	18.513	2.698	21.217
A2H	93	7.151	18.513	2.705	21.217
A3H	92	7.146	18.513	2.712	21.217
A4H	91	7.141	18.513	2.720	22.733
A5H	90	7.136	18.513	2.727	22.733
A6H	89	7.131	18.513	2.734	21.217
A7H	88	7.126	18.513	2.741	21.217
A8H	87	7.121	18.513	2.749	22.733
A9H	86	7.116	18.513	2.756	22.733
AAH	85	7.111	18.513	2.763	21.217
ABH	84	7.106	18.513	2.770	21.217
ACH	83	7.101	18.513	2.778	22.733
ADH	82	7.096	18.513	2.785	22.733
AEH	81	7.091	18.513	2.792	21.217
AFH	80	7.086	18.513	2.799	21.217
B0H	79	7.081	18.513	2.807	22.733
B1H	78	7.076	18.513	2.814	22.733
B2H	77	7.071	18.513	2.822	22.733
B3H	76	7.066	18.513	2.829	22.733
B4H	75	7.061	18.513	2.837	22.733
B5H	74	7.056	18.513	2.844	22.733
B6H	73	7.051	20.364	2.852	22.733
B7H	72	7.045	20.364	2.859	22.733
B8H	71	7.040	18.513	2.867	22.733
B9H	70	7.035	18.513	2.874	22.733
BAH	69	7.030	18.513	2.882	22.733
BBH	68	7.025	18.513	2.889	22.733
BCH	67	7.020	18.513	2.897	24.249
BDH	66	7.015	18.513	2.905	24.249
BEH	65	7.010	20.364	2.913	24.249
BFH	64	7.004	20.364	2.921	24.249
C0H	63	6.999	18.513	2.929	24.249
C1H	62	6.994	18.513	2.937	24.249
C2H	61	6.989	20.364	2.945	24.249
C3H	60	6.983	20.364	2.953	24.249
C4H	59	6.978	20.364	2.961	24.249
C5H	58	6.972	20.364	2.969	24.249
C6H	57	6.967	20.364	2.978	25.764
C7H	56	6.961	20.364	2.986	25.764
C8H	55	6.956	20.364	2.995	25.764
C9H	54	6.950	20.364	3.003	25.764
CAH	53	6.945	20.364	3.012	27.280
CBH	52	6.939	20.364	3.021	27.280
CCH	51	6.933	22.215	3.030	27.280
CDH	50	6.927	22.215	3.039	27.280
CEH	49	6.922	20.364	3.048	27.280
CFH	48	6.916	20.364	3.057	27.280
D0H	47	6.910	22.215	3.066	27.280
D1H	46	6.904	22.215	3.075	27.280
D2H	45	6.898	22.215	3.085	30.311
D3H	44	6.892	22.215	3.095	30.311
D4H	43	6.886	24.067	3.105	28.795
D5H	42	6.879	24.067	3.114	28.795
D6H	41	6.873	24.067	3.125	31.826
D7H	40	6.866	24.067	3.135	31.826
D8H	39	6.860	24.067	3.146	31.826
D9H	38	6.853	24.067	3.156	31.826
DAH	37	6.846	25.918	3.167	31.826
DBH	36	6.839	25.918	3.177	31.826
DCH	35	6.832	25.918	3.189	34.857
DDH	34	6.825	25.918	3.200	34.857
DEH	33	6.818	25.918	3.212	34.857
DFH	32	6.811	25.918	3.223	34.857
E0H	31	6.803	29.620	3.236	37.888
E1H	30	6.795	29.620	3.248	37.888
E2H	29	6.788	27.769	3.261	37.888
E3H	28	6.780	27.769	3.273	37.888
E4H	27	6.772	31.472	3.287	40.919
E5H	26	6.763	31.472	3.300	40.919

E6H	25	6.754	33.323	3.314	42.435
E7H	24	6.745	33.323	3.328	42.435
E8H	23	6.736	33.323	3.343	45.466
E9H	22	6.727	33.323	3.358	45.466
EAH	21	6.717	37.026	3.374	46.982
EBH	20	6.707	37.026	3.389	46.982
ECH	19	6.697	38.877	3.406	50.013
EDH	18	6.686	38.877	3.422	50.013
EEH	17	6.675	42.579	3.440	54.559
EFH	16	6.663	42.579	3.458	54.559
F0H	15	6.651	46.282	3.479	62.137
F1H	14	6.638	46.282	3.499	62.137
F2H	13	6.623	55.538	3.522	69.715
F3H	12	6.608	55.538	3.545	69.715
F4H	11	6.592	61.092	3.571	77.292
F5H	10	6.575	61.092	3.596	77.292
F6H	9	6.555	74.051	3.626	90.932
F7H	8	6.535	74.051	3.656	90.932
F8H	7	6.510	94.415	3.694	113.665
F9H	6	6.484	94.415	3.731	113.665
FAH	5	6.447	136.995	3.783	157.616
FBH	4	6.410	136.995	3.835	157.616
FCH	3	6.361	181.425	3.902	201.566
FDH	2	6.312	181.425	3.968	201.566
FEH	1	6.236	283.246	4.064	289.467
FFH	0	6.159	283.246	4.159	289.467

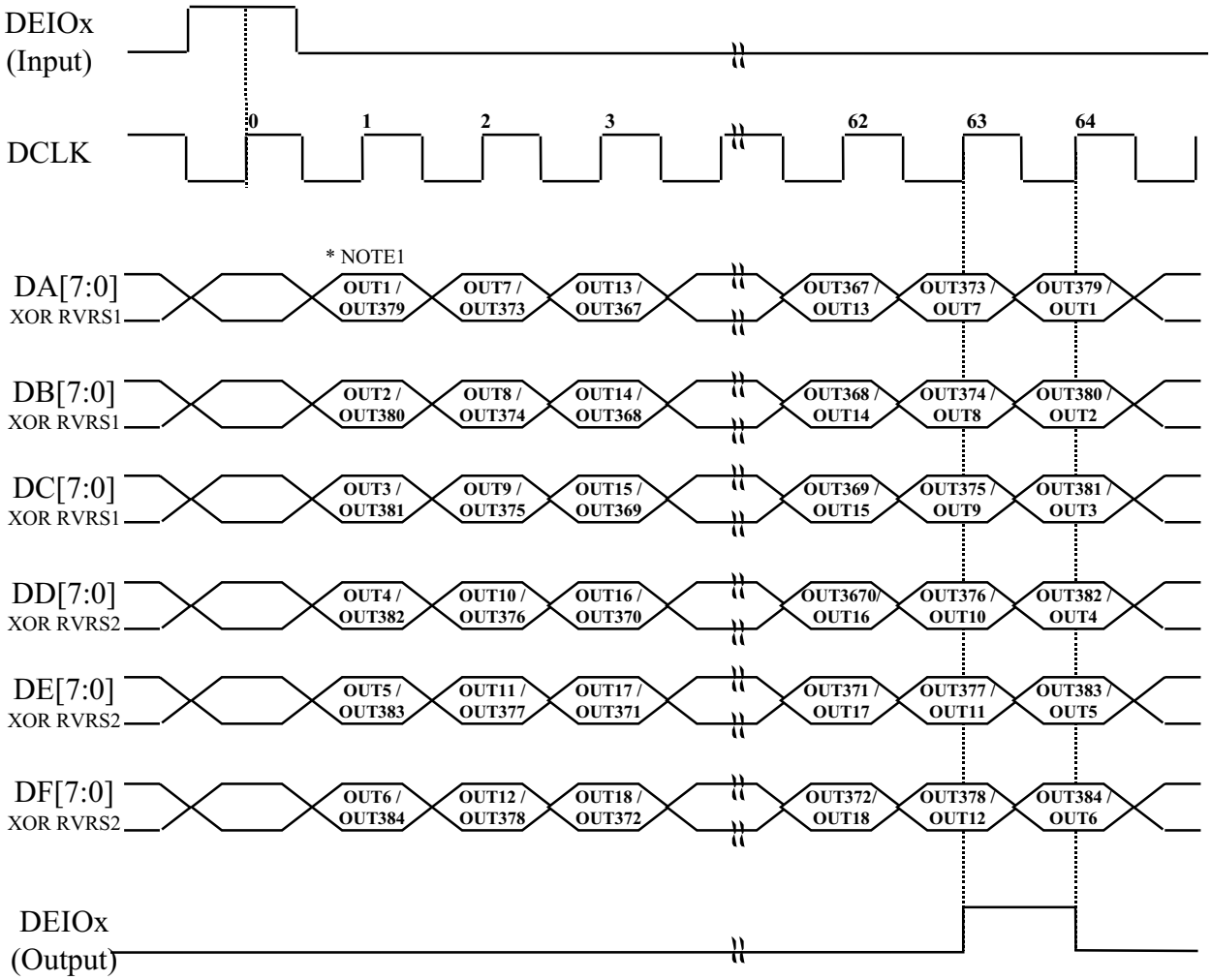
• **Timing Diagram 1**

- LOAD, POLC, and Output waveforms



• **Timing Diagram 2**

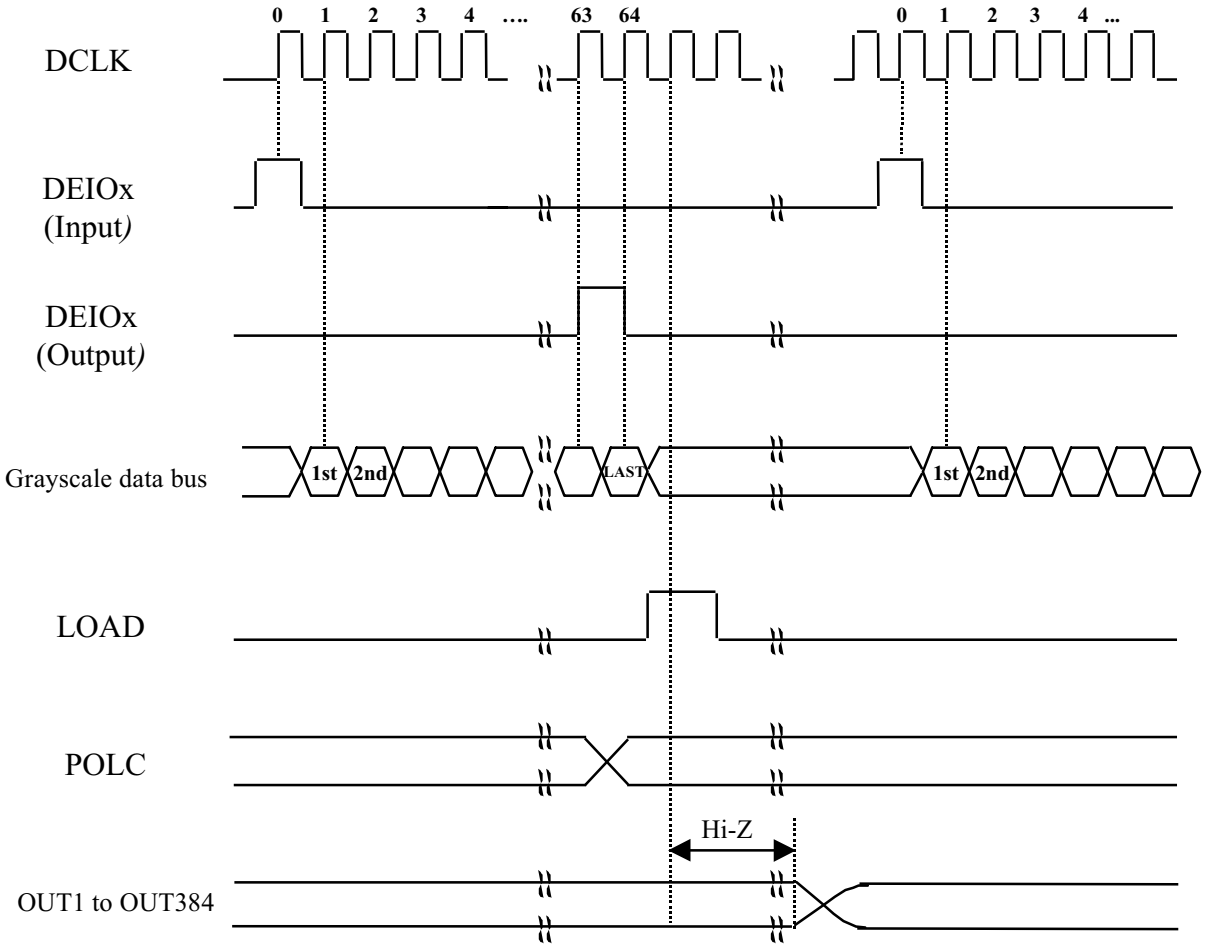
- DEIOx and Data latch sequence



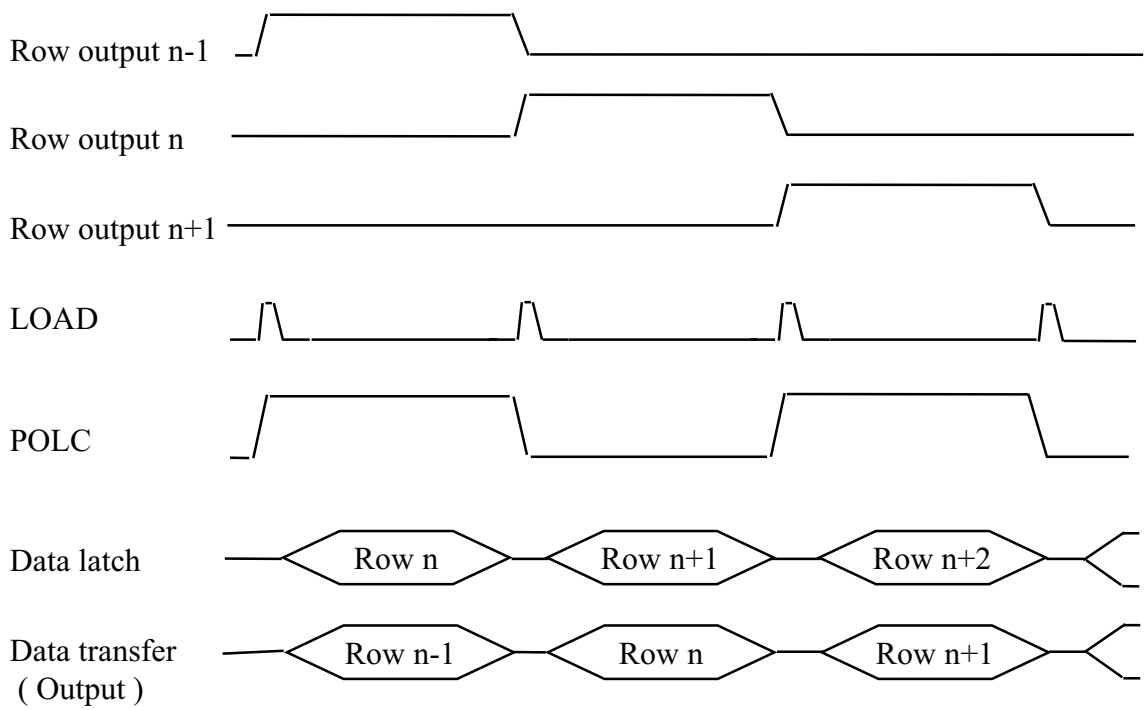
* NOTE1 : LTOR = 1, OUT1
LTOR = 0, OUT379

• Timing Diagram 3

- DEIOx and LOAD operations



• **Timing Diagram 4**



• HM10S801A Electrical Characteristics

1) Absolute Maximum Ratings

Parameter	Symbol	Limit	Units
Analog voltage supply range (Note 1)	VDD	-0.3 ~ +15	V
Digital voltage supply range (Note 1)	VCC	-0.3 ~ +6.0	V
GHxx(High range) (Note 1)		1/2VDD-1.0 ~ VDD+0.3	V
GLxx(Low range) (Note 1)		-0.3 ~ 1/2VDD+0.3	V
Input voltage(Digital logic)	Vin	-0.3 ~ VCC+0.3	V
Output voltage	Vout	-0.3 ~ VDD+0.3	V
Operating temperature	Top	-25 ~ +75	℃
Storage temperature	TSTR	-55 ~ +125	℃

[Table 1] Absolute Maximum Ratings

Notes : 1. Absolute voltage referenced to VSS = 0.0V ,VSA=0.0V.

Device operation above the parametric values listed may cause device damage.
Functional operation of the device at these or any other conditions beyond those listed in the ˝DC operating Condition˝section of this specification is not implied.

2) DC Operating Conditions

[Table 2] show electrical characteristics for typical operating conditions for the HM10S801A.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
3.3V Logic supply range	VCC	–	3.0	3.3	3.6	V
Input high voltage	VIH	–	0.7VCC	–	–	V
Input low voltage	VIL	–	–	–	0.3VCC	V
Output high voltage	VOH	IOH=0.5mA	2.8	–	–	V
Output low voltage	VOL	IOL=0.5mA	–	–	0.5	V
Logic current consumption (Note 1)	ICC 3.3V	–	–	1.1*	–	mA
Input leakage	IIH	VCC=3.6V VIN=3.6V	–	–	10	uA
Input leakage	IIL	VCC=3.6V VIN=0V	–	–	10	uA

[Table 5] Logic Section Electrical Characteristics

Note: 1. GH255=12.8V, GL255=0.2V, DCLK frequency=37.5MHz, VSA=0.0V, VDD=13V,
. Line time=20us.

* This value is the only simulation result.
The exact value will be modified after measuring values of silicon samples.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage range	VDD	–	11.0	12.0	13.0	V
Supply current consumption	IDD	VDD=13V	–	20/56*	–	mA
Power dissipation (Note 1)	PWD	–	–	260/730*	–	mW
Output voltage range	VOUT	VDD=13V	0.2	-	12.8	V
Output current	IOUT	–	–	2.0*	–	mA
Output absolute error (Note 2)	Verr	Vout,exp - Vout,meas	–	5	–	mV

[Table 3] Output drivers electrical characteristics

Notes :

Power On sequence : VCC -> Input signals -> VDD -> GHxx,GLxx.
Power Off sequence : GHxx, GLxx -> VDD -> Input signals -> VCC.

1. Power dissipation configuration : GH255=12.8V, GL255=0.2V, DCLK frequency= 37.5MHz, VSS=0.0V, VSA=0.0V, VCC=3.3V, VDD=13V, Load =8KΩ/180pF, Line time=20us.
   This is equivalent to an all black display.
2. Power dissipation = [VCC*ICC]+[VDD*IDD]
   This parameter is from output to output and from driver to driver and represents one sigma(standard deviation)

* These values are the only simulation results.
  The format is as follows: the Value without LOAD Condition / the Value with LOAD Condition.
  Load Conditions are R=8Ω and C=180pF.
  The exact values will be modified after measuring values of silicon samples.

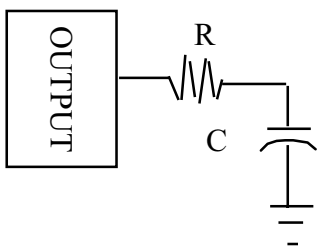
• Switching Characteristics

Supplies : VDD = 12.0V, VSA = 0.0V

Parameter	Symbol	Cond	Min	Typ	Max	Unit
Data Clock Frequency (Note 1)	DCLK	–	–	–	37.5	MHz
DCLK Pulse Width High (Note 1)	tCWH	–	8	–	–	ns
DCLK Pulse Width Low (Note 1)	tCWL	–	8	–	–	ns
Enable Setup Time	tsDI	–	4	–	–	ns
Enable Hold Time	thDI	–	4	–	–	ns
Data(Dx[7:0], RVRSx) Setup Time	tsDD	–	4	–	–	ns
Data(Dx[7:0], RVRSx) Hold Time	thDD	–	4			ns
LOAD Setup time	tsDL	–	4	–	–	ns
LOAD High Duration	twDL	–	1	–	–	DCLK period
LOAD to Enable Input Duration (Note 2)	tsLD1	–	2	–	–	DCLK period
LOAD to Enable Output Duration	tsLD2	–	1	–	–	DCLK period
POLC Setup Time	tsDP	–	4	–	–	ns
POLC Hold Time	thDP	–	4	–	–	ns
Enable Output Delay Time	tpdDO	Load=25pF	–	–	10	ns
Output High-Z Time	tpdDZ	–	–	49	–	DCLK period
Output Delay Time 1	tpdDE	(Note 3, 5)	–	–	3	us
Output Delay Time 2	tpdDX	(Note 4, 5)	–	–	7	us

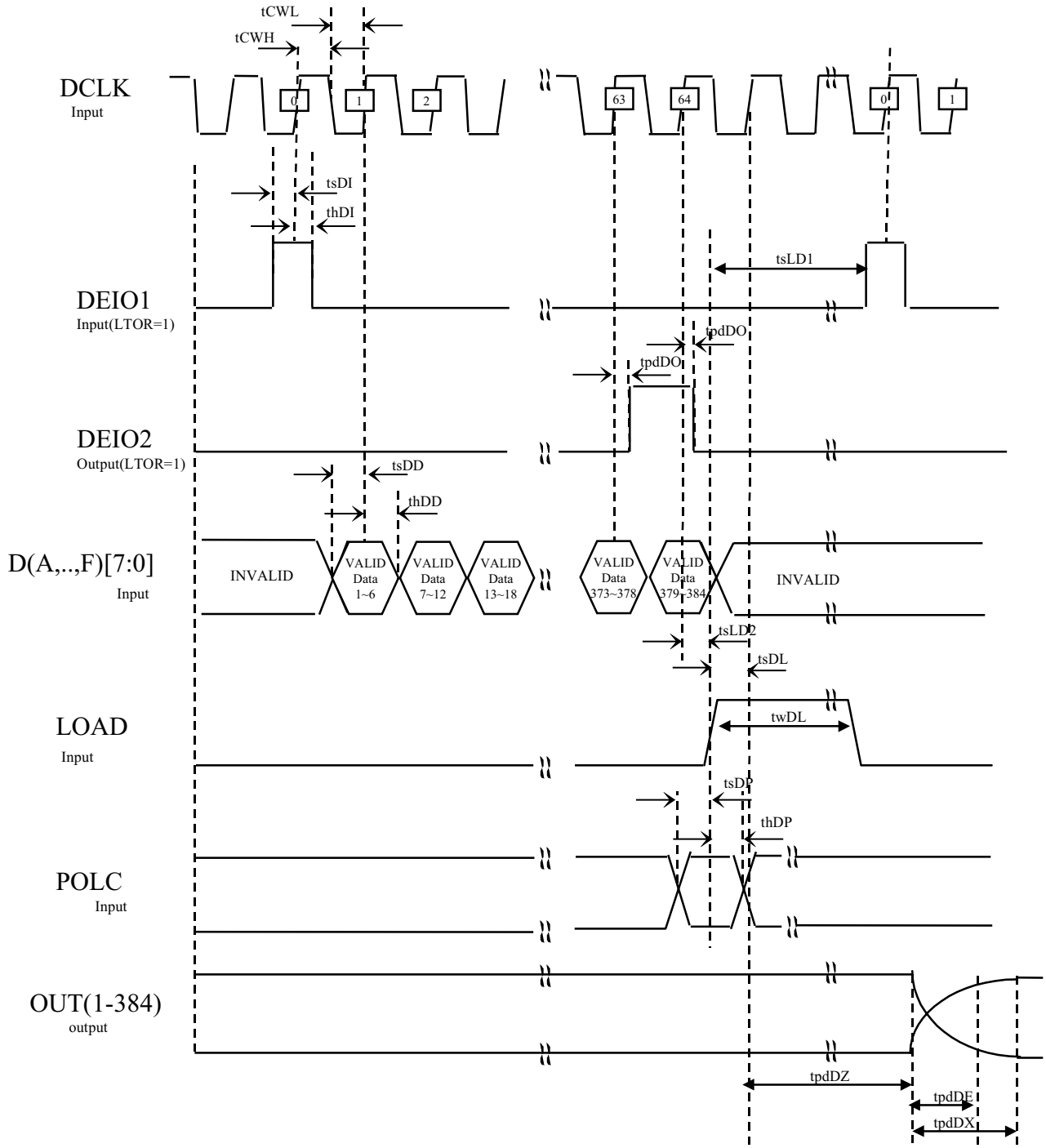
[Table 6] VCC = +3.3V , VSS=0.0V switching characteristics

Notes : 1. DCLK Rise/Fall=2.0ns max. (10%~90%)
2. Does not need to be synchronous to clock.
3. Target output voltage × 0.9
4. Target output voltage ± ΔVO
5. Load condition of analog output pin is shown in [Fig 6].



R = 8KΩ
C = 180pF

[Fig 6] Load conditions of analog output pin.
The values of R and C could be changed according to the situation.



[Fig 7] Timing diagram for cascaded devices with free-running DCLK.

Notes :

1. Most of signals need setup time due to Flip-flop setup time satisfaction