HYUNDAI
Electronics Industries

CMOS TFT-LCD SOURCE DRIVER

HM10S604

420/402CH TFT-LCD SOURCE DRIVER

PRELIMINARY

SPECIFICATION

HYUNDAI

HYUNDAI
Electronics Industries

CMOS TFT-LCD SOURCE DRIVER

• Description

HM10S604 is a source driver LSI that drives an active-matrix LCD panels, as well as a 64 gradation driver that implements multi-pin configuration and reduced power consumption.
HM10S604 has 420/402 panel drive outputs. Because it is expandable, the HM10S604 can easily be used in multiple application, its screen can be enlarged, and its $\overline{L}$/R(shift-direction switching) terminals can be used to simplify LCD panel interconnection.

The device has a large output dynamic range that makes the reverse driving of opposing electrodes in the LCD panel unnecessary; this reduces system power consumption and produces a high quality pictures. The device is also compatible with single sided mounting and dot reverse driving.

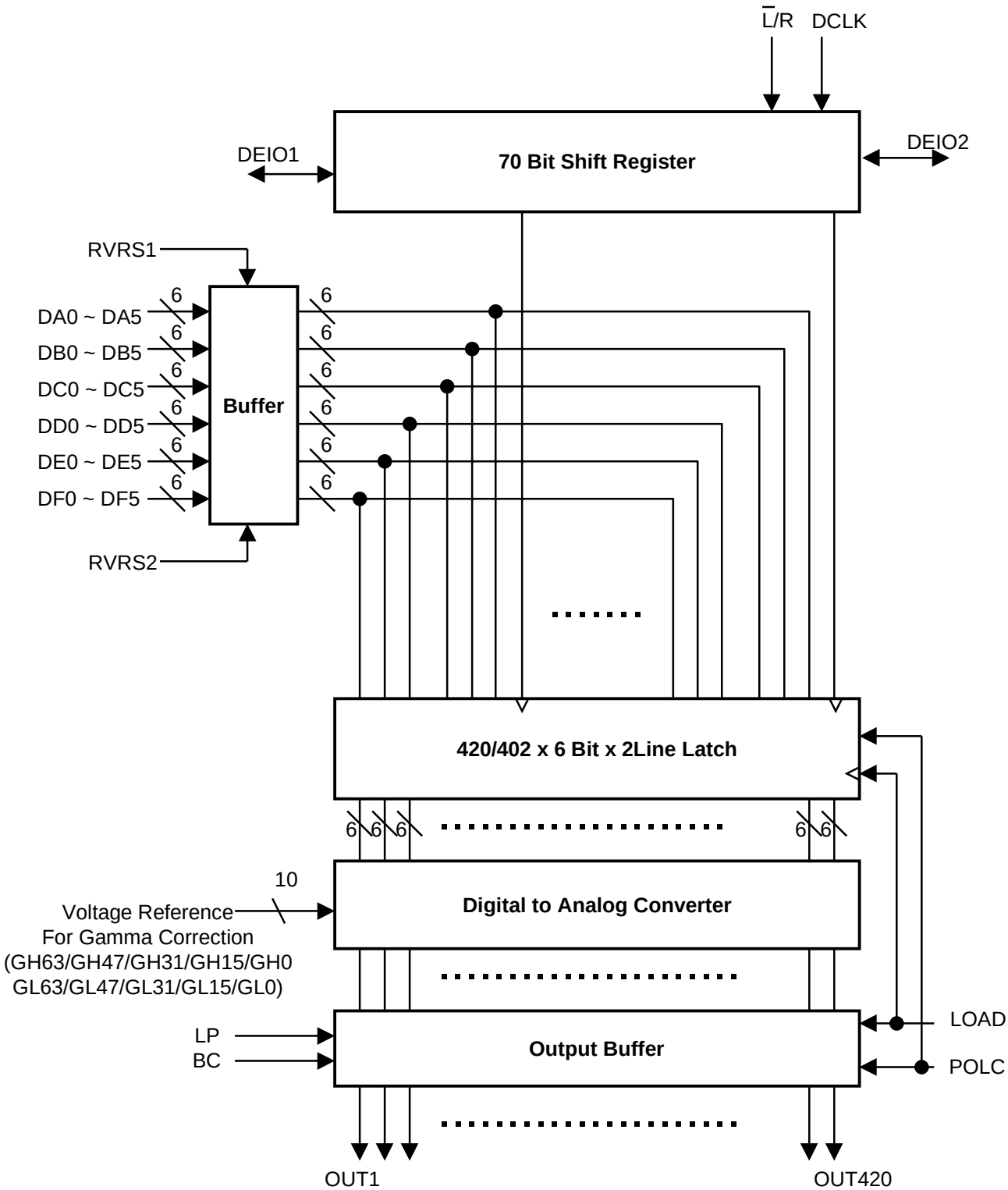
The HM10S604's 420/402 outputs ensure SXGA+ compatibility, making it useful in a wider range of applications.

The maximum operating clock frequency of the HM10S604 is 70MHz when the power supply voltage for the logic section is between 2.7V and 3.6V and the single-side driving of an LCD panel has been implemented.

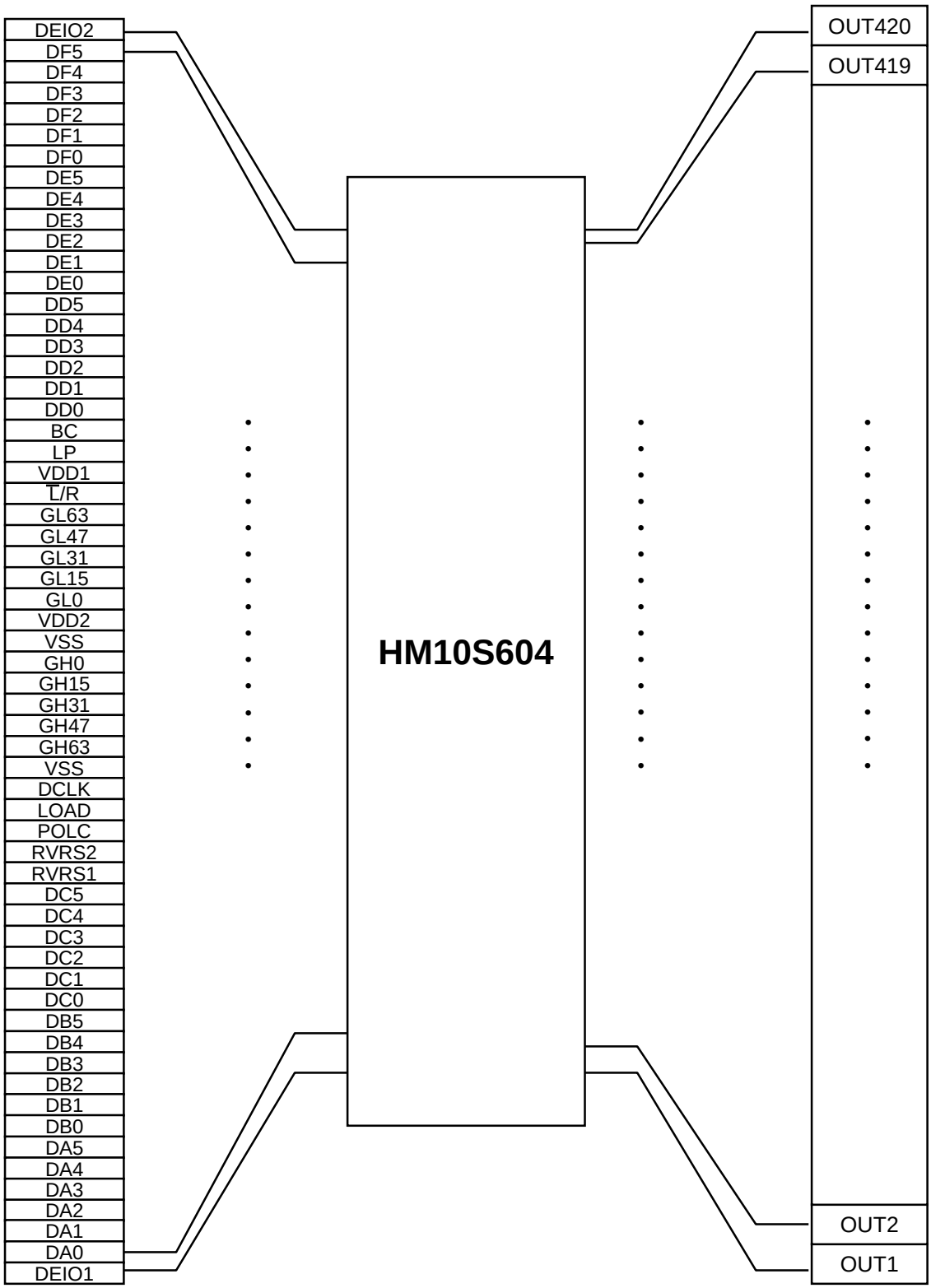
• Features

- ▶ Source Driver LSI for Active Matrix LCD
- ▶ Compatible With Dot inversion, n-line inversion, column-line inversion
- ▶ No Precharging
- ▶ Liquid Crystal Outputs : 420/402
- ▶ $\overline{L}$/R(shift-direction switching) terminals can be used to simplify LCD panel interconnection.
- ▶ Fine Pitch/TCP
- ▶ Driver With Internal 6-Bit Digital Input DAC
- ▶ Maximum Operating Clock Frequencies : 70MHz (Logic Section Power Supply : 2.7V - 3.6V)
- ▶ Dual Port Input
- ▶ Gamma Correction
- ▶ No Need For an External Reference Voltage Generation Circuit(or for Ramp Voltage or a Multi-Value Power Supply
- ▶ Low System Power Consumption Can be Accomplished Using the Low Power Mode.
- ▶ Can Handle Heavy Loads Using the LCD Capacity Switching Mode.
- ▶ Allows for Input Data Reversing
- ▶ Logic Section Power Supply Voltage : 2.7V - 3.6V
- ▶ Liquid Crystal Drive Section Power Supply Voltage : 6V - 10V

• Functional Block Diagram



• TCP Pin Configuration



• Terminal function

<table>
<tr><th colspan="2">TERMINAL</th><th rowspan="2">I/O</th><th rowspan="2">DESCRIPTION</th></tr>
<tr><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>DA0 - DA5
DB0 - DB5
DC0 - DC5</td><td>Port1
Image signal input terminal</td><td>I</td><td rowspan="2">Image signal input terminal
Inputs image signals with a 36-bit width
: 6bit gradation data X 6 dots(for 2 pixels)
Data inputs which select between one of 64 voltages
Dx0 : LSB, Dx5 : MSB</td></tr>
<tr><td>DD0 - DD5
DE0 - DE5
DF0 - DF5</td><td>Port2
Image signal input terminal</td><td>I</td></tr>
<tr><td>DEIO1
DEIO2</td><td>Start pulse I/O terminal</td><td>I/O</td><td>Internal shift register’s start pulse
<table><tr><th></th><th>$\overline{L}$/R=H</th><th>$\overline{L}$/R=L</th></tr><tr><td>DEIO1
DEIO2</td><td>Right shift input
Right shift output</td><td>Left shift output
Left shift input</td></tr></table></td></tr>
<tr><td>$\overline{L}$/R</td><td>Shift direction selection signal input terminal</td><td>I</td><td>Shift direction selection signal
Right shift (OUT1 ---> OUT420) : H
Left shift (OUT420 ---> OUT1) : L</td></tr>
<tr><td>DCLK</td><td>Shift clock Input terminal</td><td>I</td><td>Shift register clock input terminal
Writes the display data to the data register at the leading edge</td></tr>
<tr><td>VDD1
VDD2</td><td>Power supply</td><td>P</td><td>VDD1 Power supply for digital circuits.
VDD2 Power supply for analog circuits.</td></tr>
<tr><td>VSS</td><td>Ground</td><td>G</td><td>Ground for digital and analog</td></tr>
<tr><td>GHxx /
GLxx</td><td>Gamma correction reference potential input terminal</td><td>I</td><td>Potential input terminal for gamma correction
GH63 : The highest voltage in high voltage range.(necessary)
GH0 : The lowest voltage in high voltage range .(necessary)
GL0 : The highest voltage in low voltage range .(necessary)
GL63 : The lowest voltage in low voltage range .(necessary)
GH47/GL47, GH31/GL31, GH15/GL15
: Intermediate D/A voltage references (optional)</td></tr>
<tr><td>LOAD</td><td>Latch input terminal</td><td>I</td><td>Latches the data register contents with leading edge, transfers it to the D/A converter, and outputs the gradation voltage with trailing edge.</td></tr>
<tr><td>POLC</td><td>Polarity control terminal</td><td>I</td><td>POLC= L : odd numbered outputs : GH63 ~ GH0
even numbered outputs : GL0 ~ GL63
POLC= H : odd numbered outputs : GL0 ~ GL63
even numbered outputs : GH63 ~ GH0</td></tr>
<tr><td>RVRS1
RVRS2</td><td>Input data reverse terminal</td><td>I</td><td>Selects reversal/non-reversal of input data
RVRS1 : controls reversal/non-reversal of port1.
RVRS2 : controls reversal/non-reversal of port2.
RVRS1,2 = H : reversal
RVRS1,2 = L : non-reversal
This terminal can be processed within TCP. H & L are identified at the leading edge of each DCLK, like the data.</td></tr>
</table>

TERMINAL		I/O	DESCRIPTION
NAME	FUNCTION		
OUT1 ~ OUT420	LCD control output terminal	O	Sub-pixel output, provides 64 gray signals to the LCD panel.
BC	LCD drive capacity switching terminal	I	Switched LCD drive capacity : BC = H : heavy load mode BC = L : spec-load mode
LP	Low power mode selection terminal	I	Reduces charge and discharge current to a load LP = H : normal mode LP = L : low power mode

• Detailed description

Image signal capture

DEIOn=H(n=1 or n=2) is captured internally at the leading edge of DCLK. After the decay of DEIOn, the image signal data are captured in the internal latch with the rise of the next DCLK.

If DEIOn receives an input in the meantime, new image signal data is captured at the rise of the next DCLK after DEIOn decays.

It is possible to reverse the input data for each port by means of the RVRS1 and RVRS2.

Output expansion

The number of image signal output terminals can be expanded by cascading these devices,thereby enabling compatibility with large screens. Expansion is controlled by using the $\overline{L}$/R terminal:

$\overline{L}$/R=L : the previous stage DEIO1 terminals is connected to the next stage DEIO2, and input terminals other than DEIO1 and DEIO2 are connected together on each device.

$\overline{L}$/R=H : the previous stage DEIO2 terminals is connected to the next stage DEIO1, and input terminals other than DEIO1 and DEIO2 are connected together on each device

Relationship between input data values and output voltage

The output voltage is determined by the input data value and the 10 gamma correction potentials, Also, since the output voltage is compatible with dot reverse driving, it is possible to output gradation voltages for the opposing electrode voltages with polarities that differ for even and odd numbered outputs.

Input potentials with the same polarities relative to the opposing electrode voltages should be applied for GH63/GL63,GH47/GL47,GH31/GL31,GH15/GL15,GH0/GL0 of the gamma correction reference power supply.

Reference potential input for correction (i.e. GH63/GL63,GH47/GL47,GH31/GL31,GH15/GL15,GH0/GL0) should be applied externally as desired. Reference potential should be maintained during gradation voltage output. Refer to the operating conditions for the relative magnitude of each potential.

• Detailed description (continued)

Details of pixel signal data

Data format : 6bit X 2 RGB

Input width : 36bits (2-pixel data)

MSB LSB

Dx5	Dx4	Dx3	Dx2	Dx1	Dx0

Relationship between shift direction and output data:

$\overline{L}$/R = H (right shift)

Output	Out1	Out2	Out3	Out4	Out5	Out6	Out7	.....	Out420
Data	DA0-DA5	DB0-DB5	DC0-DC5	DD0-DD5	DE0-DE5	DF0-DF5	DA0-DA5	.....	DF0-DF5

$\overline{L}$/R = L (left shift)

Output	Out1	Out2	Out3	Out4	Out5	Out6	Out7	.....	Out420
Data	DA0-DA5	DB0-DB5	DC0-DC5	DD0-DD5	DE0-DE5	DF0-DF5	DA0-DA5	.....	DF0-DF5

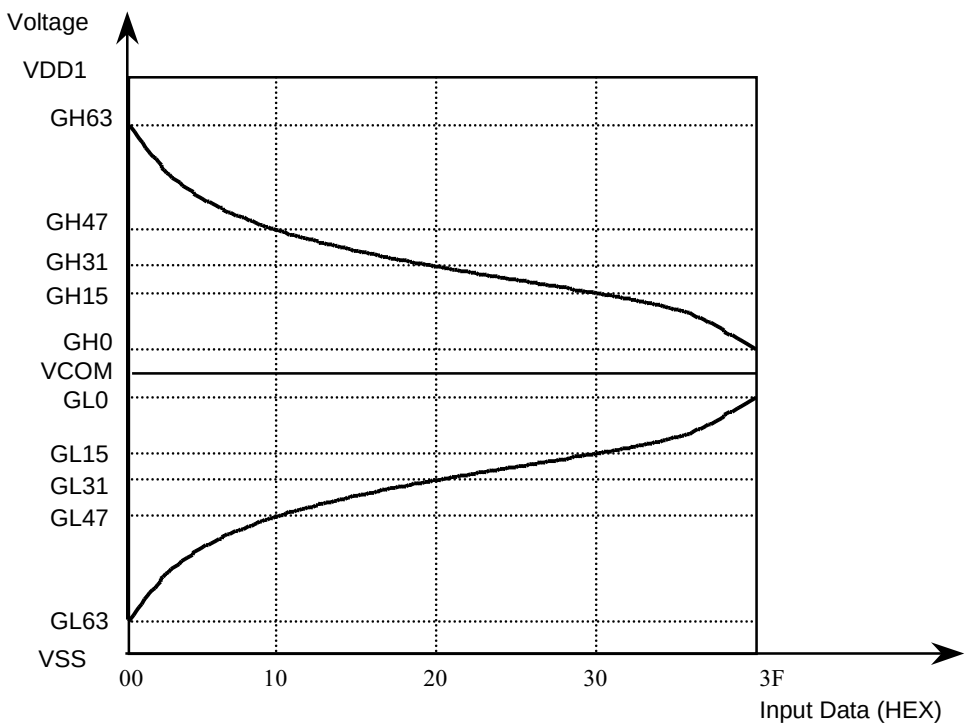
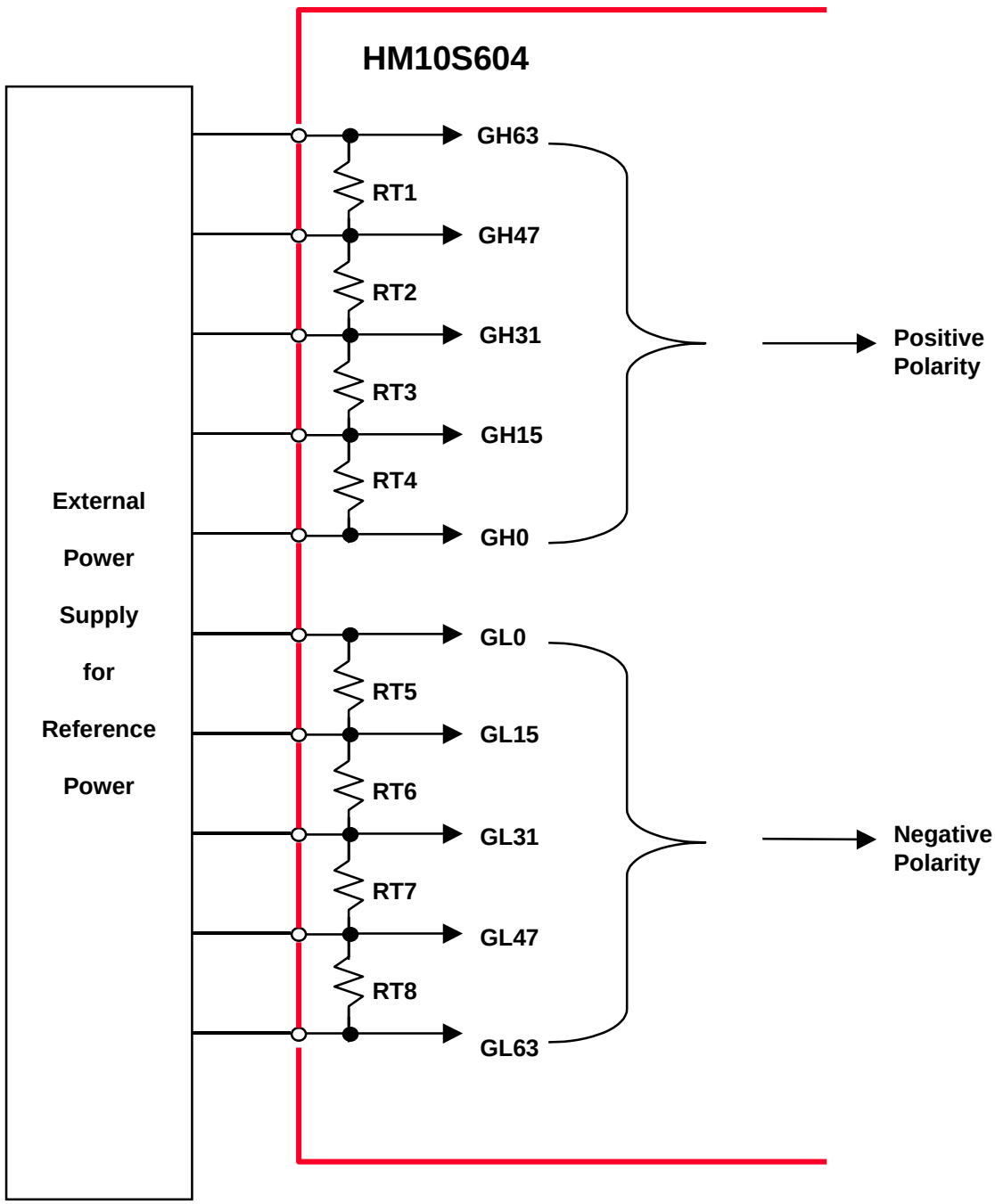


Fig 1. Conceptional Drawing of Gamma Correction

• Detailed description (continued)

Resistance Between Reference Potential Input Terminals for Gamma Correction



• Detailed description (continued)

Resistance Between Reference Potential Input Terminals for Gamma Correction

Reference Potential	Name	Resistance Ratio	Reference Potential	Name	Resistance Ratio
GH63 ,GL63	-	-	GH31,GL31	-	-
-	R0 R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15	840 560 504 448 392 392 392 392 336 336 336 280 280 280 280 168	-	R32 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47	112 112 112 112 112 112 112 112 112 112 112 112 112 112 112 112
GH47,GL47	-	-	GH15,GL15	-	-
-	R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31	168 168 168 168 168 168 168 168 168 168 168 112 112 112 112 112	-	R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62	112 112 112 112 112 168 168 168 168 168 224 280 280 616 1176
GH31,GL31	-	-	GH0,GL0	-	-

Relationship between Input data and output voltages at positive polarity

DATA (Hex)	Dx[5:0]	Output Voltage	DATA (Hex)	Dx[5:0]	Output Voltage
00	000000	GH63	20	100000	GH31
01	000001	GH47+(GH63 -GH47)X5376/6216	21	100001	GH15+(GH31-GH15)X1680/1792
02	000010	GH47+(GH63 -GH47)X4816/6216	22	100010	GH15+(GH31-GH15)X1568/1792
03	000011	GH47+(GH63 -GH47)X4312/6216	23	100011	GH15+(GH31-GH15)X1456/1792
04	000100	GH47+(GH63 -GH47)X3864/6216	24	100100	GH15+(GH31-GH15)X1344/1792
05	000101	GH47+(GH63 -GH47)X3472/6216	25	100101	GH15+(GH31-GH15)X1232/1792
06	000110	GH47+(GH63 -GH47)X3080/6216	26	100110	GH15+(GH31-GH15)X1120/1792
07	000111	GH47+(GH63 -GH47)X2688/6216	27	100111	GH15+(GH31-GH15)X1008/1792
08	001000	GH47+(GH63 -GH47)X2296/6216	28	101000	GH15+(GH31-GH15)X896/1792
09	001001	GH47+(GH63 -GH47)X1960/6216	29	101001	GH15+(GH31-GH15)X784/1792
0A	001010	GH47+(GH63 -GH47)X1624/6216	2A	101010	GH15+(GH31-GH15)X672/1792
0B	001011	GH47+(GH63 -GH47)X1288/6216	2B	101011	GH15+(GH31-GH15)X560/1792
0C	001100	GH47+(GH63 -GH47)X1008/6216	2C	101100	GH15+(GH31-GH15)X448/1792
0D	001101	GH47+(GH63 -GH47)X728/6216	2D	101101	GH15+(GH31-GH15)X336/1792
0E	001110	GH47+(GH63 -GH47)X448/6216	2E	101110	GH15+(GH31-GH15)X224/1792
0F	001111	GH47+(GH63 -GH47)X168/6216	2F	101111	GH15+(GH31-GH15)X112/1792
10	010000	GH47	30	110000	GH15
11	010001	GH31+(GH47-GH31)X2240/2408	31	110001	GH0+(GH15-GH0)X3864/3976
12	010010	GH31+(GH47-GH31)X2072/2408	32	110010	GH0+(GH15-GH0)X3752/3976
13	010011	GH31+(GH47-GH31)X1904/2408	33	110011	GH0+(GH15-GH0)X3640/3976
14	010100	GH31+(GH47-GH31)X1736/2408	34	110100	GH0+(GH15-GH0)X3528/3976
15	010101	GH31+(GH47-GH31)X1568/2408	35	110101	GH0+(GH15-GH0)X3416/3976
16	010110	GH31+(GH47-GH31)X1400/2408	36	110110	GH0+(GH15-GH0)X3248/3976
17	010111	GH31+(GH47-GH31)X1232/2408	37	110111	GH0+(GH15-GH0)X3080/3976
18	011000	GH31+(GH47-GH31)X1064/2408	38	111000	GH0+(GH15-GH0)X2912/3976
19	011001	GH31+(GH47-GH31)X896/2408	39	111001	GH0+(GH15-GH0)X2744/3976
1A	011010	GH31+(GH47-GH31)X728/2408	3A	111010	GH0+(GH15-GH0)X2576/3976
1B	011011	GH31+(GH47-GH31)X560/2408	3B	111011	GH0+(GH15-GH0)X2352/3976
1C	011100	GH31+(GH47-GH31)X448/2408	3C	111100	GH0+(GH15-GH0)X2072/3976
1D	011101	GH31+(GH47-GH31)X336/2408	3D	111101	GH0+(GH15-GH0)X1792/3976
1E	011110	GH31+(GH47-GH31)X224/2408	3E	111110	GH0+(GH15-GH0)X1176/3976
1F	011111	GH31+(GH47-GH31)X112/2408	3F	111111	GH0

Relationship between Input data and output voltages at negative polarity

DATA (Hex)	Dx[5:0]	Output Voltage
00	000000	GL63
01	000001	GL63+(GL47-GL63)X840/6216
02	000010	GL63+(GL47-GL63)X1400/6216
03	000011	GL63+(GL47-GL63)X1904/6216
04	000100	GL63+(GL47-GL63)X2352/6216
05	000101	GL63+(GL47-GL63)X2744/6216
06	000110	GL63+(GL47-GL63)X3136/6216
07	000111	GL63+(GL47-GL63)X3528/6216
08	001000	GL63+(GL47-GL63)X3920/6216
09	001001	GL63+(GL47-GL63)X4256/6216
0A	001010	GL63+(GL47-GL63)X4592/6216
0B	001011	GL63+(GL47-GL63)X4928/6216
0C	001100	GL63+(GL47-GL63)X5208/6216
0D	001101	GL63+(GL47-GL63)X5488/6216
0E	001110	GL63+(GL47-GL63)X5768/6216
0F	001111	GL63+(GL47-GL63)X6048/6216
10	010000	GL47
11	010001	GL47+(GL31-GL47)X168/2408
12	010010	GL47+(GL31-GL47)X336/2408
13	010011	GL47+(GL31-GL47)X504/2408
14	010100	GL47+(GL31-GL47)X672/2408
15	010101	GL47+(GL31-GL47)X840/2408
16	010110	GL47+(GL31-GL47)X1008/2408
17	010111	GL47+(GL31-GL47)X1176/2408
18	011000	GL47+(GL31-GL47)X1344/2408
19	011001	GL47+(GL31-GL47)X1512/2408
1A	011010	GL47+(GL31-GL47)X1680/2408
1B	011011	GL47+(GL31-GL47)X1848/2408
1C	011100	GL47+(GL31-GL47)X1960/2408
1D	011101	GL47+(GL31-GL47)X2072/2408
1E	011110	GL47+(GL31-GL47)X2184/2408
1F	011111	GL47+(GL31-GL47)X2296/2408

DATA (Hex)	Dx[5:0]	Output Voltage
20	100000	GL31
21	100001	GL31+(GL15-GL31)X112/1792
22	100010	GL31+(GL15-GL31)X224/1792
23	100011	GL31+(GL15-GL31)X336/1792
24	100100	GL31+(GL15-GL31)X448/1792
25	100101	GL31+(GL15-GL31)X560/1792
26	100110	GL31+(GL15-GL31)X672/1792
27	100111	GL31+(GL15-GL31)X784/1792
28	101000	GL31+(GL15-GL31)X896/1792
29	101001	GL31+(GL15-GL31)X1008/1792
2A	101010	GL31+(GL15-GL31)X1120/1792
2B	101011	GL31+(GL15-GL31)X1232/1792
2C	101100	GL31+(GL15-GL31)X1344/1792
2D	101101	GL31+(GL15-GL31)X1456/1792
2E	101110	GL31+(GL15-GL31)X1568/1792
2F	101111	GL31+(GL15-GL31)X1680/1792
30	110000	GL15
31	110001	GL15+(GL0-GL15)X112/3976
32	110010	GL15+(GL0-GL15)X224/3976
33	110011	GL15+(GL0-GL15)X336/3976
34	110100	GL15+(GL0-GL15)X448/3976
35	110101	GL15+(GL0-GL15)X560/3976
36	110110	GL15+(GL0-GL15)X728/3976
37	110111	GL15+(GL0-GL15)X896/3976
38	111000	GL15+(GL0-GL15)X1064/3976
39	111001	GL15+(GL0-GL15)X1232/3976
3A	111010	GL15+(GL0-GL15)X1400/3976
3B	111011	GL15+(GL0-GL15)X1624/3976
3C	111100	GL15+(GL0-GL15)X1904/3976
3D	111101	GL15+(GL0-GL15)X2184/3976
3E	111110	GL15+(GL0-GL15)X2800/3976
3F	111111	GL0

Absolute maximum ratings over operating free air temperature range(unless otherwise noted)

Parameter		Absolute Maximum Ratings	Unit
Supply Voltage	VDD1(Note1&2)	-0.5 ~ 5.5	V
	VDD2	-0.5 ~ 15.0	V
Input Voltage	V_{GMA} (Note3)	-0.5 ~ VDD2 + 0.5	V
	V_I (Inputs)	-0.5 ~ VDD1 + 0.5	V
Output Voltage	V_O (DEIO1,2)	-0.5 ~ VDD1 + 0.5	V
	V_O (OUT1 ~ 420)	-0.5 ~ VDD2 + 0.5	V
Storage Temperature Range , T_{STR}		-55 ~ 125	℃

Stresses beyond those listed under " absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under " recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Notes : 1. All voltage values are with respect to VSS = 0V.

2. Power up in the following order : VDD1 , control inputs, VDD2, V_{GMA}.
   Power down by reversing the sequence.
3. V_{GMA} = GH63/GL63,GH47/GL47,GH31/GL31,GH15/GL15,GH0/GL0
   The relative magnitudes of the reference potentials are as follows:
   VDD2 > GH63 > GH0 > GL0 > GL63>VSS

Recommended operating conditions

Parameter		MIN	TYP	MAX	Unit
Supply Voltage	VDD1	2.7	-	3.6	V
	VDD2	6.0		10.0	V
Output Voltage	V_O(OUT1 ~OUT420)	VSS+0.2		VDD2-0.2	V
Gamma correction potential	V_{GMA} (GH63 ~ GH0)	0.5*VDD2		VDD2-0.2	V
	V_{GMA} (GL0 ~ GL63)	VSS+0.2		0.5*VDD2	V
Clock frequency, f_{clk}	2.7V≤VDD1 ≤3.6V			70	MHz
Load capacitance for outputs, C_L				75	pF
Operating free air temperature, T_A		-10		75	℃

Electrical characteristics over recommended operating conditions

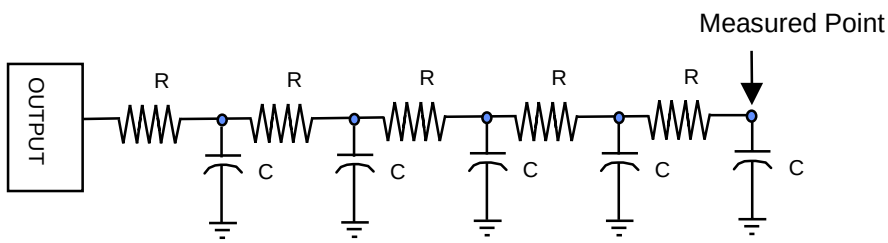
Parameter			Test Conditions	MIN	TYP	MAX	Unit
VIH	High level input voltage	Dx0~ Dx5,DCLK, LOAD,RVRS1,RVRS2 DEIO1,DEIO2, L/R,POLC,LP,BC	-	0.7VDD1		VDD1	V
VIL	Low level input voltage	Dx0~ Dx5,DCLK, LOAD,RVRS1,RVRS2 DEIO1,DEIO2,L/R, POLC,LP,BC	-	0		0.3VDD1	V
I_{lk}	Input leakage current	Dx0~ Dx5,DCLK, LOAD,RVRS1,RVRS2 DEIO1,DEIO2,L/R, POLC,LP,BC	-			±10	uA
I_{CHG}	Output current (Note 4)	OUT1 ~ OUT420	Vx = VDD2 - 0.2 V VO = Vx - 1.0 V			-110	uA
I_{DIS}			Vx = VSS2+ 0.2 V VO = Vx + 1.0 V	110			
Vo	Deviation between output voltage pins (Note 5)	OUT1 ~ OUT420	VSS + 0.2 ~ VDD2 - 0.2		±10		mV
$\triangle V_{AV}$	Average output variation (Note 6)	OUT1 ~ OUT420	-		±10		mV
R_{GMA}	Resistance between reference power supplies	GH63 ~ GH0 GL0 ~ GL63	-		14,392		Ω
DI_{DD2}	Supply current (during operation)	Analog section	LOAD interval = 20us fclk = 36 MHz, No load VDD2=8.0V Black raster pattern GH63 =7.8 V GL63 = 0.2 V		TBD		uA
SI_{DD2}	Supply current (during standby)		No load, VDD2=8V Black raster pattern GH63 =7.8 V GL63 = 0.2 V Clock and input signal are in the stop state		TBD		uA
DI_{DD1}	Supply current (during operation)	Digital section	LOAD interval = 20us fclk = 36 MHz, Checked dot test pattern		TBD		uA
SI_{DD1}	Supply current (during standby)		Clock and input signal are in the stop state		TBD		uA

Notes : 4. Vx is the output voltage of OUT1 ~ OUT420. Vo is the voltage impressed at OUT1 ~ OUT420.
5.This is the deviation between terminals with differences in positive and negative amplitude, when all chip outputs display the same data.
6. This is the inter-chip deviation in the average of the output voltage inter-pin deviation

Timing requirements over recommended operating free air temperature range.
VDD1 = 2.7V to 3.6V

Parameter		Test Conditions	MIN	TYP	MAX	Unit
tc1	DCLK cycle time	- See Fig 3.	14			ns
tw1	High level DCLK pulse width duration	- See Fig 3.	2.0			ns
tw2	Low level DCLK pulse width duration	- See Fig 3.	2.0			ns
tsu1	Data/REV setup time	- See Fig 3.	2.0			ns
th1	Data/REV hold time	- See Fig 3.	0			ns
tsu2	Start pulse setup time	- See Fig 3.	2.0			ns
th2	Start pulse hold time	- See Fig 3.	0			ns
td1	Start pulse signal delay time (Load = 25pF)	- See Fig 3			10	ns
td2	LCD drive signal delay time	- See Fig 4.note7,9			5	μs
td3		- See Fig 4.note8,9			8	μs
tsu3	LOAD signal EIO(input) setup time	- See Fig 4.	2			DCLK cycle
th3	LOAD low hold time from final data DCLK	- See Fig 4.	1			DCLK cycle
tw3	High level LOAD signal pulse width duration	- See Fig 4.	2			DCLK cycle
thiz	Output high impedance duration	- See Fig 4.note 10		66		DCLK cycle
		- See Fig 5.note 11		tw3+3 DCLK cycle		-
tsu4	POLC signal LOAD setup time	- See Fig 4.	-5			ns
th4	POLC signal LOAD hold time	- See Fig 4.	6.0			ns

Notes : 7. Specified as the value at which the driver's output voltage reaches the target output voltage ±(VDD2X0.1).
8. Specified as the value at which ther driver's output voltage reaches the target output voltage(6-bit precision)
9. The load of the analog output terminal is the value shown in Fig 2.
10. When LOAD high level pulse width duration is shorter than 63 DCLK cycle, high-Z duration is 66 DCLK cycle.
11. When LOAD high level pulse width duration is longer than 63 DCLK cycle, high-Z duration is tw3+3DCLK cycle.



R = 1kΩ
C = 15pF

Fig 2. Load conditions of analog output pin.
The values of R and C could be changed according to the situation.

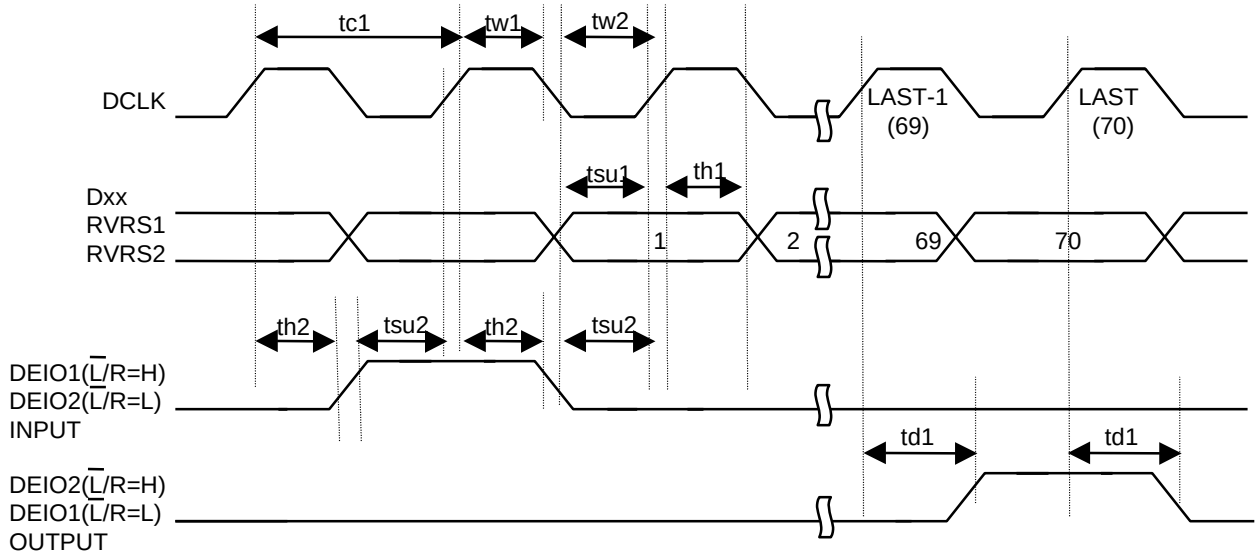


Fig 3. Timing Waveform

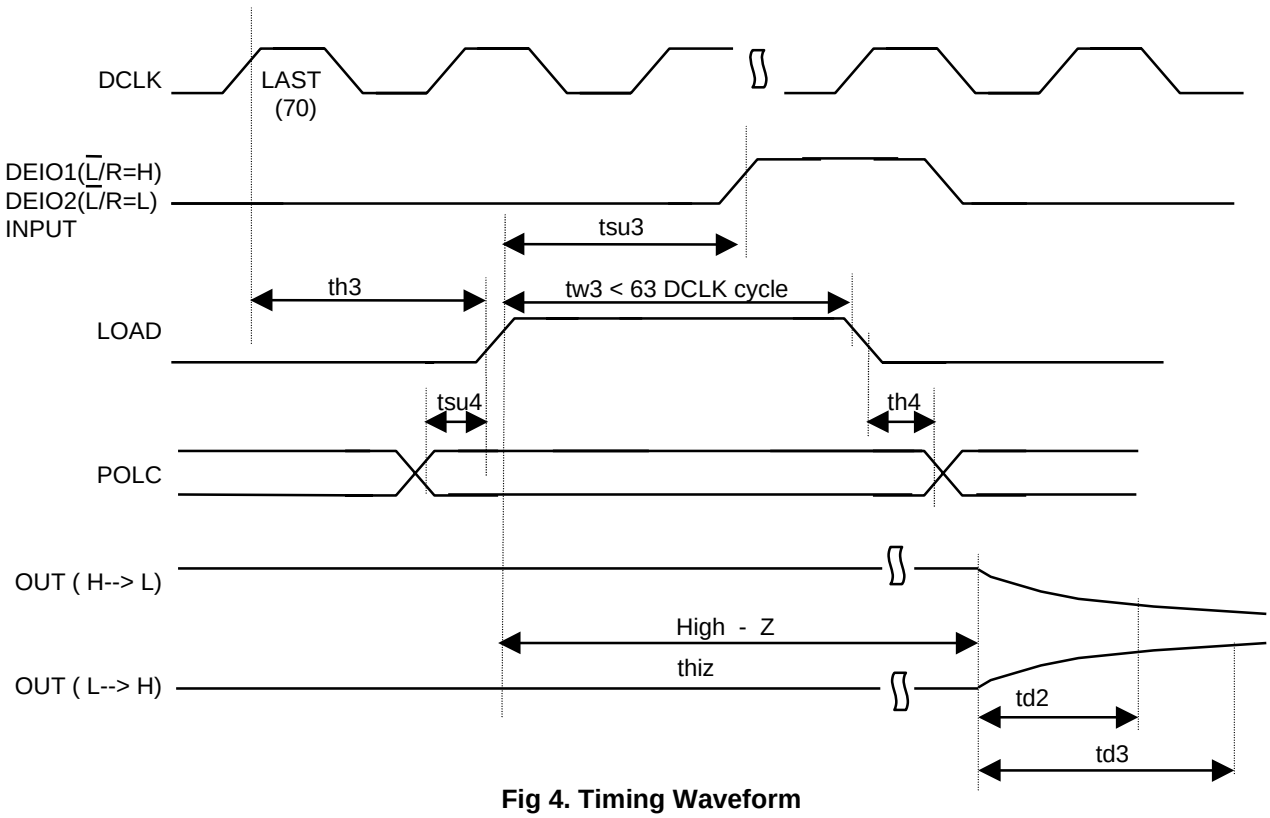


Fig 4. Timing Waveform

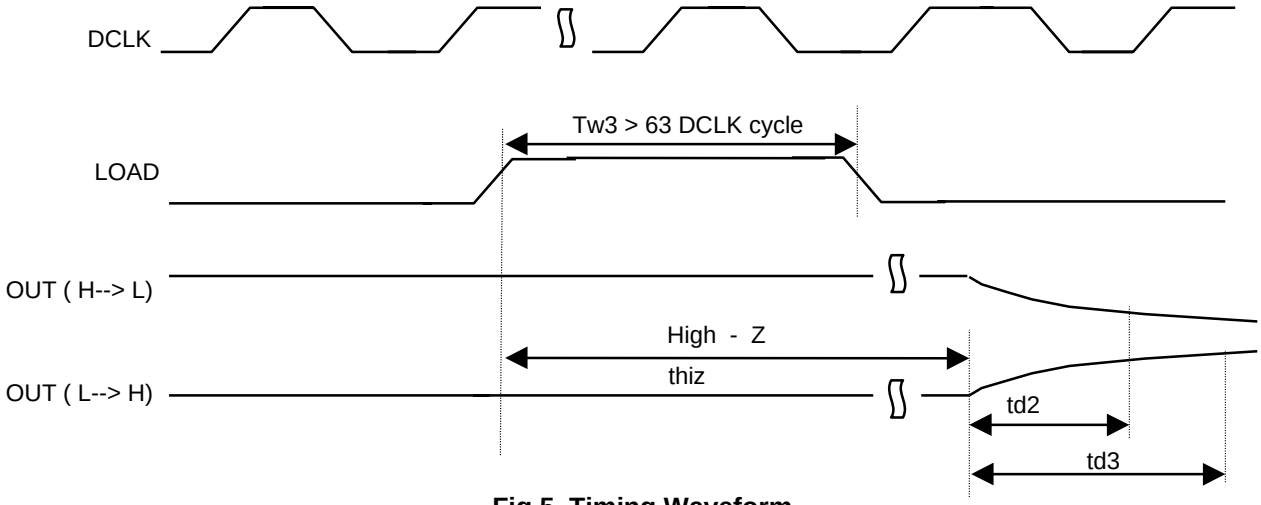


Fig 5. Timing Waveform

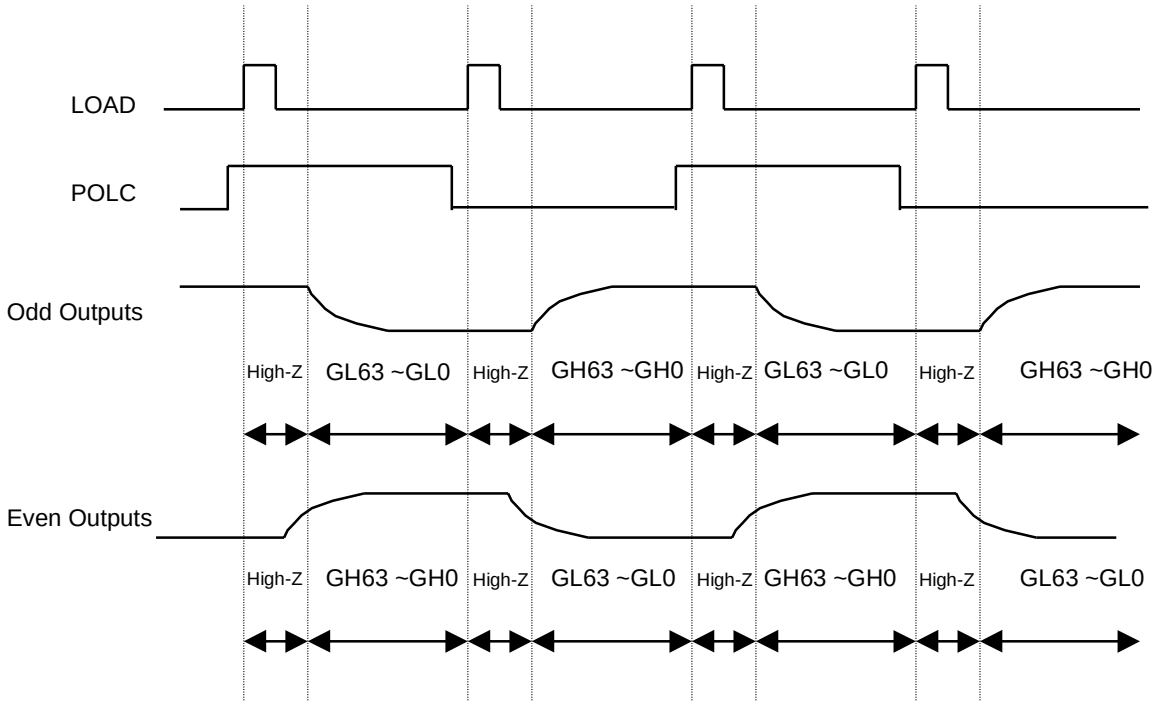


Fig 6. Relationship between LOAD, POLC, and outputs