

January 1998

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8-Bit, 35 MSPS, High Speed D/A Converter (TTL Input)

Features

- Resolution 8-Bit
- High Speed Operation 35MHz
(Maximum Conversion Speed)
- Non-Linearity Less Than $\pm 1/2$ LSB
- Low Glitch
- TTL Compatible Input
- Power Supply
 - Single +5V
 - Dual $\pm 5V$
- Low Power Consumption
 - +5V Single Power Supply (Typ) 200mW
 - $\pm 5V$ Dual Power Supply (Typ) 400mW
- Direct Replacement for the Sony CXA1106

Description

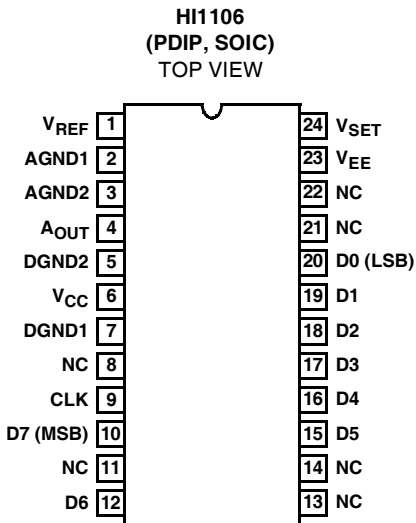
The HI1106 is an 8-bit, 35MHz, high-speed D/A converter IC. Summing type current for the upper 2 bits and ladder type resistance for the lower 6 bits, ensures a low power consumption of 200mW (single power supply).

This IC is suitable for digital TVs, graphic displays and other applications.

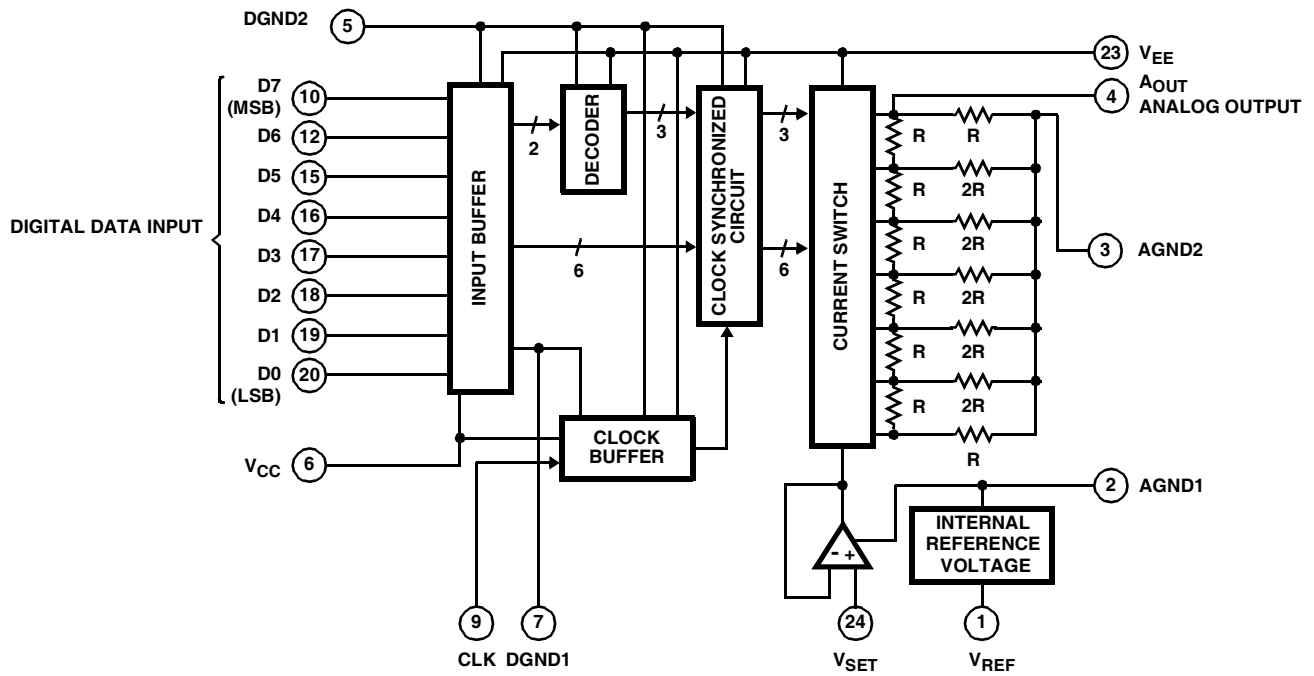
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1106JCB	-20 to 75	24 Ld SOIC	M24.2-S
HI1106JCP	-20 to 75	24 Ld PDIP	E24.4-S

Pinout



Functional Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1	V _{REF}		Internal Reference Voltage Output pin 1.2V (Typ). An external pull down resistance is necessary. For reference see Notes on Application 1.
2	AGND1		Set to Analog V _{CC} for signal power supply and to Analog GND for dual power supply. Connect to AGND2 and use.
3	AGND2		Connect to AGND1.
4	A _{OUT}		Analog Output pin.
5	DGND2		Set to Digital V _{CC} for signal power supply and to Digital GND for dual power supply.
6	V _{CC}		Digital V _{CC} .
7	DGND1		Digital GND.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
8	NC		No Connect.
9	CLK		Clock Input pin.
10, 12, 15 - 20	D7, D6, D5 - D0		Digital Input pin. D1 to MSB, D8 to LSB
11, 13, 14	NC		No Connect
21, 22	NC		Connect to AGND or V_{EE} .
23	V_{EE}		Set to Analog GND for single power supply and to V_{EE} for dual power supply.
24	V_{SET}		Bias Input pin. Normally set $V_{SET} - V_{EE}$ to 0.84V. For reference see Notes on Application 1.

NOTE: See the Application Circuit for reference.

Absolute Maximum Ratings $T_A = 25^{\circ}\text{C}$

Supply Voltage	
$V_{CC} - \text{DGND1}$0V to 6V
$V_{EE} - \text{AGND1, AGND2}$	-6V to 0V
DGND2 - DGND10V to 6V
Digital Input Voltage	
V_I	DGND1 - 0.3V to $V_{CC} + 0.3\text{V}$
V_{CLK}	DGND1 - 0.3V to $V_{CC} + 0.3\text{V}$
Input Voltage (V_{SET} Pin), V_{SET}	$V_{EE} - 0.3\text{V}$ to $V_{EE} + 2.7\text{V}$
Output Current (V_{REF} Pin), I_{REF}	-5mA to 0mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{\circ}\text{C}/\text{W}$)
PDIP Package	90
SOIC Package	90
Maximum Power Dissipation, P_D	1.27W
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}\text{C}$
Maximum Storage Temperature Range, T_{STG}	-55 $^{\circ}\text{C}$ to 150 $^{\circ}\text{C}$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}\text{C}$
(SOIC - Lead Tips Only)	

Recommended Operating Conditions

SINGLE POWER SUPPLY	MIN	TYP	MAX	DUAL POWER SUPPLY	MIN	TYP	MAX
Supply Voltage				Supply Voltage			
$V_{CC}, \text{DGND2}, \text{AGND1}, \text{AGND2}$	4.75V	5V	5.25V	V_{CC}	4.75V	5V	5.25V
DGND2 - AGND1, DGND2 - AGND2	-0.2V	0V	0.2V	V_{EE}	-5.5V	5V	-4.75V
AGND1 - AGND2	-0.1V	0V	0.1V	DGND2 - AGND1, DGND2 - AGND2	-0.2V	0V	-0.2V
Digital Input Voltage				AGND1 - AGND2	-0.1V	0V	0.1V
H Level, $V_{\text{IH}}, V_{\text{CLKH}}$	2.0V	-	V_{CC}	Digital Input Voltage			
L Level, $V_{\text{IL}}, V_{\text{CLKL}}$	DGND1	-	1V	H Level, $V_{\text{IH}}, V_{\text{CLKH}}$	2.0V	-	V_{CC}
V_{SET} Input Voltage, V_{SET}	0.70V	0.84V	1V	L Level, $V_{\text{IL}}, V_{\text{CLKL}}$	DGND1	-	1V
V_{REF} Pin Current, I_{REF}	-3.0mA	-	-0.4mA	V_{SET} Input Voltage, V_{SET}	-4.30V	-4.16V	-4.00V
Clock Pulse Width (Note 1)				V_{REF} Pin Current, I_{REF}	-3mA	-	-0.4mA
t_{PW1}	10ns	-	-	Clock Pulse Width			
t_{PW0}	10ns	-	-	t_{PW1}	10ns	-	-
Temperature Range, T_{OPR}	-20 $^{\circ}\text{C}$ to 75 $^{\circ}\text{C}$			t_{PW0}	10ns	-	-

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- See Figure 6 in the Timing Diagram.
- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^{\circ}\text{C}, V_{CC} = \text{DGND2} = \text{AGND1} = \text{AGND2} = 5\text{V}, \text{DGND1} = V_{EE} = 0\text{V}, V_{\text{SET}} = 0.84\text{V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINGLE POWER SUPPLY					
Resolution, n		-	8	-	Bit
Maximum Conversion Speed, f_{MAX}	$R_L > 10\text{k}\Omega, C_L < 20\text{pF}$	35	-	-	MHz
Linearity Error, EL	$R_L > 10\text{k}\Omega$	-0.5	-	0.5	LSB
Differential Linearity Error, ED		-0.5	-	0.5	LSB
Full Scale Output Voltage, V_{FS}	$R_L > 10\text{k}\Omega$	0.9	1.0	1.1	V
Offset Voltage (Note 2), V_{OS}	$R_L > 10\text{k}\Omega$	0	4	10	mV
Output Resistance, R_O		290	350	410	Ω
Power Supply Current, I_{CC}	$R_L > 10\text{k}\Omega, I_{\text{REF}} = -400\mu\text{A}$	32	40	48	mA
Digital Input Current					
H Level, I_{IH}		0	-	5	μA
L Level, I_{IL}		-400	-	0	μA
V_{SET} Input Current, I_{SET}		-3	-	0	μA
Internal Reference Output Voltage, V_{REF}	$I_{\text{REF}} = -400\mu\text{A}$	1.17	1.25	1.33	V
Accuracy Output Voltage Range, V_{OC}	$R_L > 10\text{k}\Omega$	0.5	1.0	1.50	V
Set-Up Time, t_s		10	-	-	ns
Hold Time, t_H		2	-	-	ns
Propagation Delay Time, t_{PD}	$R_L > 10\text{k}\Omega$	-	11	-	ns
Glitch Energy, GE	$R_L > 10\text{k}\Omega,$ $f_{\text{CLK}} = 1\text{MHz}, \text{Digital Lamp Output}$	-	30	-	pV/s

NOTE:

- $V_{\text{OS}} = \text{AGND2} - V_{255}$ (V_{255} is the output voltage when full input is at high level).

HI1106

Electrical Specifications $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $\text{DGND1} = \text{DGND2} = \text{AGND1} = \text{AGND2} = 0\text{V}$, $V_{EE} = -5\text{V}$, $V_{SET} - V_{EE} = 0.84\text{V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DUAL POWER SUPPLY					
Resolution, n		-	8	-	Bit
Maximum Conversion Speed, f_{MAX}	$R_L > 10\text{k}\Omega$, $C_L < 20\text{pF}$	35	-	-	MHz
Linearity Error, EL	$R_L > 10\text{k}\Omega$	-0.5	-	0.5	LSB
Differential Linearity Error, DNL		-0.5	-	0.5	LSB
Full Scale Output Voltage, V_{FS}	$R_L > 10\text{k}\Omega$	0.9	1.0	1.1	V
Offset Voltage, V_{OS}	$R_L > 10\text{k}\Omega$	0	4	10	mV
Output Resistance, R_O		290	350	410	Ω
Power Supply Current	$R_L > 10\text{k}\Omega$, $I_{REF} = -400\mu\text{A}$				
I_{CC}		24	30	36	mA
I_{EE}		40	50	60	mA
Digital Input Current					
H Level, I_{IH}		0	-	5	μA
L Level, I_{IL}		-400	-	0	μA
V_{SET} Input Current, I_{SET}		-3	-	0	μA
Internal Reference Output Voltage, V_{REF}	$I_{REF} = -400\mu\text{A}$	-3.83	-3.75	-3.67	V
Accuracy Output Voltage Range, V_{OC}	$R_L > 10\text{k}\Omega$	0.5	1.0	1.50	V
Set-Up Time, t_S		10	-	-	ns
Hold Time, t_H		2	-	-	ns
Propagation Delay Time, t_{PD}	$R_L > 10\text{k}\Omega$	-	11	-	ns
Glitch Energy, GE	$R_L > 10\text{k}\Omega$, $f_{CLK} = 1\text{MHz}$ Digital Lamp Output	-	30	-	pV/s

INPUT/OUTPUT CODE TABLE
(When Output Full Scale Voltage at 1.00V)

INPUT CODE								OUTPUT VOLTAGE (SINGLE SUPPLY)	OUTPUT VOLTAGE (DUAL SUPPLY)
MSB							LSB		
1	1	1	1	1	1	1	1	V_{CC}	-0V
1	0	0	0	0	0	0	0	$V_{CC} - 0.5\text{V}$	-0.5V
0	0	0	0	0	0	0	0	$V_{CC} - 1\text{V}$	-1V

Test Circuits

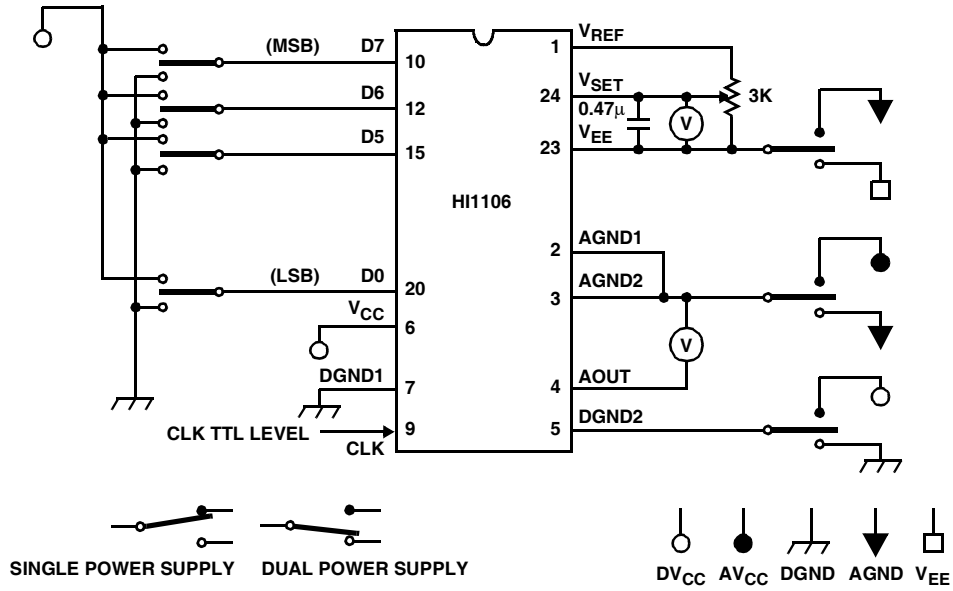


FIGURE 1. DC CHARACTERISTICS

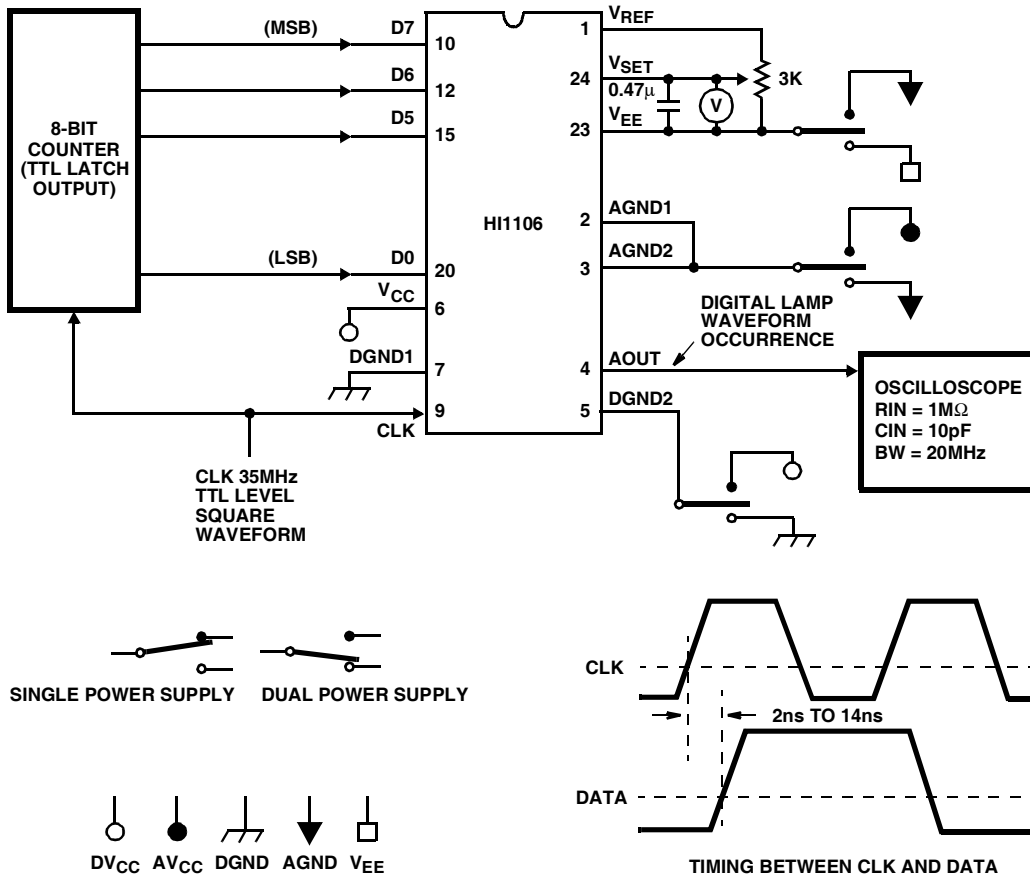


FIGURE 2. MAXIMUM CONVERSION SPEED

Test Circuits (Continued)

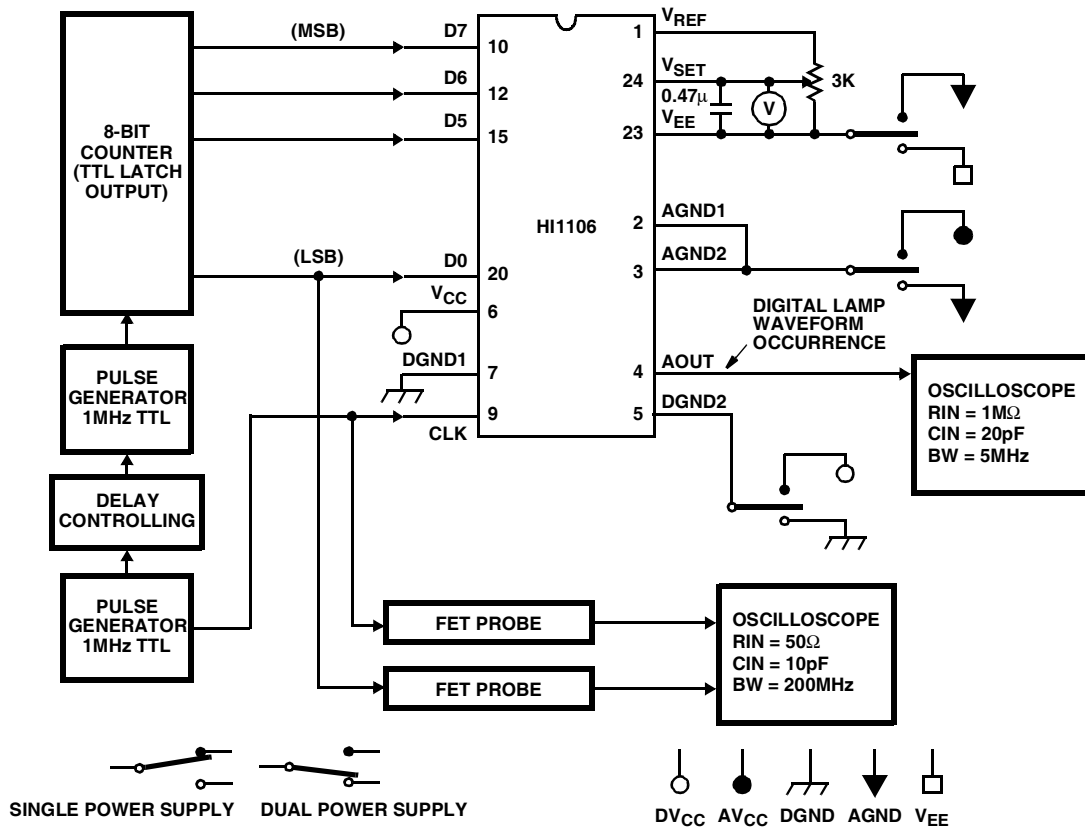


FIGURE 3. SET-UP TIME AND HOLD TIME

Test Circuits (Continued)

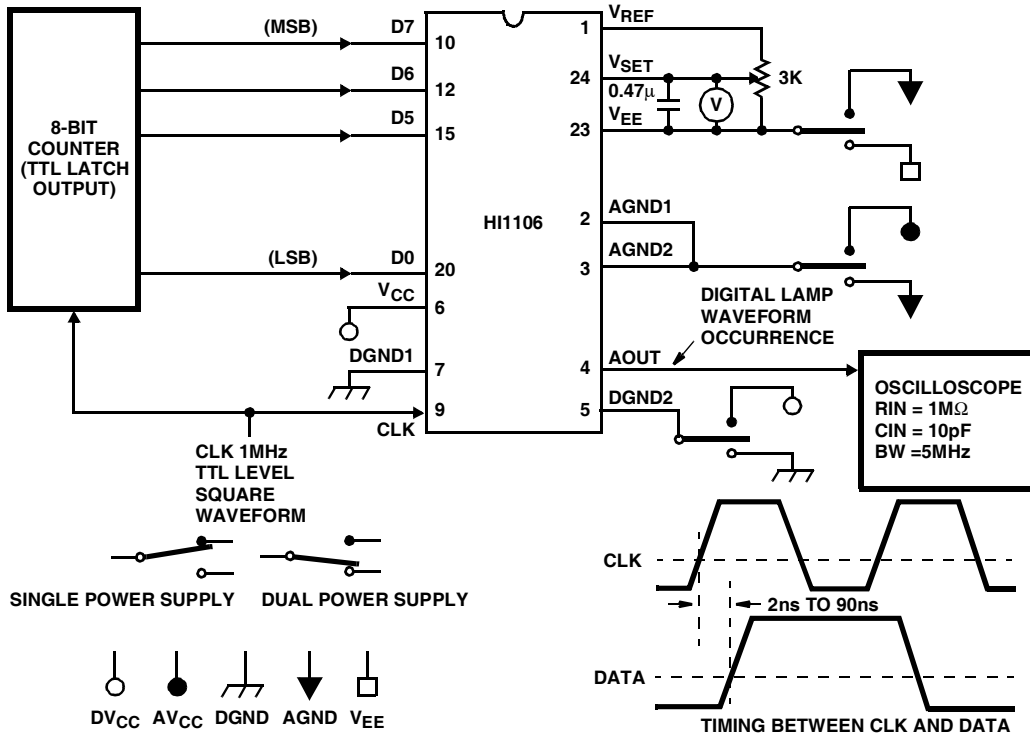


FIGURE 4. GLITCH AREA

Test Circuits (Continued)

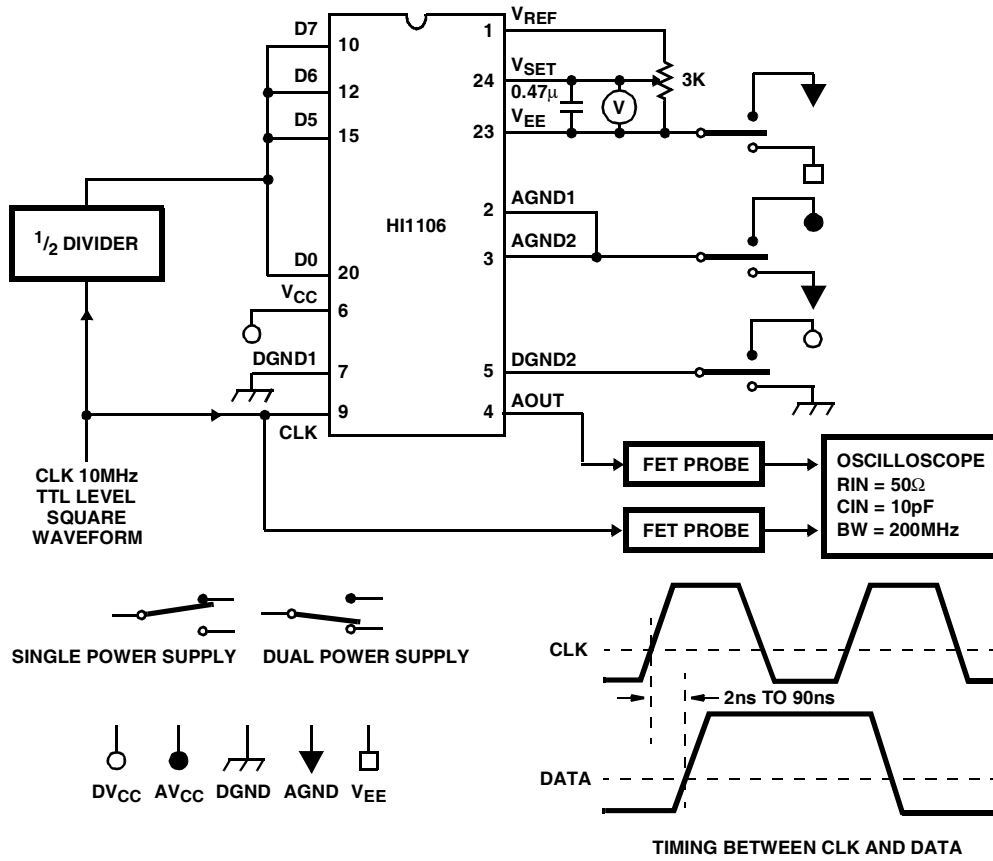


FIGURE 5. PROPAGATION DELAY TIME

Timing Diagram

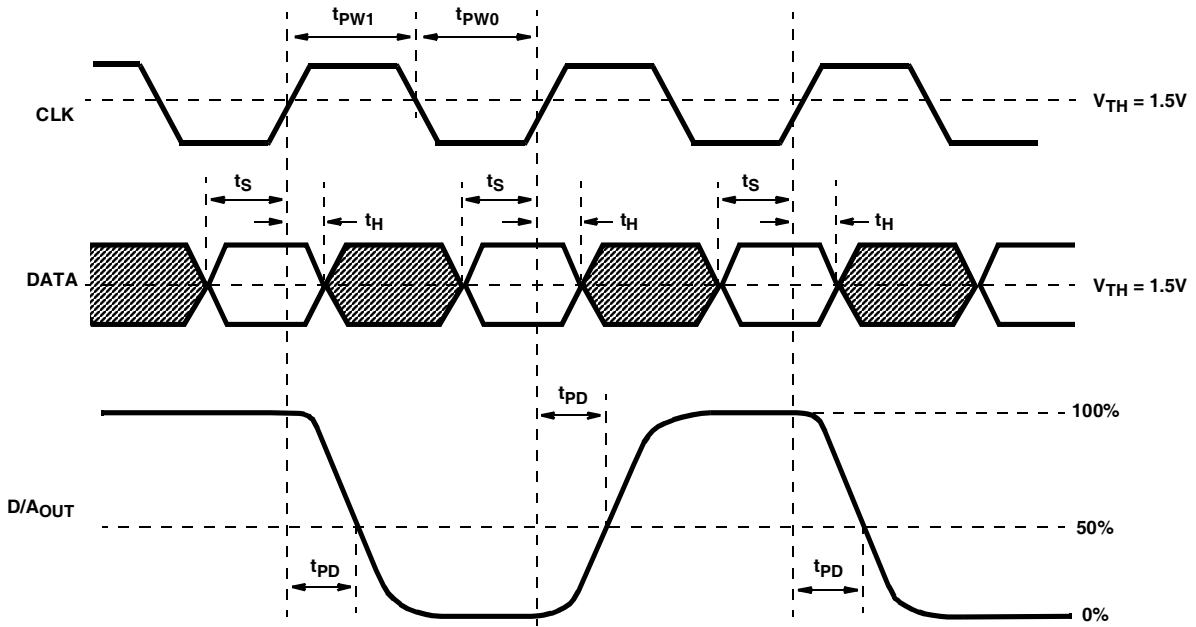


FIGURE 6.

Typical Performance Curves

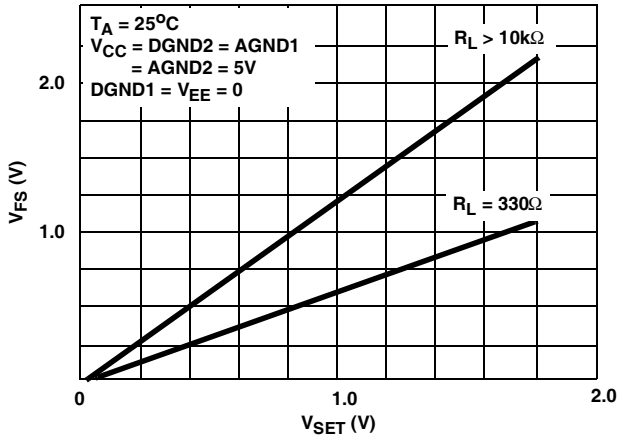


FIGURE 7. FULL-SCALE OUTPUT VOLTAGE (V_{FS}) vs V_{SET} (SINGLE POWER SUPPLY)

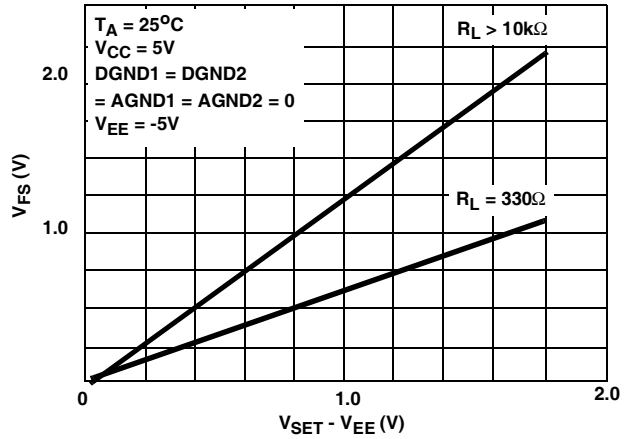


FIGURE 8. FULL-SCALE OUTPUT VOLTAGE (V_{FS}) vs $V_{SET} - V_{EE}$ (DUAL POWER SUPPLY)

Typical Performance Curves (Continued)

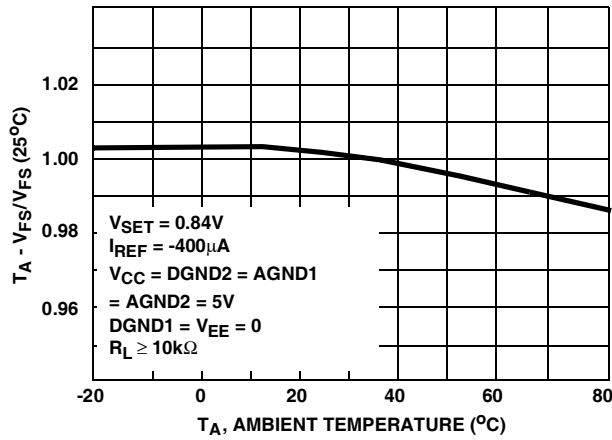


FIGURE 9. FULL-SCALE OUTPUT VOLTAGE (V_{FS}) vs TEMPERATURE (SINGLE POWER SUPPLY)

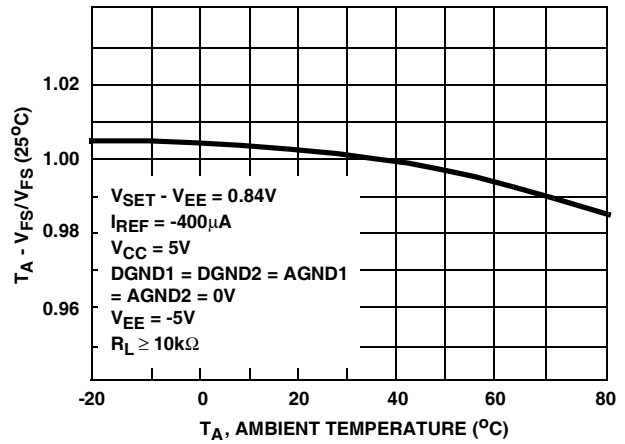


FIGURE 10. FULL-SCALE OUTPUT VOLTAGE (V_{FS}) vs TEMPERATURE (DUAL POWER SUPPLY)

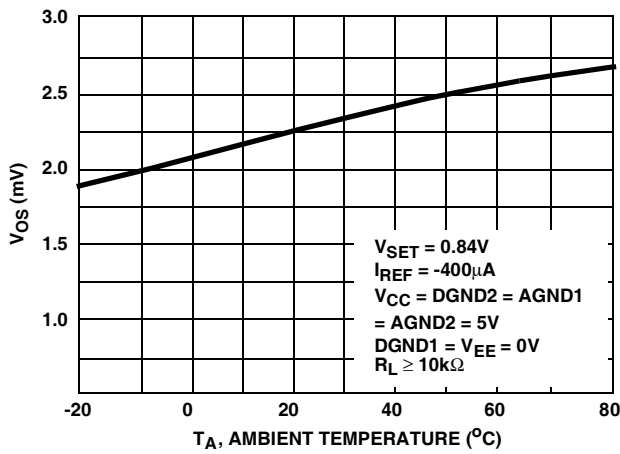


FIGURE 11. OUTPUT OFFSET VOLTAGE (V_{OS}) vs TEMPERATURE (SINGLE POWER SUPPLY)

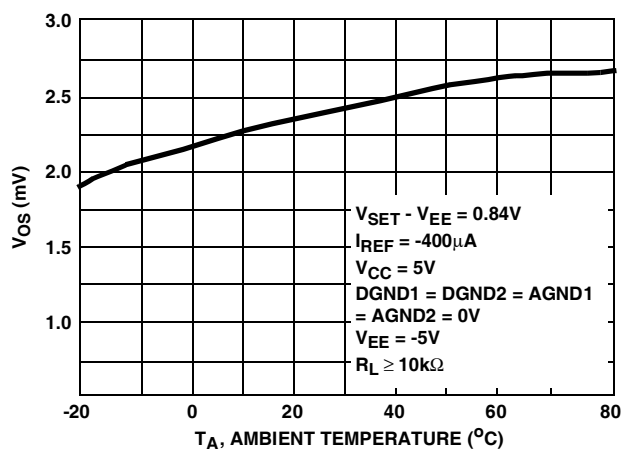


FIGURE 12. OUTPUT OFFSET VOLTAGE (V_{OS}) vs TEMPERATURE (DUAL POWER SUPPLY)

Typical Performance Curves (Continued)

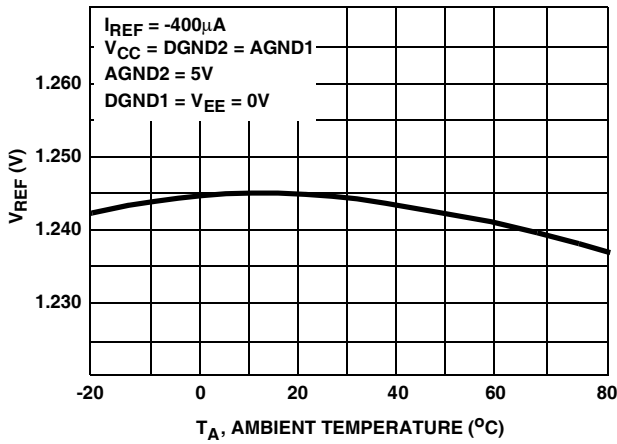


FIGURE 13. INTERNAL REFERENCE VOLTAGE (V_{REF}) vs TEMPERATURE (SINGLE POWER SUPPLY)

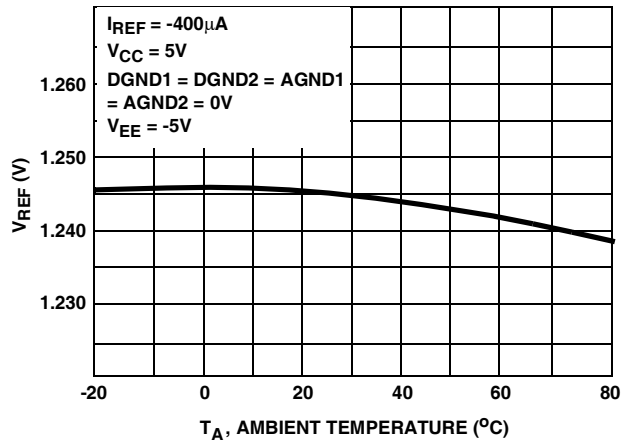


FIGURE 14. INTERNAL REFERENCE VOLTAGE (V_{REF}) vs TEMPERATURE (DUAL POWER SUPPLY)

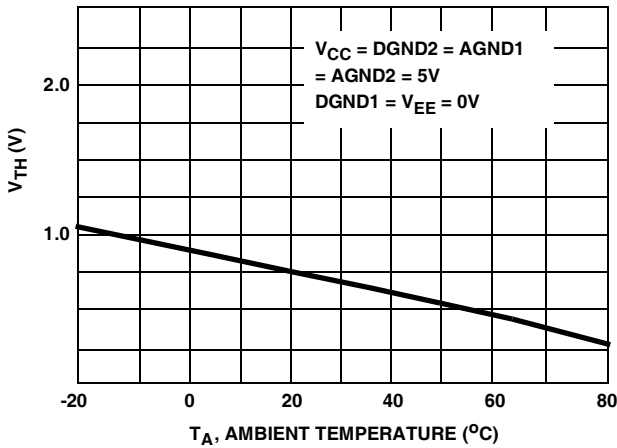


FIGURE 15. THRESHOLD VOLTAGE (V_{TH}) OF DIGITAL INPUT vs TEMPERATURE (SINGLE POWER SUPPLY)

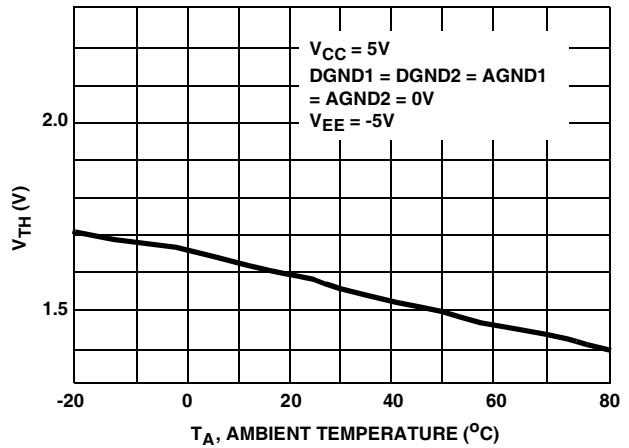


FIGURE 16. THRESHOLD VOLTAGE (V_{TH}) OF DIGITAL INPUT vs TEMPERATURE (DUAL POWER SUPPLY)

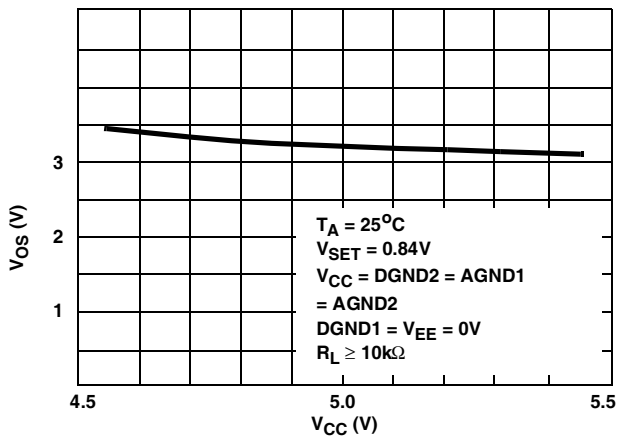


FIGURE 17. OUTPUT OFFSET VOLTAGE (V_{OS}) vs SUPPLY VOLTAGE (SINGLE POWER SUPPLY)

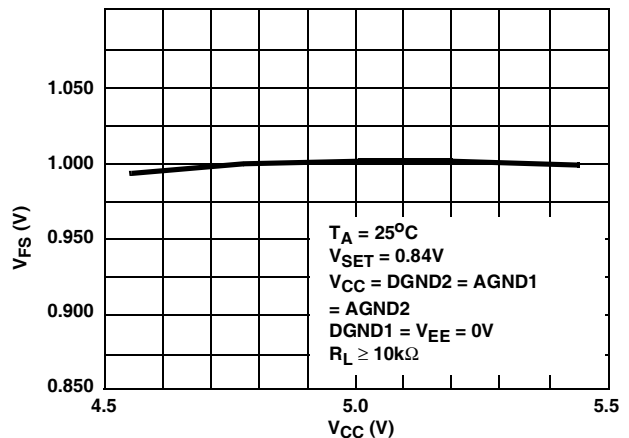


FIGURE 18. OUTPUT FULL-SCALE VOLTAGE (V_{FS}) vs SUPPLY VOLTAGE (DUAL POWER SUPPLY)

Typical Performance Curves (Continued)

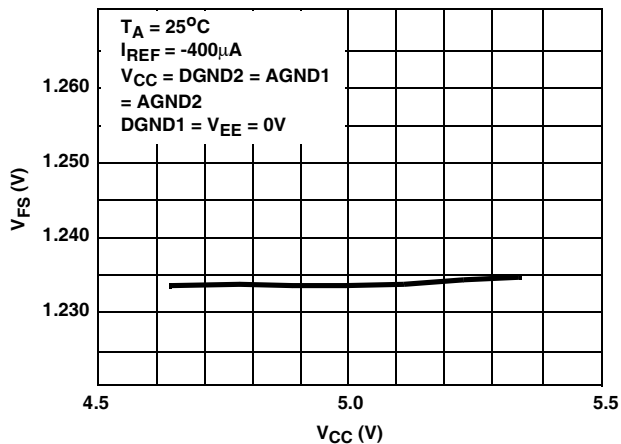


FIGURE 19. INTERNAL REFERENCE VOLTAGE (V_{REF}) vs SUPPLY VOLTAGE (SINGLE POWER SUPPLY)

Application Circuits

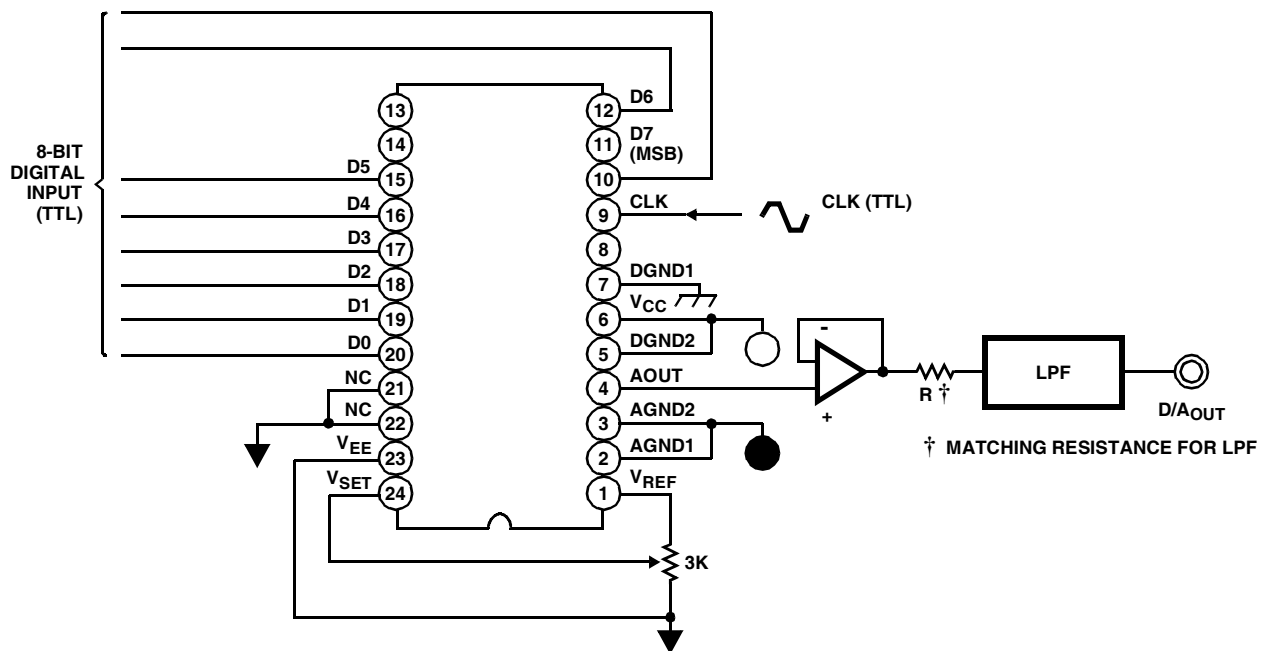


FIGURE 20. SINGLE POWER SUPPLY

Application Circuits

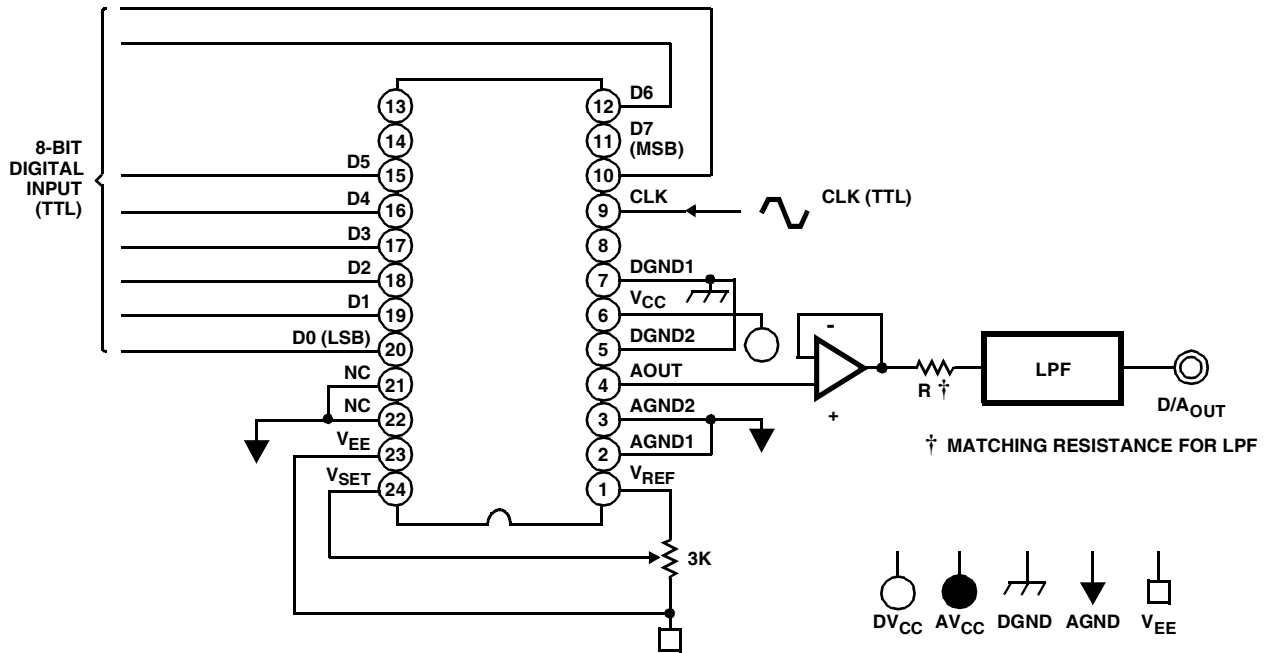


FIGURE 21. DUAL POWER SUPPLY

Notes On Application

1. Setting of V_{REF} Pin (Pin 24)

The full-scale voltage of the D/A output is determined by V_{SET} input voltage. As about $(1.2V - V_{EE})$ DC voltage is generated at V_{REF} pin (Pin 1) by connecting an external resistor from V_{REF} pin to V_{EE} pin (Pin 23), divide this voltage using resistors and apply it to V_{SET} pin as Figure 22. Example of usage:

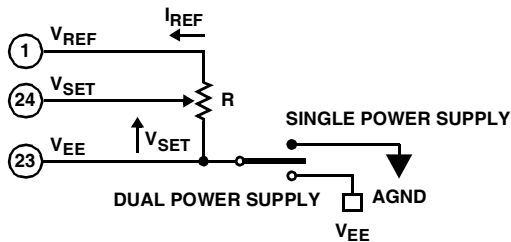


FIGURE 22.

The full-scale voltage of the D/A output can be determined from the following equation:

$$V_{FS} = 1.2 (V_{SET} - V_{EE}) \quad (R_L > 10k\Omega, 0.4V \leq V_{SET} \leq 1.2V)$$

Select an external resistor R (connected to V_{REF} pin) so that I_{REF} (current of an external resistor) is within the value indicated as the Recommended Operating Conditions of $(-3mA < I_{REF} < -0.4mA)$.

2. Phase Relation Between Data and Clock

To make the best use of the inherent characteristics of this D/A converter the phase relation between the data and clock applied from the exterior, should be properly set. Set up time (t_S) and Hold time (t_H) should be as indicated in the Electrical Specifications. For t_S and t_H refer to Figure 6 in the Timing Waveform. Also, set the clock pulse width according to the Recommended Operating Conditions.

3. D/A Output Pin Load

Receive the D/A output stage at high impedance, so as to obtain:

$$R_L > 10k\Omega,$$

$$C_L < 20pF.$$

4. Noise Reduction

Refer to the following notes in order to minimize noise contamination that occurs from outside the IC and penetrates D/A output.

- The power supply line and ground line should be made as wide as possible when fixed to the printed circuit board. Analog and Digital circuits should be separated.
- Connected a bypass capacitor between each of DV_{CC} (Pin 6) and $DGND1$ (Pin 7); $AGND1, 2$ (Pins 2, 3) and V_{EE} (Pin 23); V_{SET} (Pin 24) and V_{EE} (Pin 23), respectively.