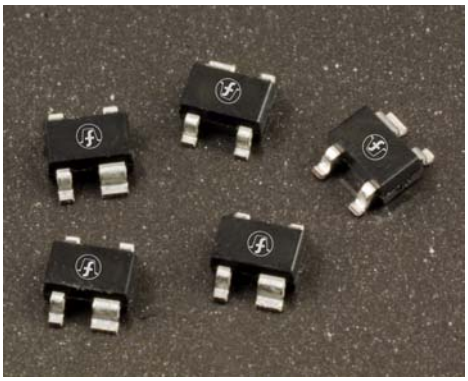


- PERFORMANCE (1850 MHz)
  - 0.5 dB Noise Figure
  - 20 dBm Output Power (P_{1dB})
  - 20 dB Small-Signal Gain (SSG)
  - 32 dBm Output IP3
  - Evaluation Boards Available

- DESCRIPTION AND APPLICATIONS

The FPD6836SOT343 is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 µm x 360 µm Schottky barrier Gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and input power levels. The FPD6836 is available in die form and in other packages.

Typical applications include drivers or output stages in PCS/Cellular base station high-intercept-point LNAs, WLL and WLAN systems, and other types of wireless infrastructure systems.

- ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
RF SPECIFICATIONS MEASURED AT f = 1850 MHz USING CW SIGNAL						
Minimum Noise Figure	NF	V_{DS} = 3.0 V; I_{DS} = 50% I_{DSS}		0.5	0.9	dB
		V_{DS} = 3.0 V; I_{DS} = 25% I_{DSS}		0.4		
Output Third-Order Intercept Point (from 15 to 5 dB below P_{1dB})	IP3	V_{DS} = 3.0 V; I_{DS} = 50% I_{DSS}	32			dBm
		V_{DS} = 3.0 V; I_{DS} = 25% I_{DSS}		30		
		Tuned for Optimum IP3				
Small-Signal Gain	SSG	V_{DS} = 3.0 V; I_{DS} = 50% I_{DSS}	18	20		dB
		V_{DS} = 3.0 V; I_{DS} = 25% I_{DSS}		18		
Power at 1dB Gain Compression	P_{1dB}	V_{DS} = 3.0 V; I_{DS} = 50% I_{DSS}	18	20		dBm
		V_{DS} = 3.0 V; I_{DS} = 25% I_{DSS}		18		
Saturated Drain-Source Current	I_{DSS}	V_{DS} = 1.3 V; V_{GS} = 0 V	90		135	mA
Maximum Drain-Source Current	I_{MAX}	V_{DS} = 1.3 V; $V_{GS} \cong$ +1 V		200		mA
Transconductance	G_M	V_{DS} = 1.3 V; V_{GS} = 0 V		100		mS
Gate-Source Leakage Current	I_{GSO}	V_{GS} = -5 V		1	10	µA
Pinch-Off Voltage	$\|V_P\|$	V_{DS} = 1.3 V; I_{DS} = 0.75 mA	0.7	1.0	1.3	V
Gate-Source Breakdown Voltage	$\|V_{BDGS}\|$	I_{GS} = 0.75 mA	12	18		V
Gate-Drain Breakdown Voltage	$\|V_{BDGD}\|$	I_{GD} = 0.75 mA	12	18		V

• ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$-3V < V_{GS} < +0V$		6	V
Gate-Source Voltage	V_{GS}	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	I_{DS}	For $V_{DS} > 2V$		I_{DSS}	mA
Gate Current	I_G	Forward or reverse current		5	mA
RF Input Power[2]	P_{IN}	Under any acceptable bias state		60	mW
Channel Operating Temperature	T_{CH}	Under any acceptable bias state		175	ºC
Storage Temperature	T_{STG}	Non-Operating Storage	-40	150	ºC
Total Power Dissipation	P_{TOT}	See De-Rating Note below		0.5	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits		80	%

[1] $T_{Ambient}$ = 22°C unless otherwise noted [2] Max. RF Input Limit must be further limited if input VSWR > 2.5:1
[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings will result in permanent damage to the device.
- Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where:
  P_{DC}: DC Bias Power
  P_{IN}: RF Input Power
  P_{OUT}: RF Output Power
- Total Power Dissipation to be de-rated as follows above 22°C:
  $P_{TOT} = 0.5W - (0.0056W/°C) \times T_{PACK}$
  where T_{PACK} = *source tab lead temperature above 22°C*
  (coefficient of de-rating formula is the Thermal Conductivity)

Example: For a 65°C source lead temperature: $P_{TOT} = 0.5W - (0.0056 \times (65 - 22)) = 0.26W$

• HANDLING PRECAUTIONS

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A per ESD-STM5.1-1998, Human Body Model. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

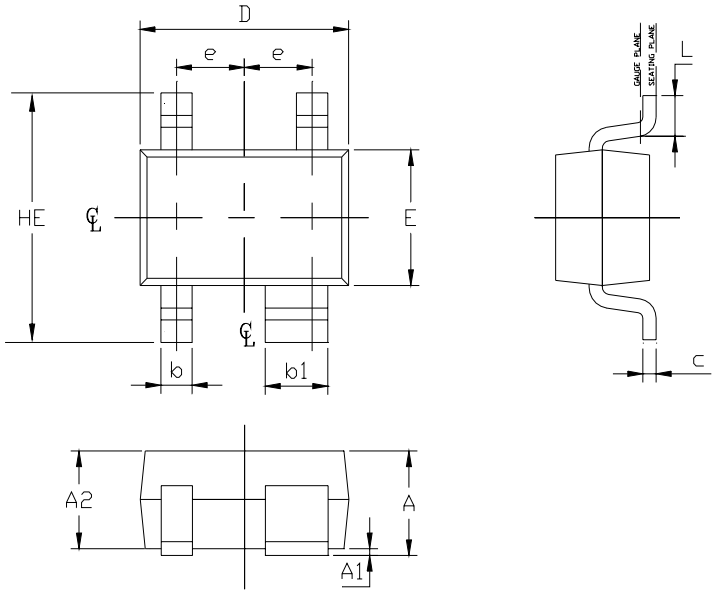
• APPLICATIONS NOTES & DESIGN DATA

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site. Evaluation Boards available upon request.

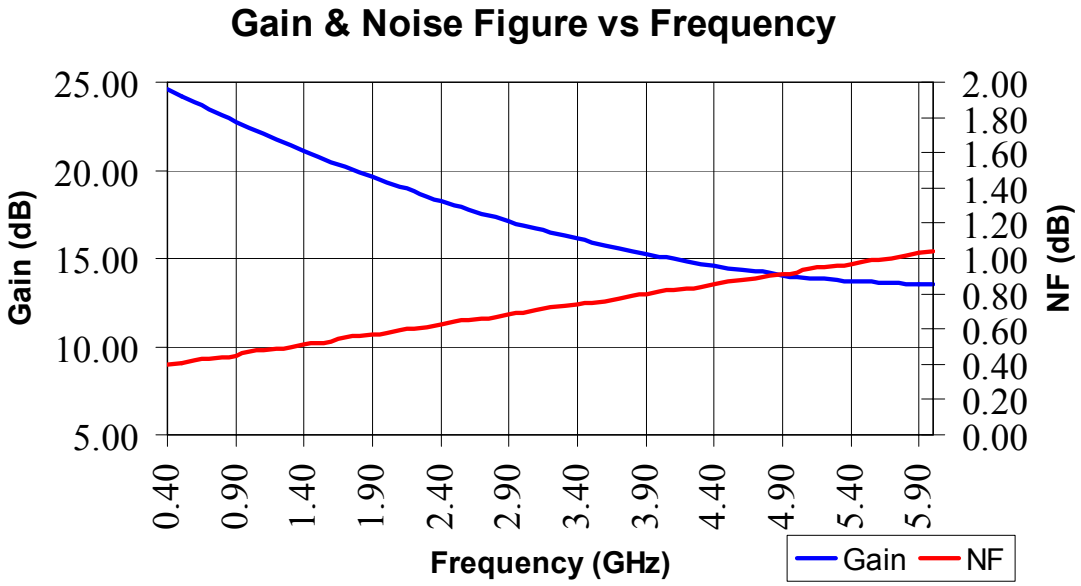
- BIASING GUIDELINES
  - Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.
  - Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices such as the FPD750SOT343.
  - Self-biased circuits employ an RF-bypassed Source resistor to provide the negative Gate-Source bias voltage, and such circuits provide some temperature stabilization for the device. A nominal value for circuit development is 5.45 Ω for a 50% of I_{DSS} operating point.
  - For standard Class A operation, a 50% of I_{DSS} bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Note that pHEMTs, since they are "quasi- E/D mode" devices, exhibit Class AB traits when operated at 50% of I_{DSS}. To achieve a larger separation between P_{1dB} and IP3, an operating point in the 25% to 33% of I_{DSS} range is suggested. Such Class AB operation will not degrade the IP3 performance.

- PACKAGE OUTLINE

(dimensions in mm)



SYMBOL	MIN	MAX
E	1.15	1.35
D	1.85	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
e	0.65 BSC	
b	0.25	0.40
b1	0.55	0.70
c	0.10	0.18
L	0.26	0.46


Gain & Noise Figure vs Frequency
Gain (dB)
25.00
20.00
15.00
10.00
5.00
NF (dB)
2.00
1.80
1.60
1.40
1.20
1.00
0.80
0.60
0.40
0.20
0.00
0.40
0.90
1.40
1.90
2.40
2.90
3.40
3.90
4.40
4.90
5.40
5.90
Frequency (GHz)
Gain
NF