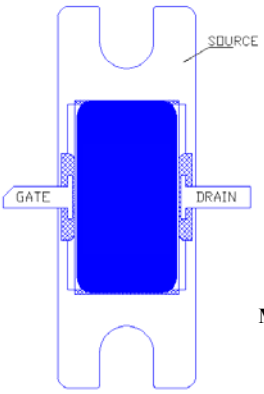
- PERFORMANCE (1.8 GHz)
  - 36.5 dBm Output Power (P_{1dB})
  - 10.5 dB Power Gain (G_{1dB})
  - 49 dBm Output IP3
  - 10V Operation
  - 45% Power-Added Efficiency
  - Evaluation Boards Available
  - Additional Design Data Available on Website
  - Usable Gain to 4GHz



SEE PACKAGE OUTLINE FOR MARKING CODE

- DESCRIPTION AND APPLICATIONS

The FPD4000AF is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT), optimized for power applications in L-Band. The high power flange-mount package has been optimized for low electrical parasitics and optimal heatsinking.

Typical applications include drivers or output stages in PCS/Cellular base station transmitter amplifiers, as well as other power applications in WLL/WLAN amplifiers.

- ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
RF SPECIFICATIONS MEASURED AT f = 1.8 GHz USING CW SIGNAL						
Power at 1dB Gain Compression	P_{1dB}	V_{DS} = 10V; I_{DQ} = 720 mA Γ_S and Γ_L tuned for Optimum IP3	35.5	36.5		dBm
Power Gain at dB Gain Compression	G_{1dB}	V_{DS} = 10V; I_{DQ} = 720 mA Γ_S and Γ_L tuned for Optimum IP3	9.5	10.5		
Maximum Stable Gain S_{21}/S_{12}	MSG	V_{DS} = 10 V; I_{DQ} = 720 mA P_{IN} = 0dBm, 50Ω system		19		dB
Power-Added Efficiency at 1dB Gain Compression	PAE	V_{DS} = 10V; I_{DQ} = 720 mA Γ_S and Γ_L tuned for Optimum IP3		45		%
3rd-Order Intermodulation Distortion	IP3	V_{DS} = 10V; I_{DQ} = 720 mA Γ_S and Γ_L tuned for Optimum IP3 P_{OUT} = 25.5 dBm (single-tone level)		-47	-44	dBc
Saturated Drain-Source Current	I_{DSS}	V_{DS} = 1.3 V; V_{GS} = 0 V	1.9	2.3	2.65	A
Maximum Drain-Source Current	I_{MAX}	V_{DS} = 1.3 V; V_{GS} ≅ +1 V		3.6		A
Transconductance	G_M	V_{DS} = 1.3 V; V_{GS} = 0 V		2.4		S
Gate-Source Leakage Current	I_{GSO}	V_{GS} = -3 V		70	170	µA
Pinch-Off Voltage	$\|V_P\|$	V_{DS} = 1.3 V; I_{DS} = 8 mA	0.7	0.9	1.4	V
Gate-Source Breakdown Voltage	$\|V_{BDGS}\|$	I_{GS} = 8 mA	6	8		V
Gate-Drain Breakdown Voltage	$\|V_{BDGD}\|$	I_{GD} = 8 mA	20	22		V
Thermal Resistivity (channel-to-case)	Θ_{CC}	See Note on following page		12		°C/W

- RECOMMENDED OPERATING BIAS CONDITIONS

  Drain-Source Voltage: From 5V to 10V

  Quiescent Current: From 25% I_{DSS} to 55% I_{DSS}

- ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$-3V < V_{GS} < +0V$		12	V
Gate-Source Voltage	V_{GS}	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	I_{DS}	For $V_{DS} > 2V$		I_{DSS}	mA
Gate Current	I_G	Forward / Reverse current		+25/-4	mA
RF Input Power[2]	P_{IN}	Under any acceptable bias state		1.5	W
Channel Operating Temperature	T_{CH}	Under any acceptable bias state		175	ºC
Storage Temperature	T_{STG}	Non-Operating Storage	-40	150	ºC
Total Power Dissipation	P_{TOT}	See De-Rating Note below		12	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits		80	%

[1] $T_{Ambient}$ = 22°C unless otherwise noted [2] Max. RF Input Limit must be further limited if input VSWR > 2.5:1

[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings will result in permanent damage to the device.
- Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where:

  P_{DC}: DC Bias Power

  P_{IN}: RF Input Power

  P_{OUT}: RF Output Power
- Total Power Dissipation to be de-rated as follows above 22°C:

  $P_{TOT} = 12 - (0.083W/°C) \times T_{PACK}$

  where T_{PACK} = *source tab lead temperature above 22°C*

  (coefficient of de-rating formula is the Thermal Conductivity)

Example: For a 55°C source lead temperature: $P_{TOT} = 12 - (0.083 \times (55 - 22)) = 9.3W$

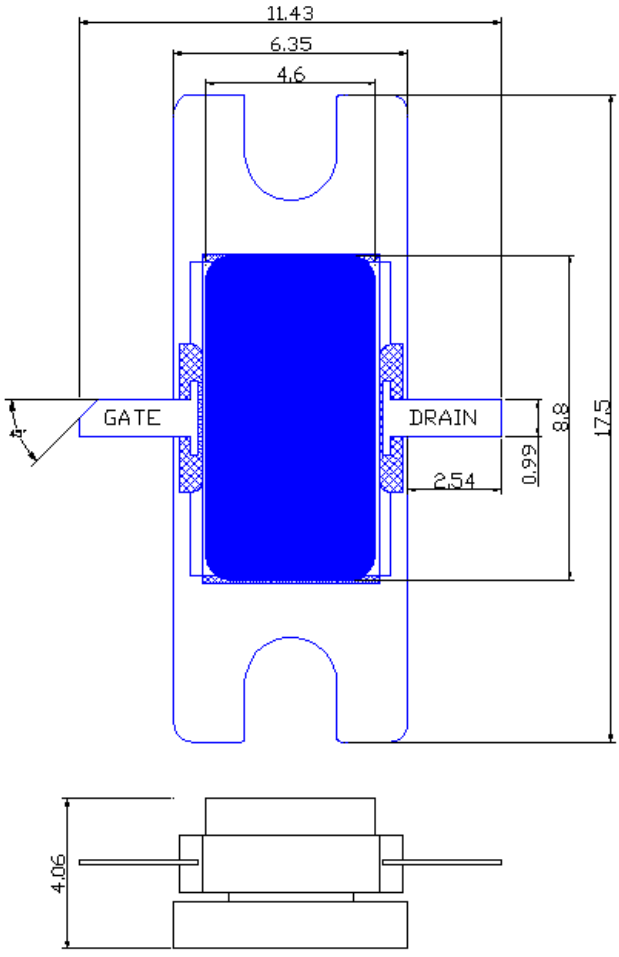
- *Note on Thermal Resistivity:* The nominal value of 12°C/W is measured with the package mounted on a large heatsink with thermal compound to ensure adequate contact. The package temperature is referred to the Source flange.

- HANDLING PRECAUTIONS

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A per ESD-STM5.1-1998, Human Body Model. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

- BIASING GUIDELINES
  - Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.
  - Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices such as the FPD4000AF.
  - Self-biased circuits employ an RF-bypassed Source resistor to provide the negative Gate-Source bias voltage, and such circuits provide some temperature stabilization for the device. A nominal value for circuit development is 0.7 Ω for the recommended 720mA operating point. This approach will require a DC Source resistor capable of at least 365mW dissipation.
  - The recommended 720mA bias point is nominally a Class AB mode. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point.

- PACKAGE OUTLINE
  (dimensions in millimeters – mm)



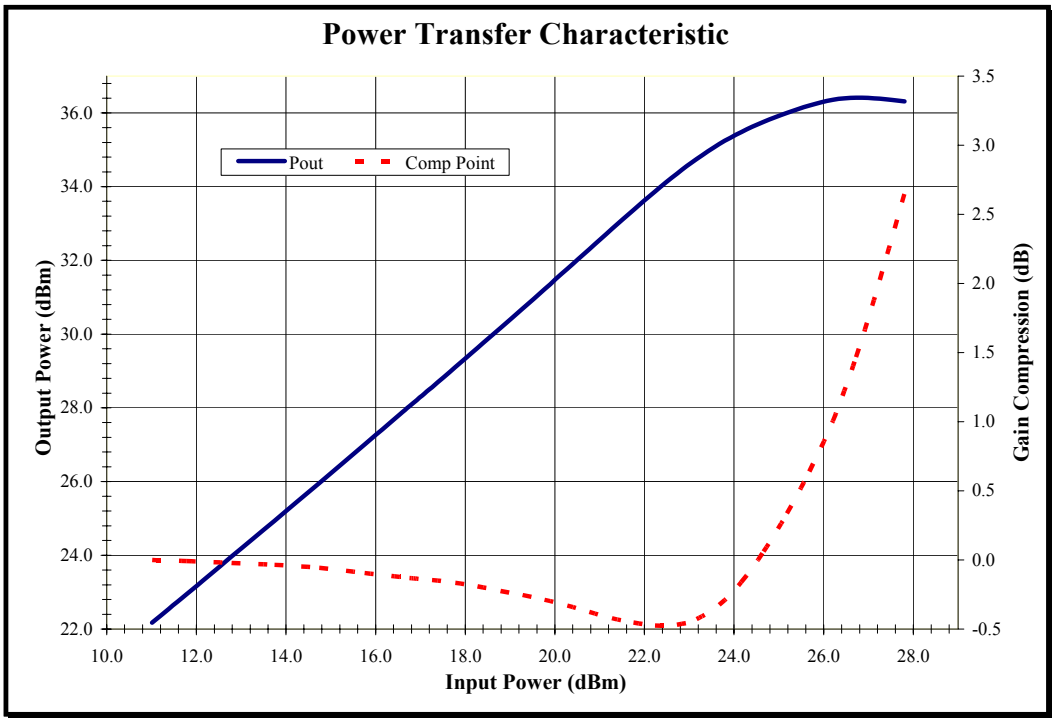
PACKAGE MARKING CODE

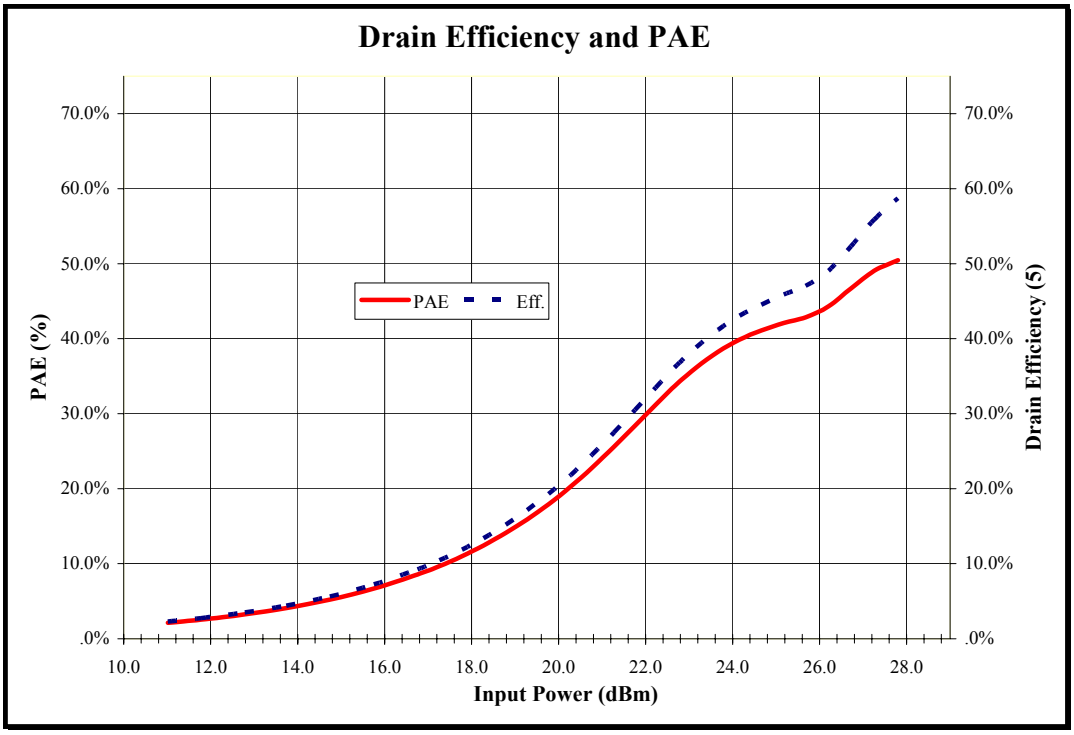
Example:

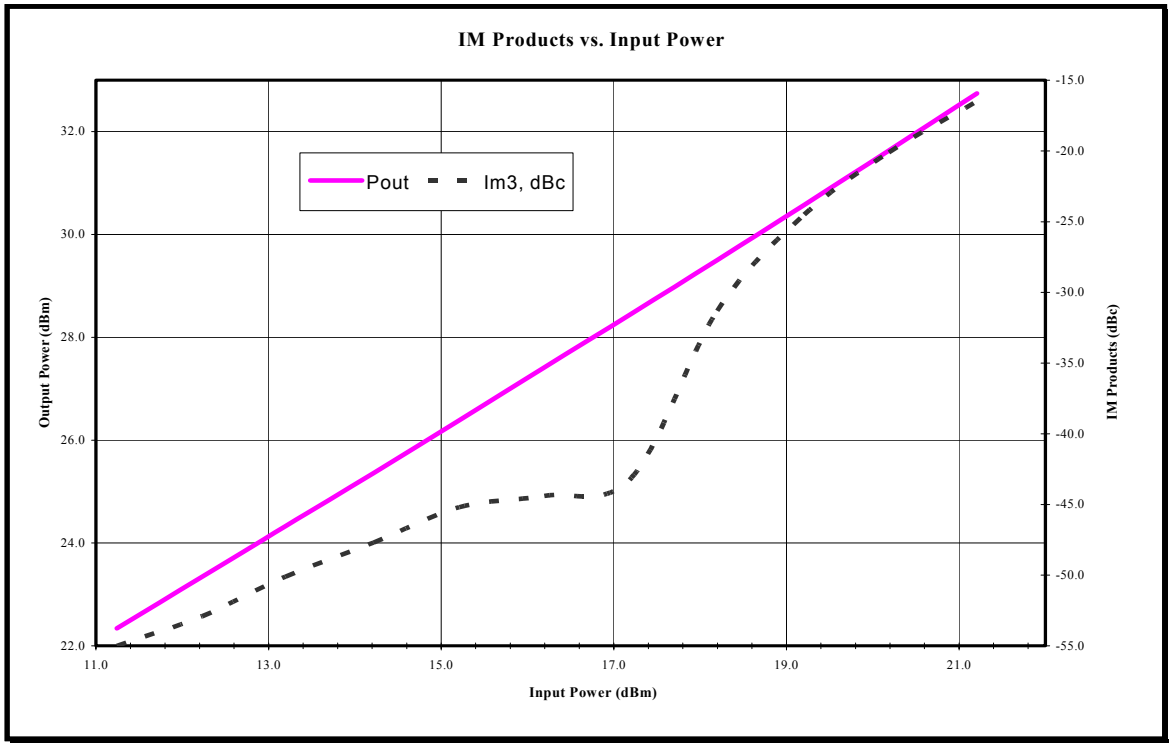
***f*1ZD**
P2F

***f* = Filtronic**
1ZD = Lot and Date Code
P2F = Status, Part Code, Part Type
Status: D=Development P = Production
Part Code denotes model (e.g. FPD4000AF)
Part Type: F = FET (pHEMT)

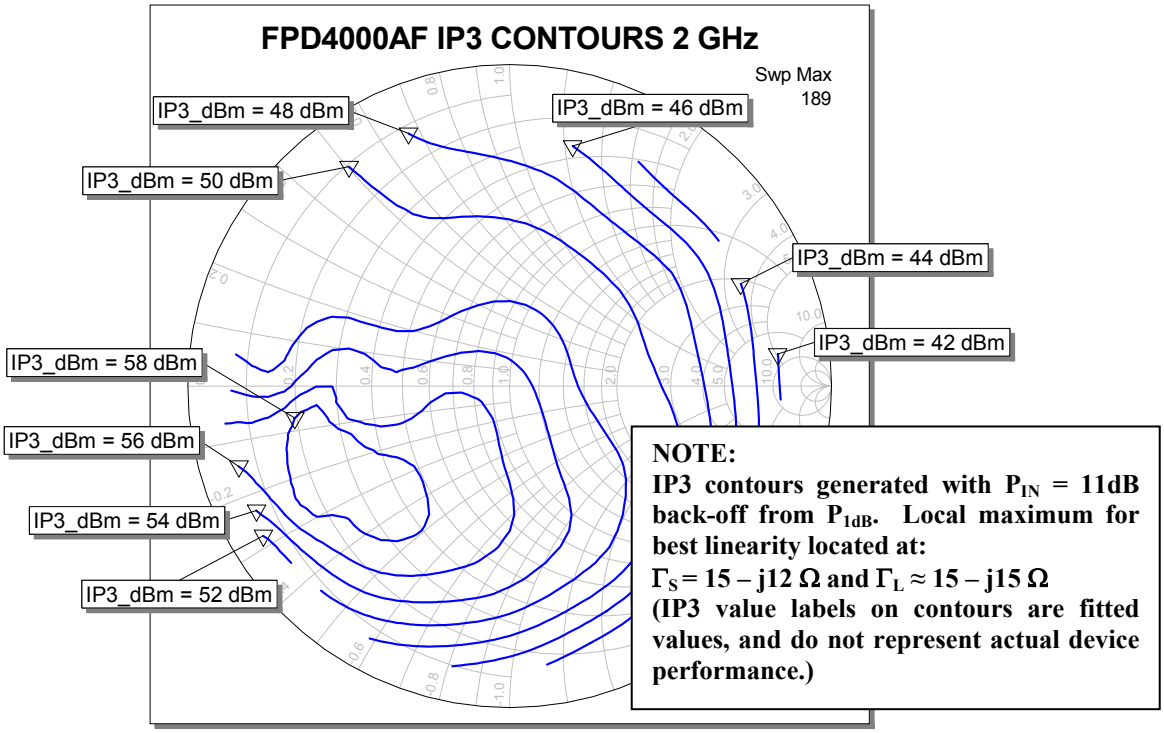
- TYPICAL RF PERFORMANCE (V_{DS} = 10V I_{DQ} = 720 mA f = 2000 MHz):

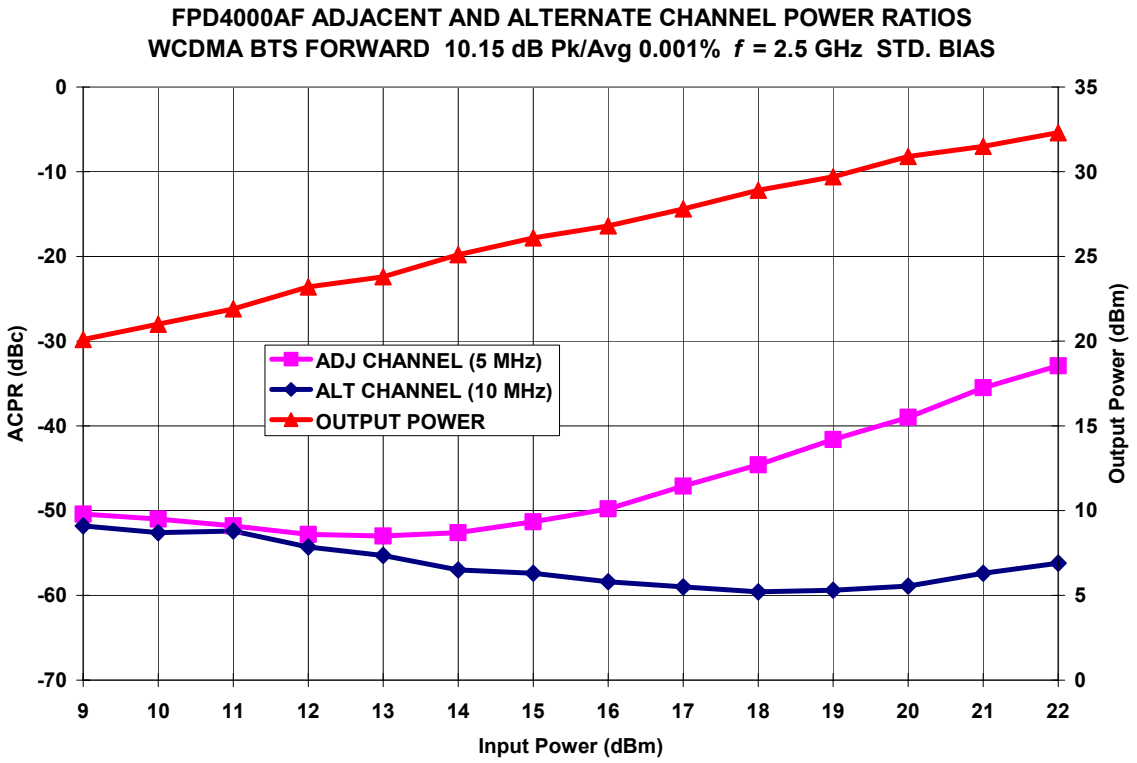




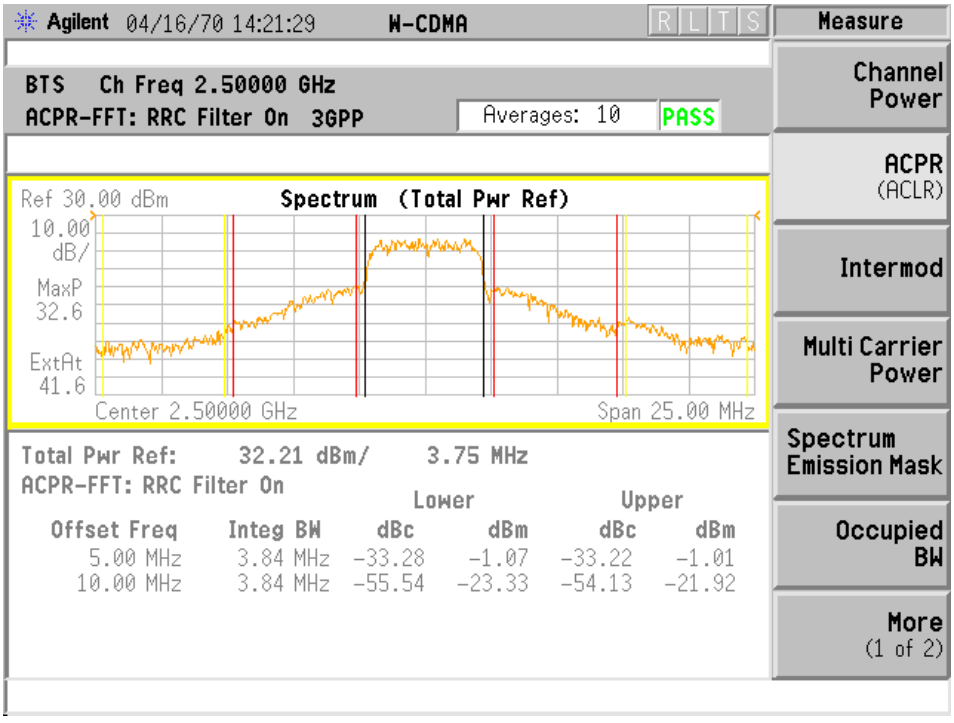


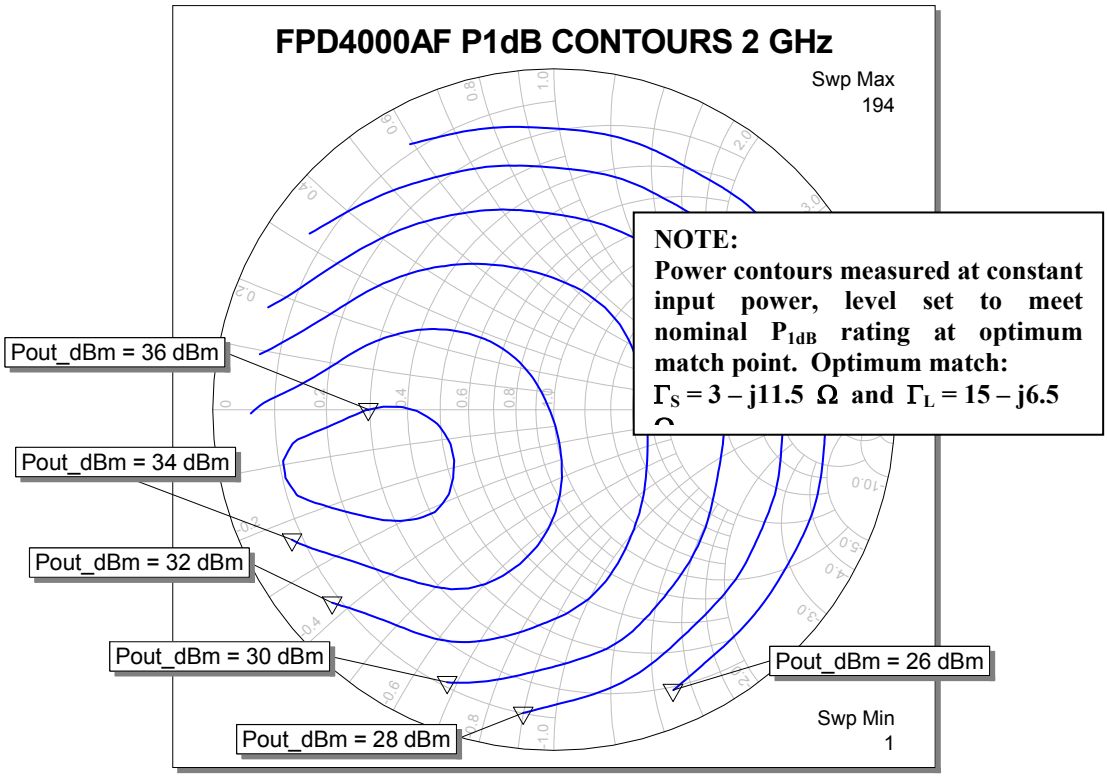
Note: Graph above shows Input and Output power as single carrier or single-tone levels.

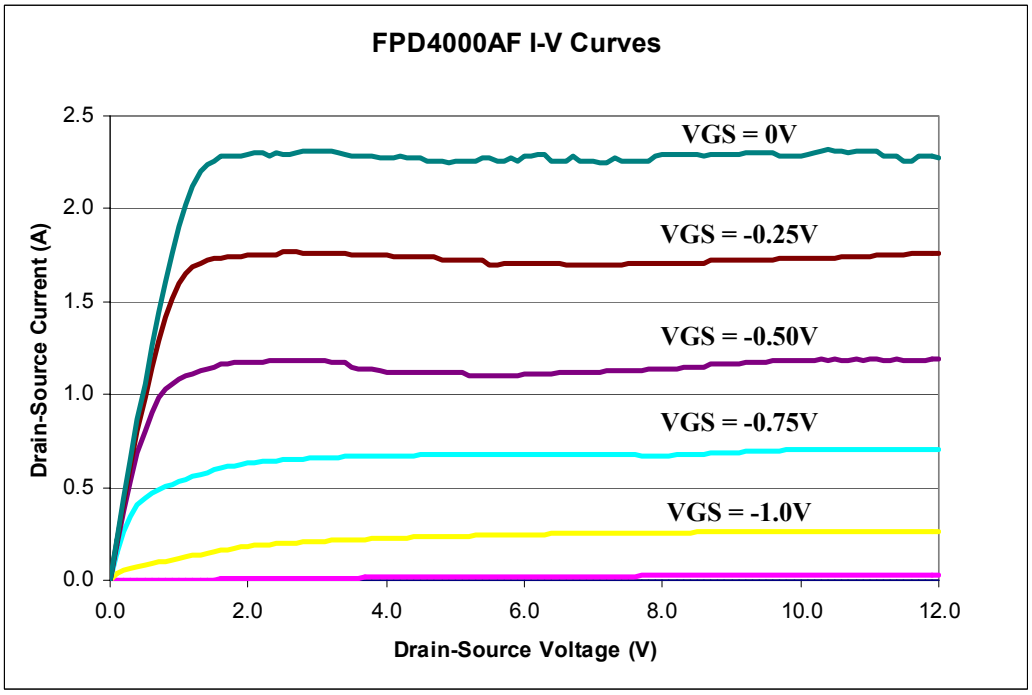




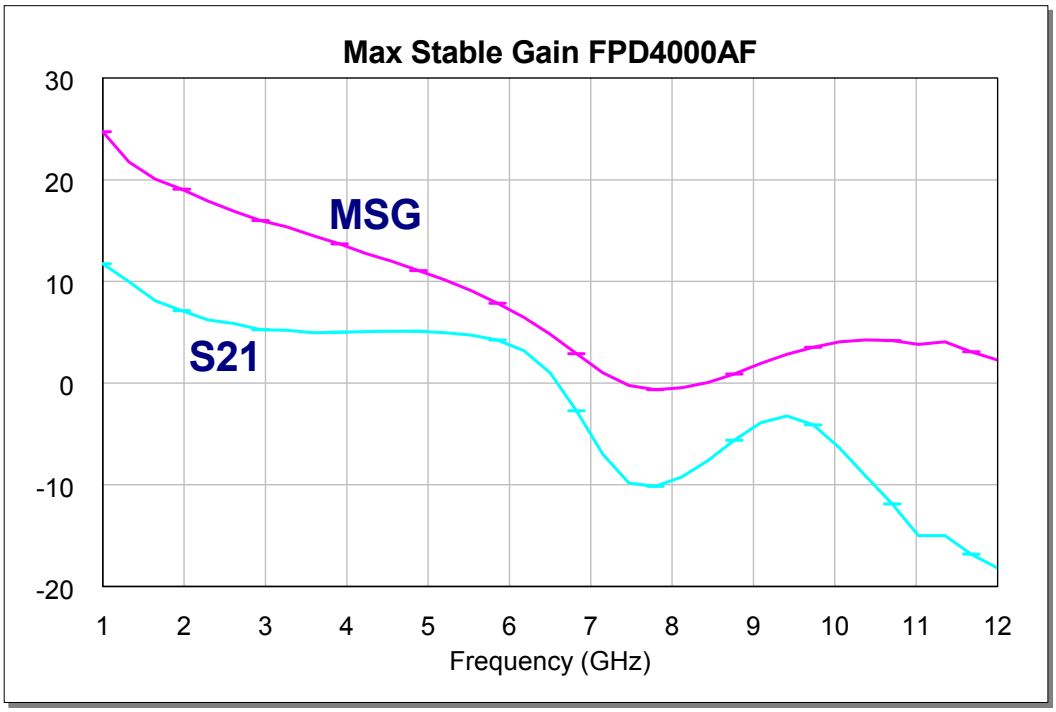
ACPR measurement at 4 dB back-off from P_{1dB} with WCDMA BTS Forward modulation:




FPD4000AF P1dB CONTOURS 2 GHz
Swp Max
194
NOTE:
Power contours measured at constant input power, level set to meet nominal P1dB rating at optimum match point. Optimum match:
ΓS = 3 – j11.5 Ω and ΓL = 15 – j6.5
Pout_dBm = 36 dBm
Pout_dBm = 34 dBm
Pout_dBm = 32 dBm
Pout_dBm = 30 dBm
Pout_dBm = 28 dBm
Pout_dBm = 26 dBm
Swp Min
1

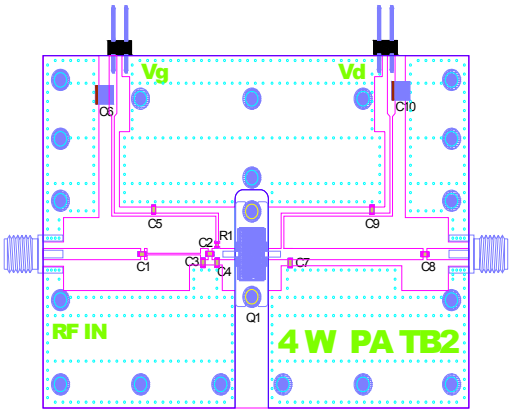

FPD4000AF I-V Curves
Drain-Source Current (A)
2.5
2.0
1.5
1.0
0.5
0.0
VGS = 0V
VGS = -0.25V
VGS = -0.50V
VGS = -0.75V
VGS = -1.0V
0.0
2.0
4.0
6.0
8.0
10.0
12.0
Drain-Source Voltage (V)

- RF PERFORMANCE OVER FREQUENCY:



Note: The FPD4000AF is suitable for applications up to 4 GHz.

- STANDARD EVALUATION BOARD (1.70-1.85 GHZ):



NOTE: AutoCAD™ drawing available on Website

Bill of Materials for Evaluation Board, FPD4000AF EV-BL-000026-002-A			
Designator	Part Number	Description	Quantity
C1	ATC600S0R9JW250	Capacitor, 0.9 pF, 0603, ATC 600, tol. ±5%	1
C2	ATC600S3R0JW250	Capacitor, 3.0 pF, 0603, ATC 600, tol. ±5%	1
C3	ATC600S1R8JW250	Capacitor, 1.8 pF, 0603, ATC 600, tol. ±5%	1
C4	ATC600S1R0JW250	Capacitor, 1.0 pF, 0603, ATC 600, tol. ±5%	1
C5	ATC600S330JW250	Capacitor, 33 pF, 0603, ATC 600, tol. ±5%	1
C6	T491B105M035AS7015	Capacitor, 1 μF, SMD-B, Kemet, tol. ±20%	1
C7	ATC600S1R5JW250	Capacitor, 1.5 pF, 0603, ATC 600, tol. ±5%	1
C8	ATC600S330JW250	Capacitor, 33 pF, 0603, ATC 600, tol. ±5%	1
C9	ATC600S330JW250	Capacitor, 33 pF, 0603, ATC 600, tol. ±5%	1
C10	T491B105M035AS7015	Capacitor, 1 μF, SMD-B, Kemet, tol. ±20%	1
R1	RCI-0603-10R1J	Resistor, 100 Ω, 0603, IMS, tol. ±5%	1
Q1	FPD4000AF	Packaged Discrete pHEMT, Filtronic	1
	PC-SP-000022-002	PCB, FPD4000AF Eval Board, 2 GHz	1
	142-0711-841	Connector, RF, SMA End Launch, Jack Assy, Johnson	2
	AMP-103185-2	Connector, DC, 0.100 on center, 0.025 sq. posts, Tyco	2
	TF-SP-000025	Test Fixture Base, Flange Mount Package, 2 GHz	1
		Screw, #2-56	20