# Power management, Dual-chip Bipolar Transistor

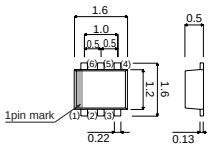
## EMF33

### ●Applications
Power management circuit

### ●Features
1) DTB513Z (digital transistor) and 2SK3019 (MOS FET) are housed independently in the EMT6 package.
2) Power switching circuit in a single package.
3) Mounting cost and area can be cut in half.

### ●Dimensions (Unit : mm)

**EMT6**




Each lead has same dimensions

Abbreviated symbol : F33

### ●Structure
Epitaxial Plannar Silicon Transistor

### ●Packaging specifications

| | | |
|---|---|---|
| Type | Package | Taping |
| | Code | T2R |
| | Basic ordering unit (pieces) | 8000 |
| EMF33 | | ◯ |

### ●Absolute maximum ratings (Ta=25°C)

<Tr1>

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | –12 | V |
| Input voltage | $V_{IN}$ | –10 to +5 | V |
| Collector current | $I_{C(max)}$ * | –500 | mA |

* Characteristics of built-in transistor.

<Tr2>

| Parameter | | Symbol | Limits | Unit |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | 30 | V |
| Gate-source voltage | | $V_{GSS}$ | ±20 | V |
| Drain current | Continous | $I_D$ | 100 | mA |
| | Pulsed | $I_{DP}$ * | 200 | mA |
| Reverse drain current | Continous | $I_{DR}$ | 100 | mA |
| | Pulsed | $I_{DRP}$ * | 200 | mA |

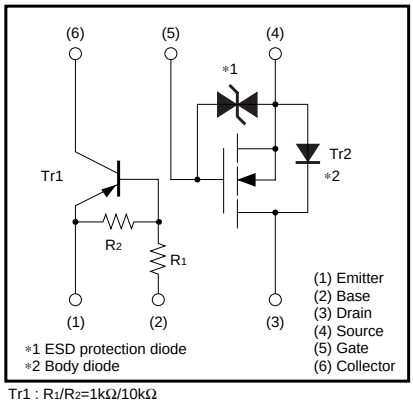
* PW≤10ms DUTY CYCLE≤50%

<Tr1, Tr2 in common>

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power dissipation | $P_D$ * | 150 | mW / TOTAL |
| | | 120 | mW / ELEMENT |
| Junction temperature | Tj | 150 | °C |
| Range of storage temperature | Tstg | –55 to +150 | °C |

* Each terminal mounted on a recommended land.

### ●Equivalent circuit




Tr1 : $R_1/R_2$=1kΩ/10kΩ
Tr2 : MOS FET

●**Electrical characteristics** (Ta=25°C)

<Tr1>

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input voltage | $V_{I(off)}$ | – | – | –0.3 | V | $V_{CC}$= –5V, $I_O$= –100µA |
| | $V_{I(on)}$ | –2.5 | – | – | V | $V_O$= –0.3V, $I_O$= –20mA |
| Output voltage | $V_{O(on)}$ | – | –60 | –300 | mV | $V_O$= –100mA, $I_I$= –5mA |
| Input current | $I_I$ | – | – | –6.4 | mA | $V_I$= –5V |
| Output current | $I_{O(off)}$ | – | – | –0.5 | uA | $V_{CC}$= –12V, $V_I$= 0V |
| DC current gain | $G_I$ | 140 | – | – | – | $V_O$= –5V, $I_O$= –100mA |
| Transition frequency | $f_T$ * | – | 260 | – | – | $V_{CE}$= –10V, $I_E$= 5mA, f=100MHz |
| Input resistance | R1 | 0.7 | 1 | 1.3 | kΩ | |
| Resistance ratio | R2/R1 | 8 | 10 | 12 | – | |

* Characteristics of built-in transistor.

<Tr2>

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Gate-source leakage | $I_{GSS}$ | – | – | ±1 | µA | $V_{GS}$= ±20V, $V_{DS}$=0V |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 30 | – | – | – | $I_D$= 10µA, $V_{GS}$=0A |
| Zero gate voltage drain current | $I_{DSS}$ | – | – | 1.0 | µA | $V_{DS}$= 30V, $V_{GS}$=0V |
| Gate-threshold voltage | $V_{GS(th)}$ | 0.8 | – | 1.5 | V | $V_{DS}$= 3V, $I_D$=100µA |
| Static drain-source on-resistance | $R_{DS(on)}$ | – | 5 | 8 | Ω | $I_D$= 10mA, $V_{GS}$= 4V |
| | | – | 7 | 13 | Ω | $I_D$= 1mA, $V_{GS}$= 2.5V |
| Forward transfer admittance | \| $Y_{fs}$ \| | 20 | – | – | ms | $V_{DS}$= 3V, $I_D$= 10mA |
| Input capacitance | $C_{iss}$ | – | 13 | – | pF | $V_{DS}$= 5V<br>$V_{GS}$= 0V<br>f=1MHz |
| Output capacitance | $C_{oss}$ | – | 9 | – | pF | |
| Reverse transfer capacitance | $C_{rss}$ | – | 4 | – | pF | |
| Turn-on delay time | $t_{d(on)}$ | – | 15 | – | ns | $I_D$= 10mA<br>$V_{DD}$≒ 5V<br>$V_{GS}$= 5V<br>$R_L$= 500Ω<br>$R_{GS}$= 10Ω |
| Rise time | $t_r$ | – | 35 | – | ns | |
| Turn-off delay time | $t_{d(off)}$ | – | 80 | – | ns | |
| Fall time | $t_f$ | – | 80 | – | ns | |

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