EM65565A

65 COM / 132
SEG STN LCD Driver

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
0.1	Initial version	2003/01/13
0.2	Added /RST ITO trace resistor and display off current	2003/06/18
0.3	Modified the VRS and VR pin description Modified the VREG rating	2003/09/17
0.4	Added mark appearance diagram	2003/10/03
0.5	Removed the thermal gradient description	2003/10/24
0.6	Modified the VRS No. of Pins 3 → 2	2003/12/16
0.7	Modified the Vreg min. & max. value	2004/09/09
0.8	Added Tray Information	2004/04/01
0.9	Added Test Pin description	2004/05/28
1.0	1. Added VREG Temperature coefficient 2. Added the recommended Type of Capacitor for the Application Circuit. 3. Modified the VREG rating	2005/06/06

1 General Description

The EM65565A is a 65 Common 132 Segment dot matrix *Liquid Crystal Display* (***LCD***) driver LSI, which can be connected directly to a microprocessor bus, and can select an 8-bit parallel or serial data input interface. The EM65565A IC contains 65×132 bits of *display data RAM* (***DDRAM***) and there is a one-to-one correspondence between the *LCD* panel pixels and the internal RAM bits.

The EM65565A IC can drive a 65×132 dot display, and the capacity of the display can be extended by master/slave structures between ICs. This device has minimal power consumption since no external operating clock is necessary for the *DDRAM* read/write operation. Furthermore, each IC has a built-in low-power *LCD* driver power supply, on-chip resistors for *LCD* driver power voltage adjustment and a display clock RC oscillator circuit, these and all the other features combined make the EM65565A IC suitable for lowest power display systems with the fewest components for high-performance portable devices.

2 Features

- Direct display of RAM data through the DDRAM
  RAM bit data:
  "0" : Illuminated "1" : Non-illuminated
- RAM capacity: 65×132 = 8,580 bits
- Display driver circuits: 65 common output and 132 segment outputs
- High-speed 8-bit MPU interface (80-series and 68-series) / Serial interfaces are supported
- Abundant command functions: display data Read/Write, display ON/OFF, status read, Normal/Reverse display mode, page address set, display start line set, column address set, display all points ON/OFF, LCD bias set, electronic volume, read-modify-write, segment driver direction select, power saver, static indicator, common output status select, V0 voltage regulation internal resistor ratio set.
- Built-in Static drive circuit for indicators
- Built-in Low-power LCD power supply circuit
- Built-in Booster circuit, with Boost ratios of two/three/four/five times, where the step-up voltage reference power supply can be input externally
- Built-in High-accuracy voltage adjustment circuit (external input)
- Built-in V0 voltage regulator resistors
- Built-in V1 to V4 voltage divider resistors
- Built-in electronic volume function

- Voltage follower
- Internal RC oscillator circuit (external clock can also be input)
- Extreme low power consumption
- Power supply, operable on the low 1.8V
  - Logic power supply: VDD – VSS = 2.4V to 3.3V
  - Boost reference voltage: VCI = 2.4V to 3.3V
  - LCD driver power supply: VLCD = V0 – VSS = 4.5V to 12.0V
- Non-resistant to light or radiation
- Package (Ordering information)

Part Number	Package	Description	Package Information
EM65565AAGH	Gold bumped chip	NA	Page 5

Note: The EM65565A series has the following sub-codes, depending on their shapes.
H: Bare chip (Aluminum pad without bump); **GH**: Gold bumped chip
F: COF package; **T**: TAB (TCP) package

Example:

EM65565AAGH → EM65565A: Elan number; A: Package Version; GH: Gold bumped chip

3 Pin Configuration

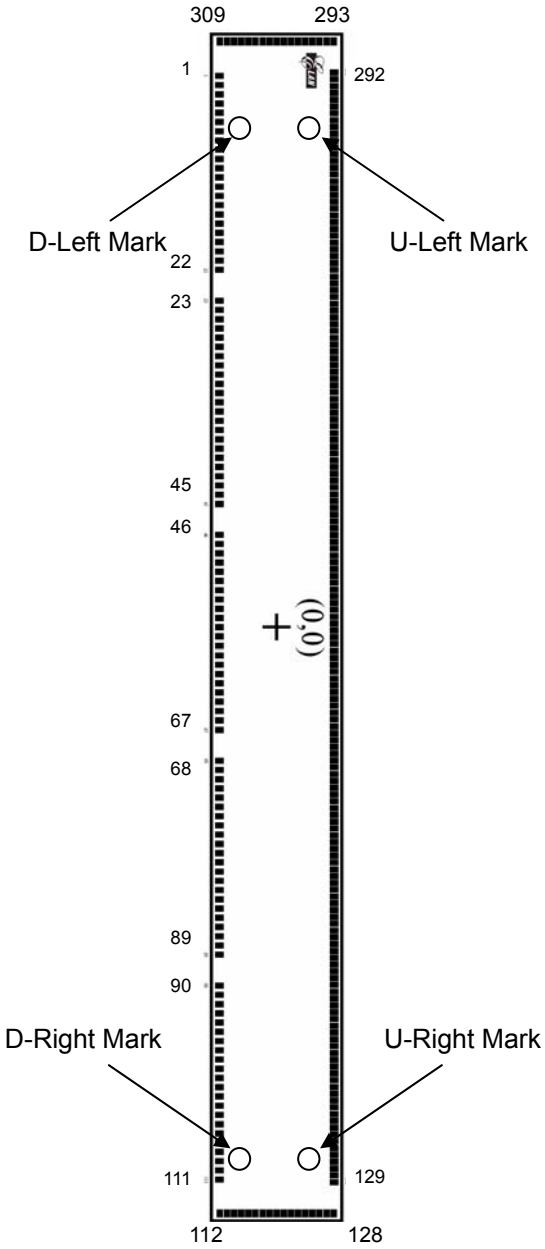


Fig. 1 Pin Configuration

NOTE

With the Elan logo at the upper left corner, Pin 1 is at the bottom left corner, viewed lengthwise.

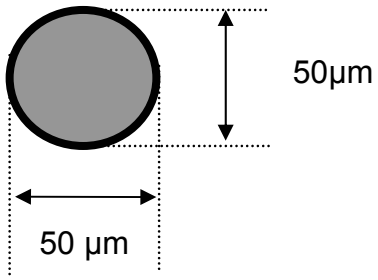
3.1 Pin Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	10570	1210	
Bump Size	1 ~ 309	43	60	
Pad Pitch	60 (min.)			μm
Die thickness (excluding bumps)	525 ± 25			
Bump Height	All Pad 17 ± 3 (within die)			
Minimum Bump Gap	17			
Coordinate Origin	Chip center			

3.2 Mark Dimensions

Mark	Coordinate (X,Y)	Mark	Coordinate (X,Y)
U-Left	-4714.25 , 124.55	U-Right	4544.1 , 124.55
D-Left	-4714.25 , -215.4	D-Right	4544.1 , -215.4

Mark Appearance



Pad Coordinates Table

Pin No	Pad Name	Coordinate (X,Y)	Pin No	Pad Name	Coordinate (X,Y)
1	NC1	-4861.2 , -485.0	51	V_{SS}	-404.4 , -485.0
2	NC2	-4779.7 , -485.0	52	V_{SS}	-322.9 , -485.0
3	NC3	-4698.2 , -485.0	53	V_{SS}	-241.4 , -485.0
4	NC4	-4616.7 , -485.0	54	V_{SS}	-159.9 , -485.0
5	NC5	-4535.2 , -485.0	55	V_{SS}	-78.4 , -485.0
6	TEST1	-4453.7 , -485.0	56	V_{SS}	3.1 , -485.0
7	TEST2	-4372.2 , -485.0	57	V_{OUT}	84.6 , -485.0
8	TEST3	-4290.7 , -485.0	58	V_{OUT}	166.1 , -485.0
9	FRS	-4209.2 , -485.0	59	CAP4+	247.6 , -485.0
10	FR	-4127.7 , -485.0	60	CAP4+	329.1 , -485.0
11	FR	-4046.2 , -485.0	61	CAP4+	410.6 , -485.0
12	DCLK	-3964.7 , -485.0	62	CAP3+	492.1 , -485.0
13	/BCT	-3883.2 , -485.0	63	CAP3+	573.6 , -485.0
14	V_{SS}	-3801.7 , -485.0	64	CAP3+	655.1 , -485.0
15	V_{SS}	-3720.2 , -485.0	65	CAP1-	736.6 , -485.0
16	/CS1	-3638.7 , -485.0	66	CAP1-	818.1 , -485.0
17	CS2	-3557.2 , -485.0	67	CAP1-	899.6 , -485.0
18	V_{DD}	-3475.7 , -485.0	68	CAP1+	1172.0 , -485.0
19	/RST	-3394.2 , -485.0	69	CAP1+	1253.5 , -485.0
20	D/I	-3312.7 , -485.0	70	CAP1+	1335.0 , -485.0
21	V_{SS}	-3231.2 , -485.0	71	CAP2+	1416.5 , -485.0
22	/WR	-3149.7 , -485.0	72	CAP2+	1498.0 , -485.0
23	/RD	-2877.3 , -485.0	73	CAP2+	1579.5 , -485.0
24	V_{DD}	-2795.8 , -485.0	74	CAP2-	1661.0 , -485.0
25	D0	-2714.3 , -485.0	75	CAP2-	1742.5 , -485.0
26	D1	-2632.8 , -485.0	76	CAP2-	1824.0 , -485.0
27	D2	-2551.3 , -485.0	77	V_{DD}	1905.5 , -485.0
28	D3	-2469.8 , -485.0	78	V_{RS}	1987.0 , -485.0
29	D4	-2388.3 , -485.0	79	V_{RS}	2068.5 , -485.0
30	D5	-2306.8 , -485.0	80	V_{SS}	2150.0 , -485.0
31	D6	-2225.3 , -485.0	81	V_1	2231.5 , -485.0
32	D7	-2143.8 , -485.0	82	V_1	2313.0 , -485.0
33	V_{SS}	-2062.3 , -485.0	83	V_1	2394.5 , -485.0
34	V_{DD}	-1980.8 , -485.0	84	V_2	2476.0 , -485.0
35	V_{SS}	-1899.3 , -485.0	85	V_2	2557.5 , -485.0
36	V_{DD}	-1817.8 , -485.0	86	V_2	2639.0 , -485.0
37	V_{DD}	-1736.3 , -485.0	87	V_3	2720.5 , -485.0
38	V_{DD}	-1654.8 , -485.0	88	V_3	2802.0 , -485.0
39	V_{DD}	-1573.3 , -485.0	89	V_3	2883.5 , -485.0
40	V_{DD}	-1491.8 , -485.0	90	V_4	3155.9 , -485.0
41	V_{DD}	-1410.3 , -485.0	91	V_4	3237.4 , -485.0
42	V_{DD}	-1328.8 , -485.0	92	V_4	3318.9 , -485.0
43	V_{CI}	-1247.3 , -485.0	93	V_0	3400.4 , -485.0
44	V_{CI}	-1165.8 , -485.0	94	V_0	3481.9 , -485.0
45	V_{CI}	-1084.3 , -485.0	95	V_0	3563.4 , -485.0
46	V_{SS}	-811.9 , -485.0	96	V_R	3644.9 , -485.0
47	V_{SS}	-730.4 , -485.0	97	V_R	3726.4 , -485.0
48	V_{SS}	-648.9 , -485.0	98	V_R	3807.9 , -485.0
49	V_{SS}	-567.4 , -485.0	99	V_{SS}	3889.4 , -485.0
50	V_{SS}	-485.9 , -485.0	100	V_{SS}	3970.9 , -485.0

Pin No	Pad Name	Coordinate (X,Y)	Pin No	Pad Name	Coordinate (X,Y)
101	V_{DD}	4052.4 , -485.0	151	SEG6	3569.9 , 485.0
102	M/S	4133.9 , -485.0	152	SEG7	3509.9 , 485.0
103	DCLKS	4215.4 , -485.0	153	SEG8	3449.9 , 485.0
104	V_{SS}	4296.9 , -485.0	154	SEG9	3389.9 , 485.0
105	MPUS	4378.4 , -485.0	155	SEG10	3329.9 , 485.0
106	P/S	4459.9 , -485.0	156	SEG11	3269.9 , 485.0
107	V_{DD}	4541.4 , -485.0	157	SEG12	3209.9 , 485.0
108	/PCT	4622.9 , -485.0	158	SEG13	3149.9 , 485.0
109	V_{SS}	4704.4 , -485.0	159	SEG14	3089.9 , 485.0
110	IRS	4785.9 , -485.0	160	SEG15	3029.9 , 485.0
111	V_{DD}	4867.4 , -485.0	161	SEG16	2969.9 , 485.0
112	COM31	5165.0 , -480.0	162	SEG17	2909.9 , 485.0
113	COM30	5165.0 , -420.0	163	SEG18	2849.9 , 485.0
114	COM29	5165.0 , -360.0	164	SEG19	2789.9 , 485.0
115	COM28	5165.0 , -300.0	165	SEG20	2729.9 , 485.0
116	COM27	5165.0 , -240.0	166	SEG21	2669.9 , 485.0
117	COM26	5165.0 , -180.0	167	SEG22	2609.9 , 485.0
118	COM25	5165.0 , -120.0	168	SEG23	2549.9 , 485.0
119	COM24	5165.0 , -60.0	169	SEG24	2489.9 , 485.0
120	COM23	5165.0 , 0.0	170	SEG25	2429.9 , 485.0
121	COM22	5165.0 , 60.0	171	SEG26	2369.9 , 485.0
122	COM21	5165.0 , 120.0	172	SEG27	2309.9 , 485.0
123	COM20	5165.0 , 180.0	173	SEG28	2249.9 , 485.0
124	COM19	5165.0 , 240.0	174	SEG29	2189.9 , 485.0
125	COM18	5165.0 , 300.0	175	SEG30	2129.9 , 485.0
126	COM17	5165.0 , 360.0	176	SEG31	2069.9 , 485.0
127	COM16	5165.0 , 420.0	177	SEG32	2009.9 , 485.0
128	COM15	5165.0 , 480.0	178	SEG33	1949.9 , 485.0
129	COM14	4889.9 , 485.0	179	SEG34	1889.9 , 485.0
130	COM13	4829.9 , 485.0	180	SEG35	1829.9 , 485.0
131	COM12	4769.9 , 485.0	181	SEG36	1769.9 , 485.0
132	COM11	4709.9 , 485.0	182	SEG37	1709.9 , 485.0
133	COM10	4649.9 , 485.0	183	SEG38	1649.9 , 485.0
134	COM9	4589.9 , 485.0	184	SEG39	1589.9 , 485.0
135	COM8	4529.9 , 485.0	185	SEG40	1529.9 , 485.0
136	COM7	4469.9 , 485.0	186	SEG41	1469.9 , 485.0
137	COM6	4409.9 , 485.0	187	SEG42	1409.9 , 485.0
138	COM5	4349.9 , 485.0	188	SEG43	1349.9 , 485.0
139	COM4	4289.9 , 485.0	189	SEG44	1289.9 , 485.0
140	COM3	4229.9 , 485.0	190	SEG45	1229.9 , 485.0
141	COM2	4169.9 , 485.0	191	SEG46	1169.9 , 485.0
142	COM1	4109.9 , 485.0	192	SEG47	1109.9 , 485.0
143	COM0	4049.9 , 485.0	193	SEG48	1049.9 , 485.0
144	COMS	3989.9 , 485.0	194	SEG49	989.9 , 485.0
145	SEG0	3929.9 , 485.0	195	SEG50	929.9 , 485.0
146	SEG1	3869.9 , 485.0	196	SEG51	869.9 , 485.0
147	SEG2	3809.9 , 485.0	197	SEG52	809.9 , 485.0
148	SEG3	3749.9 , 485.0	198	SEG53	749.9 , 485.0
149	SEG4	3689.9 , 485.0	199	SEG54	689.9 , 485.0
150	SEG5	3629.9 , 485.0	200	SEG55	629.9 , 485.0

Pin No	Pad Name	Coordinate (X,Y)	Pin No	Pad Name	Coordinate (X,Y)
201	SEG56	569.9 , 485.0	251	SEG106	-2430.1 , 485.0
202	SEG57	509.9 , 485.0	252	SEG107	-2490.1 , 485.0
203	SEG58	449.9 , 485.0	253	SEG108	-2550.1 , 485.0
204	SEG59	389.9 , 485.0	254	SEG109	-2610.1 , 485.0
205	SEG60	329.9 , 485.0	255	SEG110	-2670.1 , 485.0
206	SEG61	269.9 , 485.0	256	SEG111	-2730.1 , 485.0
207	SEG62	209.9 , 485.0	257	SEG112	-2790.1 , 485.0
208	SEG63	149.9 , 485.0	258	SEG113	-2850.1 , 485.0
209	SEG64	89.9 , 485.0	259	SEG114	-2910.1 , 485.0
210	SEG65	29.9 , 485.0	260	SEG115	-2970.1 , 485.0
211	SEG66	-30.1 , 485.0	261	SEG116	-3030.1 , 485.0
212	SEG67	-90.1 , 485.0	262	SEG117	-3090.1 , 485.0
213	SEG68	-150.1 , 485.0	263	SEG118	-3150.1 , 485.0
214	SEG69	-210.1 , 485.0	264	SEG119	-3210.1 , 485.0
215	SEG70	-270.1 , 485.0	265	SEG120	-3270.1 , 485.0
216	SEG71	-330.1 , 485.0	266	SEG121	-3330.1 , 485.0
217	SEG72	-390.1 , 485.0	267	SEG122	-3390.1 , 485.0
218	SEG73	-450.1 , 485.0	268	SEG123	-3450.1 , 485.0
219	SEG74	-510.1 , 485.0	269	SEG124	-3510.1 , 485.0
220	SEG75	-570.1 , 485.0	270	SEG125	-3570.1 , 485.0
221	SEG76	-630.1 , 485.0	271	SEG126	-3630.1 , 485.0
222	SEG77	-690.1 , 485.0	272	SEG127	-3690.1 , 485.0
223	SEG78	-750.1 , 485.0	273	SEG128	-3750.1 , 485.0
224	SEG79	-810.1 , 485.0	274	SEG129	-3810.1 , 485.0
225	SEG80	-870.1 , 485.0	275	SEG130	-3870.1 , 485.0
226	SEG81	-930.1 , 485.0	276	SEG131	-3930.1 , 485.0
227	SEG82	-990.1 , 485.0	277	COM32	-3990.1 , 485.0
228	SEG83	-1050.1 , 485.0	278	COM33	-4050.1 , 485.0
229	SEG84	-1110.1 , 485.0	279	COM34	-4110.1 , 485.0
230	SEG85	-1170.1 , 485.0	280	COM35	-4170.1 , 485.0
231	SEG86	-1230.1 , 485.0	281	COM36	-4230.1 , 485.0
232	SEG87	-1290.1 , 485.0	282	COM37	-4290.1 , 485.0
233	SEG88	-1350.1 , 485.0	283	COM38	-4350.1 , 485.0
234	SEG89	-1410.1 , 485.0	284	COM39	-4410.1 , 485.0
235	SEG90	-1470.1 , 485.0	285	COM40	-4470.1 , 485.0
236	SEG91	-1530.1 , 485.0	286	COM41	-4530.1 , 485.0
237	SEG92	-1590.1 , 485.0	287	COM42	-4590.1 , 485.0
238	SEG93	-1650.1 , 485.0	288	COM43	-4650.1 , 485.0
239	SEG94	-1710.1 , 485.0	289	COM44	-4710.1 , 485.0
240	SEG95	-1770.1 , 485.0	290	COM45	-4770.1 , 485.0
241	SEG96	-1830.1 , 485.0	291	COM46	-4830.1 , 485.0
242	SEG97	-1890.1 , 485.0	292	COM47	-4890.1 , 485.0
243	SEG98	-1950.1 , 485.0	293	COM48	-5165.0 , 480.0
244	SEG99	-2010.1 , 485.0	294	COM49	-5165.0 , 420.0
245	SEG100	-2070.1 , 485.0	295	COM50	-5165.0 , 360.0
246	SEG101	-2130.1 , 485.0	296	COM51	-5165.0 , 300.0
247	SEG102	-2190.1 , 485.0	297	COM52	-5165.0 , 240.0
248	SEG103	-2250.1 , 485.0	298	COM53	-5165.0 , 180.0
249	SEG104	-2310.1 , 485.0	299	COM54	-5165.0 , 120.0
250	SEG105	-2370.1 , 485.0	300	COM55	-5165.0 , 60.0

Pin No	Pad Name	Coordinate (X,Y)	Pin No	Pad Name	Coordinate (X,Y)
301	COM56	-5165.0 , 0.0			
302	COM57	-5165.0 , -60.0			
303	COM58	-5165.0 , -120.0			
304	COM59	-5165.0 , -180.0			
305	COM60	-5165.0 , -240.0			
306	COM61	-5165.0 , -300.0			
307	COM62	-5165.0 , -360.0			
308	COM63	-5165.0 , -420.0			
309	COMS	-5165.0 , -480.0			

4 Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>V_{DD}</td><td>–</td><td>Power supply shared with the MPU terminal V_{CC}</td></tr>
<tr><td>V_{SS}</td><td>–</td><td>Power supply, 0V terminal connected to the system GND</td></tr>
<tr><td>V_{CI}</td><td>I</td><td>Reference power supply for the step-up voltage circuit for the liquid crystal drive.</td></tr>
<tr><td>V_{RS}</td><td>I</td><td>Externally input V_{REG} power supply for the LCD power supply voltage regulator.
If an internal voltage regulator is used, V_{RS} must be floating.</td></tr>
<tr><td>V_0
V_1
V_2
V_3
V_4</td><td>I/O</td><td>Multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divider or through changing the impedance using an Op. Amp. Voltage levels are determined based on V_0, and must maintain the relative magnitudes shown below.
$V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$
Master operation: When the power supply turns ON, the internal power supply circuits generate the V_1 to V_4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table>
<tr><th></th><th>1/9 bias</th><th>1/7 bias</th></tr>
<tr><td>V_1</td><td>$8/9 \times V_0$</td><td>$6/7 \times V_0$</td></tr>
<tr><td>V_2</td><td>$7/9 \times V_0$</td><td>$5/7 \times V_0$</td></tr>
<tr><td>V_3</td><td>$2/9 \times V_0$</td><td>$2/7 \times V_0$</td></tr>
<tr><td>V_4</td><td>$1/9 \times V_0$</td><td>$1/7 \times V_0$</td></tr>
</table></td></tr>
<tr><td>CAP1+</td><td>O</td><td>Capacitor 1 positive connection pin for the voltage converter</td></tr>
<tr><td>CAP1-</td><td>O</td><td>Capacitor 1 negative connection pin for the voltage converter</td></tr>
<tr><td>CAP2+</td><td>O</td><td>Capacitor 2 positive connection pin for the voltage converter</td></tr>
<tr><td>CAP2-</td><td>O</td><td>Capacitor 2 negative connection pin for the voltage converter</td></tr>
<tr><td>CAP3+</td><td>O</td><td>Capacitor 3 positive connection pin for the voltage converter</td></tr>
<tr><td>CAP4+</td><td>O</td><td>Capacitor 4 positive connection pin for the voltage converter</td></tr>
<tr><td>V_{OUT}</td><td>I/O</td><td>DC/DC voltage converter input/output pin. Connect a capacitor between this terminal and V_{SS}</td></tr>
<tr><td>V_R</td><td>O</td><td>Output voltage regulator terminal. This is only enabled (IRS = “L”) when the V_0 voltage regulator internal resistor is not used.
When the V_0 voltage regulator internal resistor is used (IRS = “H”), this pin must be floating.</td></tr>
<tr><td>D7 to D0</td><td>I/O</td><td>8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When chip select is inactive, D0 to D7 are set to high impedance.
When serial interface is selected (P/S = “L”), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>D/I</td><td>I</td><td>Determines whether the data bits are data or instruction (command).
<table>
<tr><th>D/I</th><th>D0 to D7</th></tr>
<tr><td>H</td><td>Display data</td></tr>
<tr><td>L</td><td>Instruction (Command)</td></tr>
</table></td></tr>
<tr><td>/RST</td><td>I</td><td>When /RST is set to “L,” the settings are initialized.</td></tr>
<tr><td>/CS1
CS2</td><td>I</td><td>Chip select signal. When /CS1 = “L” and CS2 = “H,” then the chip select CS2 becomes active, and data/command I/O is enabled.</td></tr>
<tr><td>/RD
(E)</td><td>I</td><td>Enable clock signal input for the 68-series MPU, active high.
Active low input pin for the 80-series MPU /RD signal</td></tr>
<tr><td>/WR
(R/W)</td><td>I</td><td>Read/Write control signal with 68-series MPU.
R/W=”H”: Read
R/W=”L”: Write
Active low input pin for the 80 series MPU /WR signal.</td></tr>
<tr><td>MPUS</td><td>I</td><td>MPU interface switch terminal.
MPUS = ”H”: 68-series MPU interface
MPUS = ”L”: 80-series MPU interface</td></tr>
<tr><td>P/S</td><td>I</td><td>Selects whether Parallel or Serial data input interface.
P/S = “H”: Parallel data input interface
P/S = “L”: Serial data input interface
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>D/I</td><td>D0 to D7</td><td>/RD, /WR</td><td></td></tr>
<tr><td>L</td><td>D/I</td><td>D7 (SI)</td><td>Write only</td><td>D6 (SCL)</td></tr>
</table>
When P/S = “L”, D0 to D5 are HZ. D0 to D5 may be “H”, “L” or Open.
RD (E) and WR (P/W) are fixed to either “H” or “L”.
With serial data input, RAM display data reading is not supported.</td></tr>
<tr><td>DCLKS</td><td>I</td><td>Terminal used to select whether to enable or disable the display clock internal oscillator circuit.
DCLKS = “H”: Internal oscillator circuit is enabled
DCLKS = “L”: Internal oscillator circuit is disabled (requires external input)
When DCLKS = “L”, input the display clock through the DCLK terminal.</td></tr>
<tr><td>M/S</td><td>I</td><td>M/S = “H”: Master operation
M/S = “L”: Slave operation
The following is true, depending on the M/S and DCLKS status:
<table>
<tr><th>M/S</th><th>DCLKS</th><th>Oscillator circuit</th><th>Power Supply Circuit</th><th>DCLK</th><th>FR</th><th>FRS</th><th>/BCT</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enable</td><td>Enable</td><td>O</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td>L</td><td>Disable</td><td>Enable</td><td>I</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>Disable</td><td>Disable</td><td>I</td><td>I</td><td>O</td><td>I</td></tr>
<tr><td>L</td><td>Disable</td><td>Disable</td><td>I</td><td>I</td><td>O</td><td>I</td></tr>
</table>
O : Output I : Input</td></tr>
<tr><td>DCLK</td><td>I/O</td><td>Display clock input terminal.
The following is true depending on the M/S and DCLKS status.
<table>
<tr><th>M/S</th><th>DCLKS</th><th>DCLK</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Output</td></tr>
<tr><td>L</td><td>Input</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>Input</td></tr>
<tr><td>L</td><td>Input</td></tr>
</table>
When the EM65565A chips are used in master/slave mode, the various DCLK terminals must be connected.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>FR</td><td>I/O</td><td>Liquid crystal alternating current signal I/O terminal.
M/S = “H” : Output
M/S = “L” : Input
When the EM65565A Series IC is used in master/slave mode, the various FR terminals must be connected.</td></tr>
<tr><td>/BCT</td><td>I/O</td><td>LCD blanking control terminal.
M/S = “H” : Output, M/S = “L” : Input
When the EM65565A chip is used in master/slave mode, the various /BCT terminals must be connected.</td></tr>
<tr><td>FRS</td><td>O</td><td>Output terminal for the static drive.
This terminal is only enabled when the static indicator display is ON in master operation mode, and is used in conjunction with the FR terminal.</td></tr>
<tr><td>IRS</td><td>I</td><td>Terminal used to select the resistors for the V0 voltage level adjustment.
IRS = “H” : Use the internal resistors
IRS = “L” : Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.
This pin is enabled only when the master operation mode is selected.
It is fixed to either “H” or “L” when the slave operation mode is selected.</td></tr>
<tr><td>/PCT</td><td>I</td><td>Power control terminal for the liquid crystal drive power supply circuit.
/PCT = “H” : Normal mode
/PCT = “L” : High power mode
This pin is enabled only when the master operation mode is selected.
It is fixed to either “H” or “L” when the slave operation mode is selected.</td></tr>
<tr><td>SEG0
to
SEG131</td><td>O</td><td>Liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from V_0, V_2, V_3, and V_{SS}.
<table>
<tr><th>RAM DATA</th><th>FR</th><th colspan="2">Output Voltage</th></tr>
<tr><td></td><td></td><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>H</td><td>H</td><td>V_0</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>V_0</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td>Power Save & Display OFF</td><td>--</td><td colspan="2">V_{SS}</td></tr>
</table></td></tr>
<tr><td>COM 0
to
COM 63</td><td>O</td><td>LCD common drive outputs.
Through a combination of the contents of the scan data and with the FR signal, a single level is selected from V_0, V_1, V_4, and V_{SS}.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td>V_0</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
<tr><td>Power Save</td><td>--</td><td>V_{SS}</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>Common output terminal for the indicator. This terminal outputs the same signal.
Leave this open if it is not used.
When in master/slave mode, the same signal is output by both master and slave.</td></tr>
<tr><td>TEST1~3</td><td>I/O</td><td>For IC testing, should be floating</td></tr>
</table>

5 Block Diagram

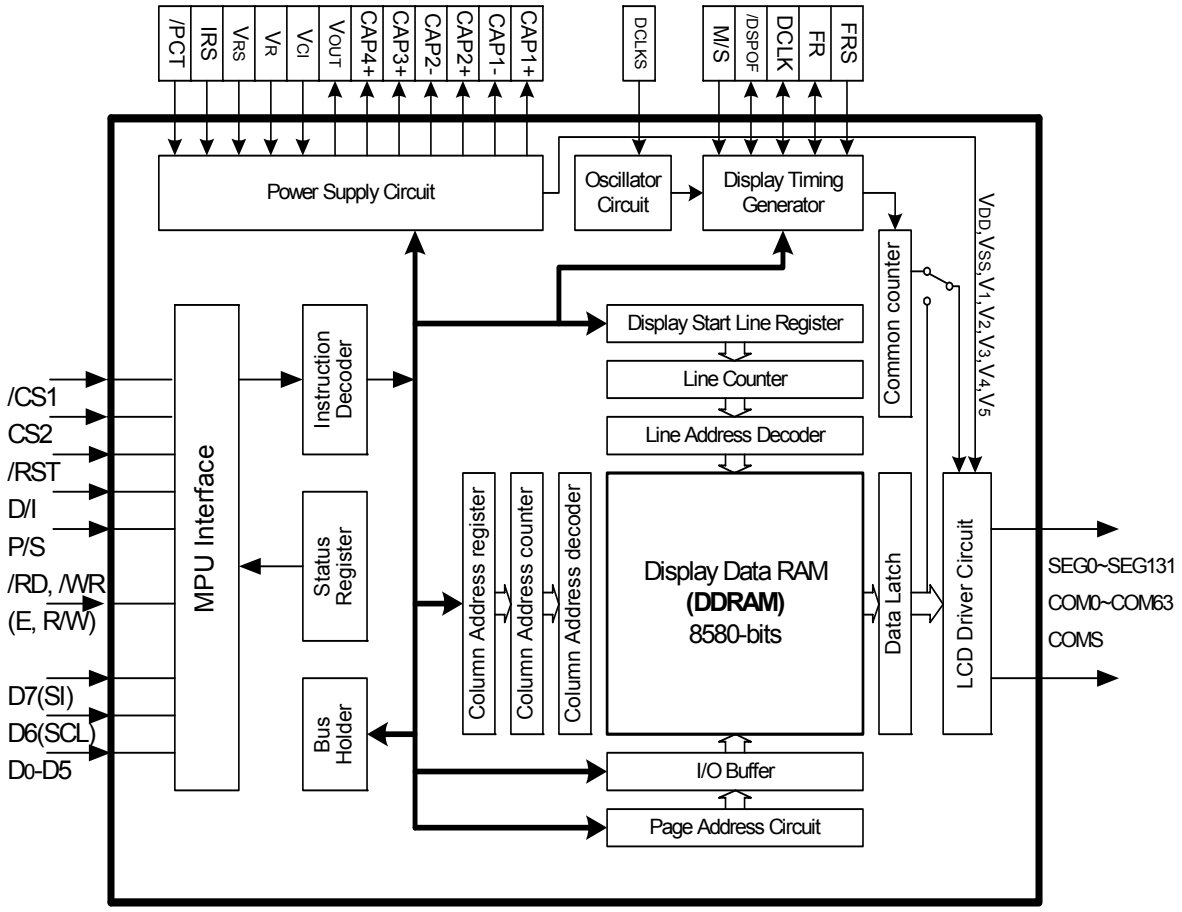


Figure 1 System Block Diagram

6 Functional Description

6.1 MPU Interface

6.1.1 Selecting the Interface Type

The EM65565A IC can be operated with either parallel interface or serial interface as selected by the P/S terminal polarity to the "H" or "L", as shown in following table:

PS	/CS1	CS2	D/I	/RD	/WR	MPUS	D7	D6	D5~D0
H : Parallel Input	↑	↑	↑	↑	↑	↑	↑	↑	↑
L : Serial Input	↑	↑	↑	–	–	–	SI	SCL	(HZ)

Note: "–" Indicates that it is fixed to either "H" or "L"

Parallel Interface:

When parallel interface is selected (P/S="H"), then it is possible to connect directly to either an 80-series MPU or a 68-series MPU by selecting the MPUS terminal to either "H" or "L".

MPUS	/CS1	CS2	D/I	/RD	/WR	D7~D0
L: 80-series MPU	↑	↑	↑	↑	↑	↑
H: 68-series MPU	↑	↑	↑	E	R/W	↑

Identification of data bus signals through a combination of D/I, /RD (E), /WR (R/W) signals as shown in the following table:

	68-Series	80-Series		Function
D/I	R/W	/RD	/WR	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Read status
0	0	1	0	Write control data (command)

Serial Interface:

When the chip is in an active state (/CS1="L" and CS2="H") the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the SI pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the 8th serial clock for the processing.

The D/I input is used to determine whether the serial data input is display data (D/I="H") or command data (D/I="L"). The D/I input is read and used for detection every 8th rising edge of the serial clock after the IC becomes active.

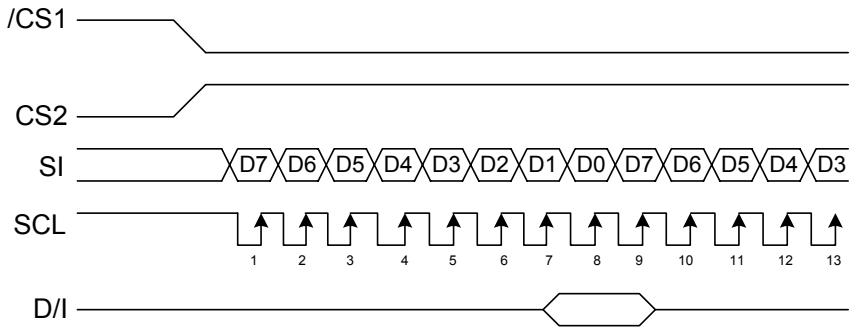


Fig. 2 Serial Interface Signal Chart

NOTE

1. *When the IC is not active, the shift registers and counter are reset to their initial states.*
2. *Reading is not possible while in serial interface mode.*
3. *Caution is required on the SCL signal when it comes to line-end reflections and external noise. It is recommended that operation be rechecked on the actual equipment.*

6.1.2 Chip Select

The EM65565A IC has two chip select terminals: /CS1 and CS2. The MPU interface or the serial interface is enabled only when /CS1="L" and CS2="H". When chip select is inactive, D0 to D7 enter a high impedance state and the D/I, /RD, and /WR inputs are inactive. When serial interface is selected, the shift register and the counter are reset.

6.1.3 Accessing the DDRAM and the Internal Registers

To match the operation frequencies between the MPU and *DDRAM* or internal register, the EM65565A performs a sort of LSI-LSI pipelining via the bus holder attached to the internal data bus.

When the MPU writes data to the *DDRAM*, once the data is stored in the bus holder, it is written to the *DDRAM* before the next data write cycle. Moreover, when the MPU reads the *DDRAM*, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.

There is a certain restriction in the read sequence of the *DDRAM*. It should be noted that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated during the second time data read. Thus, a dummy read is required whenever an address setup or write cycle operation is conducted. This relationship is shown in Figure 3.

6.1.4 Busy Flag

The busy flag is output to pin D7 by a read status command. When the busy flag is "1" it indicates that the EM65565A IC is executing its internal operations, and any command other than status read is rejected during this time. If the cycle time (t_{CYC}) is maintained, this flag need not be checked before each command. This makes it possible for vast improvements in MPU processing capabilities.

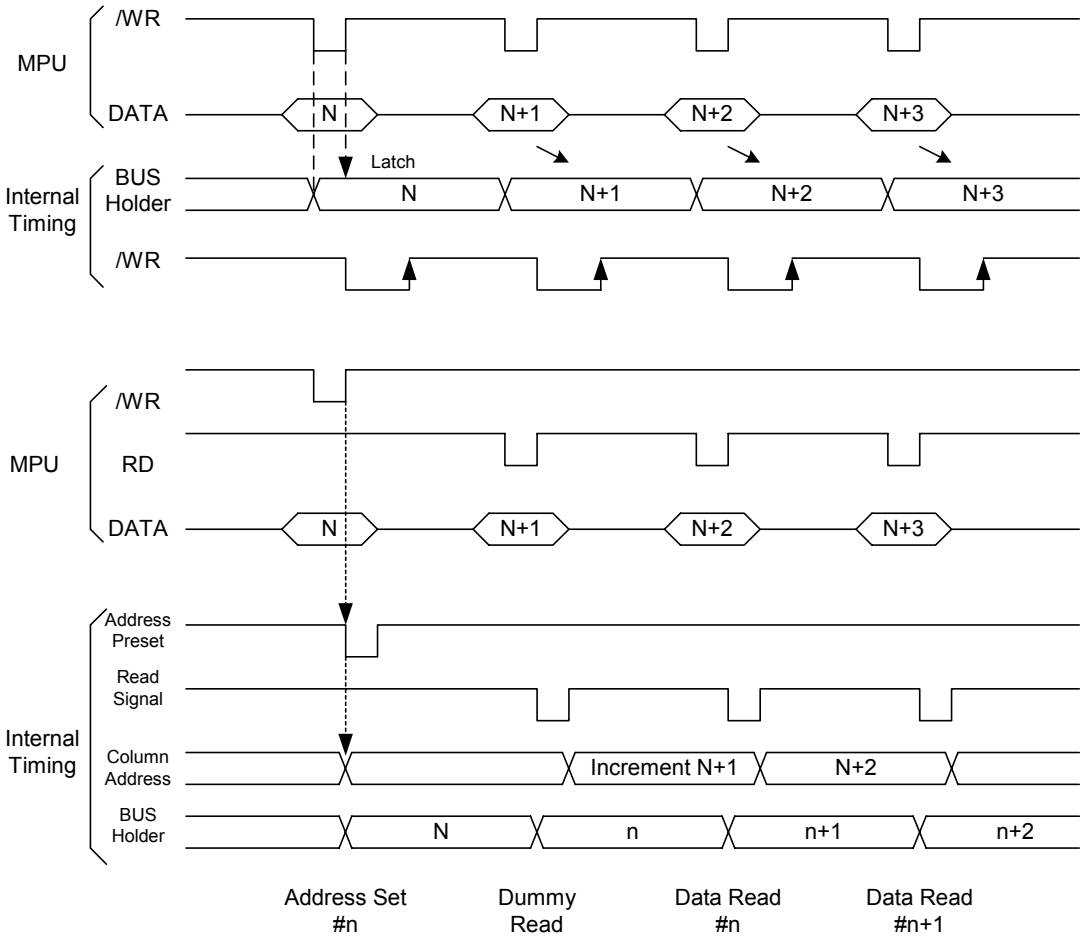


Fig. 3 DDRAM Read Sequence

6.1.5 Page Address Circuit

The page address of the *DDRAM* is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access. Page address 8 is the page for the RAM region used only by the static indicators, and only the display data D0 is used.

6.1.6 Line Address Circuit

The line address circuit specifies the line address corresponding to the common output when the *DDRAM* contents are displayed. Using the display start line address set command, the normally the top line of the display can be specified (which is the COM0 output when the common output mode is normal, and the COM63 output for the EM65565A when the common output mode is reversed. The display area is a 65 lines area for the EM65565A from the display start line address.

If the line address is changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

6.1.7 Column Addresses Circuit

The *DDRAM* column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the column address increment stops with 83H. Since the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to specify both the page address and the column address.

Furthermore, the ADC command can be used to reverse the relationship between the *DDRAM* column address and the segment output. Because of this, the constraints on the IC layout when the *LCD* module is assembled can be minimized.

6.1.8 Display Data RAM (DDRAM)

The *DDRAM* stores the dot data for the display, and it has 65×132 bits. It is possible to access the desired bit by specifying the page address and the column address. The D7 to D0 display data from the MPU corresponds to the *LCD* common direction. There are few constraints at the time of display data transfer when multiple EM65565A ICs are used. Hence, display structures can be created easily and with a high degree of freedom. Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the *DDRAM* is accessed asynchronously during a *Liquid Crystal Display*, it will not cause adverse effects on the display (such as flickering).

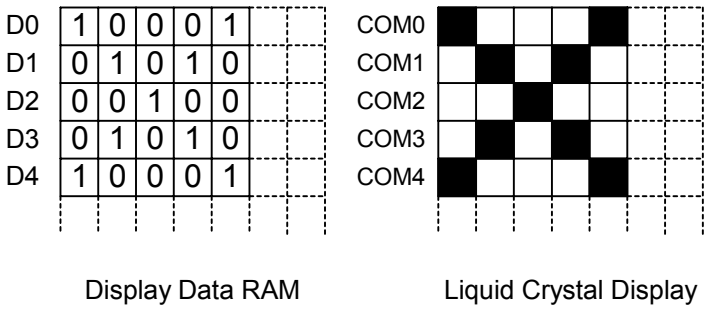


Fig. 4 Display Data RAM and Liquid Crystal Display Diagrams

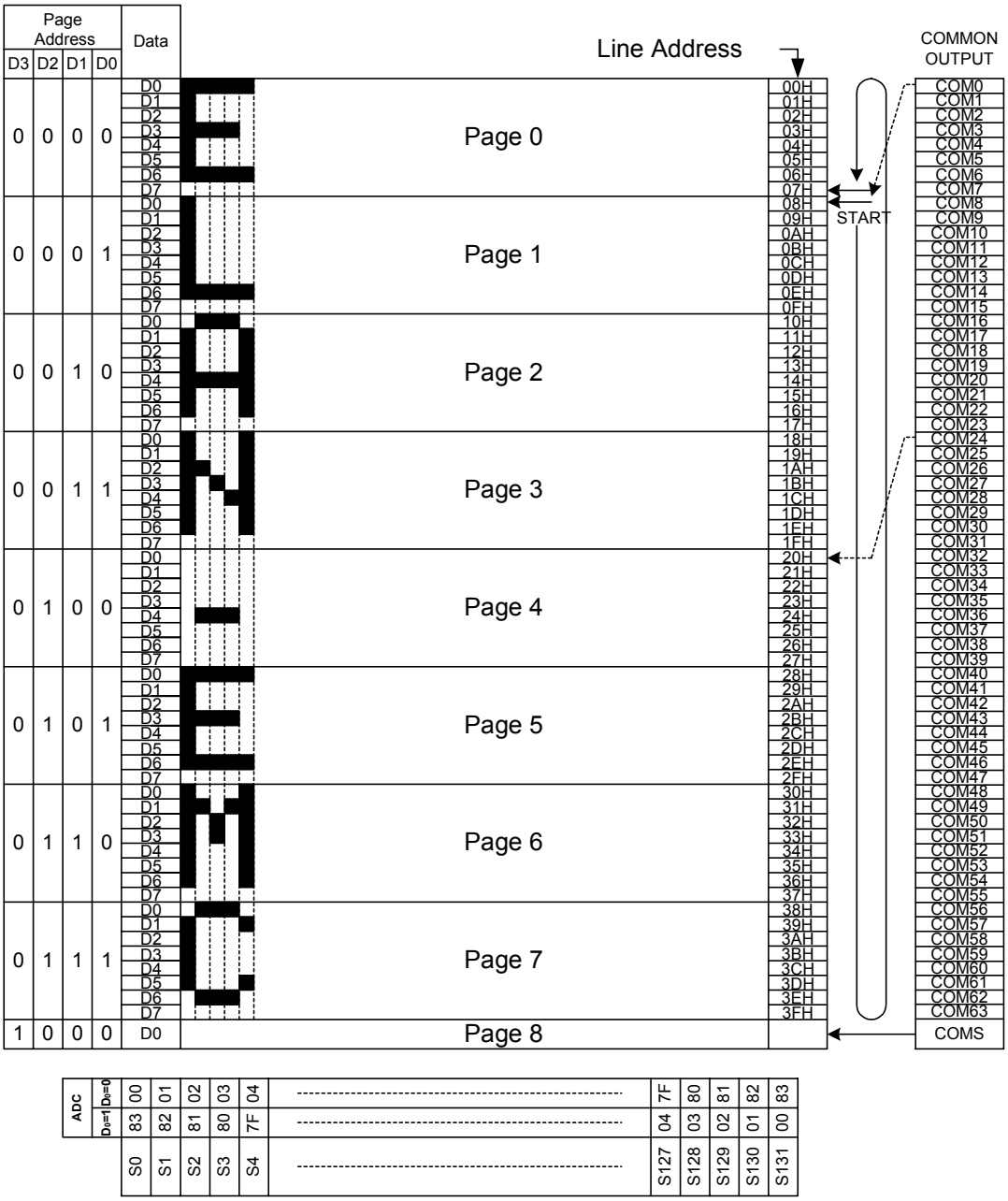


Fig. 5 Display Data RAM

6.1.9 Display Data Latch Circuit

The display data latch circuit temporarily stores the display data that is output to the liquid crystal driver from the *DDRAM*. Since the display normal/reverse status, display On/Off status, and display all points On/Off commands control only the data within the latch, they do not change the data within the *DDRAM* itself.

6.1.10 Oscillator Circuit

This is an RC-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S="H" and DCLKS="H". When DCLKS="L" the oscillation stops, and the display clock is input through the DCLK terminal.

6.1.11 Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading from the display data liquid crystal driver circuits is completely independent of accesses to the *DDRAM* by the MPU. Consequently, even if the *DDRAM* is accessed asynchronously during a *Liquid Crystal Display*, there is absolutely no adverse effect (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave from using a two-frame alternating current drive method, as shown in Figure 6, for the liquid crystal drive circuit.

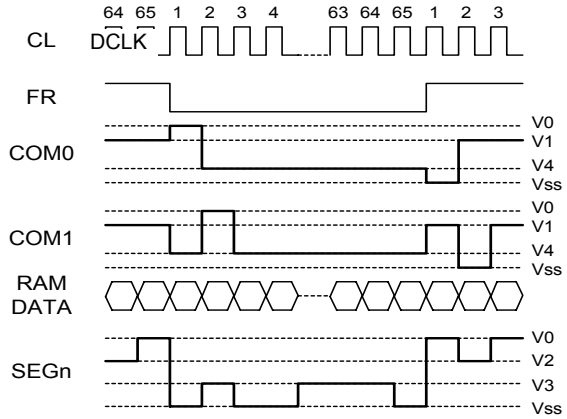


Fig. 6 Drive wave from a two-frame AC drive method

When several EM65565A ICs are used, the slave ICs must be supplied with display timing signals (FR, DCLK, /BCT) from the master ICs. Operating mode descriptions are shown in the following table:

Operating Mode		FR	DCLK	/BCT
Master (M/S = "H")	Internal oscillator circuit is enabled (DCLKS="H") Internal oscillator circuit is disabled (DCLKS="L")	O O	O I	O O
Slave (M/S = "L")	Internal oscillator circuit is enabled (DCLKS="H") Internal oscillator circuit is disabled (DCLKS="L")	I I	I I	I I

Note: O : Output I : Input

NOTE

When the EM65565A is used for the master/slave configuration, each of the DCLKS pins is set to the same level together.

6.1.12 Common Output Status Select Circuit

For the EM65565A IC, the COM output scan direction can be selected by the common output status select command (See Table below). Consequently, constrains in the IC layout at the time of *LCD* module assembly can be minimized.

Status	COM Scan Direction
Normal	COM0 → COM63
Reverse	COM63 → COM0

6.1.13 LCD Driver Circuits

These are 197 channels that generate four voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output. Figure 7 shows examples of the SEG and COM output waveform.

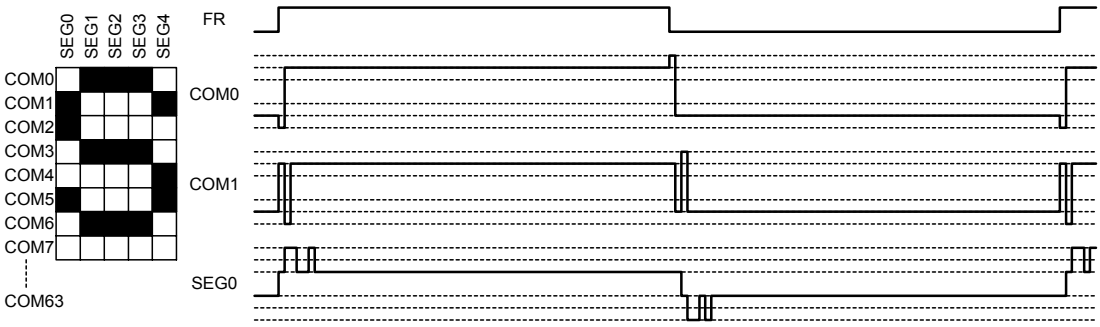


Fig. 7 SEG and COM Output Waveform

6.1.14 Power Supply Circuits

The power supply circuits have low-power consumption and can generate the voltage levels required for the liquid crystal drivers. They comprise of Booster (step-up voltage) circuits, Voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuit can turn the Booster circuits, the voltage regulator circuits and the voltage follower circuit On or Off independently through the use of the Power Control Set command. Hence, it is possible to make both external and internal power supplies function in parallel.

6.1.15 Step-up Voltage Circuit

Using the step-up voltage circuit built-in within the EM65565A IC, it is possible to produce a five times step-up, a four times step-up, a three times, and a two times step-up of the V_{CI} voltage levels. The step-up voltage relationship is shown in Figure 8.

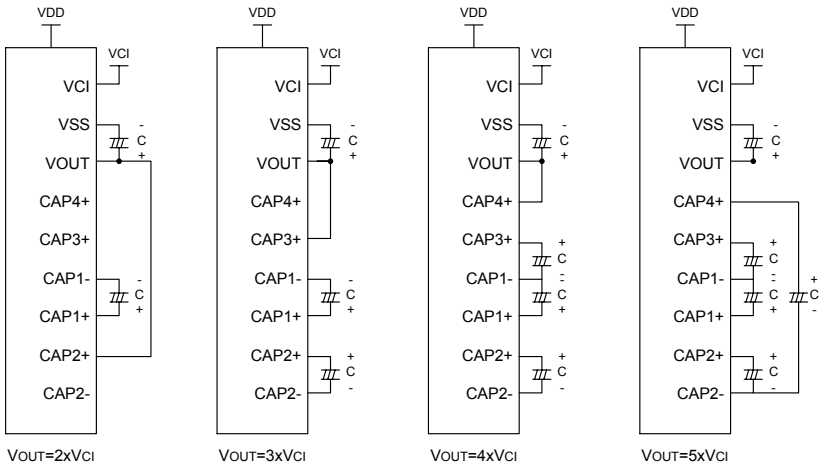


Fig. 8 Step-up Voltage Circuits

6.1.16 Voltage Regulator Circuit

The step-up voltage generated at V_{OUT}, outputs the *LCD* driver voltage V_0 through the voltage regulator circuit.

Since the EM65565A IC has an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

(a) Using the V_0 voltage regulator internal resistors

Through the use of the V_0 voltage regulator internal resistors and the electronic volume function, the liquid crystal power supply voltage V_0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the *LCD* brightness. The V_0 voltage can be calculated using equation A over the range where $V_0<V_{OUT}$.

$$V_0 = (1+\frac{Rb}{Ra})V_{EV} = (1+\frac{Rb}{Ra})(1-\frac{\alpha}{162})V_{REG} \text{ ---------- (A)}$$

$$\because V_{EV} = (1-\frac{\alpha}{162})V_{REG}$$

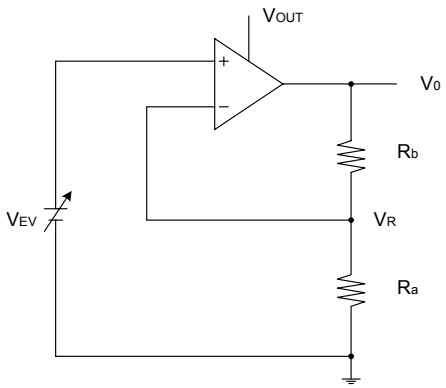


Fig. 9 Using the V0 Voltage Regulator Internal Resistors

The α is set to a particular level among the 64 possible levels through the use of the electronic volume function, depending on the data set in the 6-bit electronic volume register. The left table below shows the value for α, depending on the electronic volume register settings.

Rb/Ra is the V_0 voltage regulator internal resistor ratio and can be set to 8 different levels through the V_0 voltage regulator internal resistor ratio set command. The (1+Rb/Ra) ratio assumes the values shown in the right table below, depending on the 3-bit data settings in the V_0 voltage regulator internal resistor ratio register.

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			:			:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

D2	D1	D0	1+(Rb/Ra) Ratio	VREG External Input
0	0	0	3.0	1.5
0	0	1	3.5	2.0
0	1	0	4.0	2.5
0	1	1	4.5	3.0
1	0	0	5.0	3.5
1	0	1	5.5	4.0
1	1	0	6.0	4.5
1	1	1	6.4	5.0

The VREG is affected by Temperature interference, which is cause by a semiconductor material character. The Temperature coefficient is about –0.3% / °C.

(b) Using an External Resistance

The liquid crystal power supply voltage V_0 can also be set without using the V_0 voltage regulator internal resistors but by adding resistors Ra' and Rb'. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the *LCD* by controlling the *LCD* power supply voltage V_0 through commands. In the range where $V_0<V_{OUT}$, the V_0 voltage can be calculated using equation B, based on the external resistances Ra' and Rb'.

$$V_5 = (1+\frac{Rb'}{Ra'})V_{EV} = (1+\frac{Rb'}{Ra'})(1-\frac{\alpha}{162})V_{REG}' \text{ ---------- (B)}$$

$$\because V_{EV} = (1-\frac{\alpha}{162})V_{REG}$$

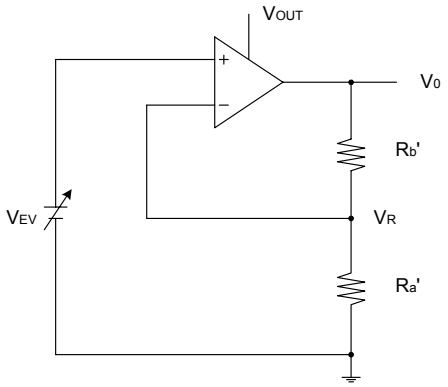


Fig. 10 Using External Resistance

6.1.17 Liquid Crystal Voltage Generator Circuit

The V_0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3 and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3, and V_4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for the EM65565A can be selected.

6.1.18 Power Supply Control Circuit

The built-in power supply circuit of the EM65565A Series IC has very low power consumption (normal mode: /PCT = "H"). However, for *LCD*s or panels with large loads, this low-power supply may cause the display quality to degrade. When this occurs, setting the /PCT terminal to "L" (high power mode) can improve the display quality. It is recommended that the display be checked on the actual equipment to determine whether or not to use this mode.

Moreover, if improvements to the display are inadequate even after high power mode has been set, then it is necessary to externally add a liquid crystal drive power supply.

6.1.19 Internal Power Supply Shutdown Command Sequence

This sequence is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

Step 1: Display OFF

Step 2: Display all points ON

Step 3: Internal power supply OFF

6.1.20 Reference Circuit Example

Figure 11 shows the reference circuit examples:

1. When all of the step-up circuit, voltage regulating circuit, V/F circuit, and the voltage regulator internal resistor are used, as shown in Fig 11-(a).
2. When all of the step-up circuit, voltage regulating circuit, V/F circuit, and the voltage regulator internal resistor are not used, as shown in Fig 11-(b).
3. When the voltage regulator circuit, V/F circuit and the V0 voltage regulator internal resistor are used, as shown in Fig 11-(c).
4. When the voltage regulator circuit and V/F circuit are used, and the V0 voltage regulator internal resistor is not used, as shown in Fig 11-(d).
5. When the V/F circuit is used, as shown in Fig 11-(e).
6. When any internal LCD power supply circuit is not used, as shown in Fig 11-(f).

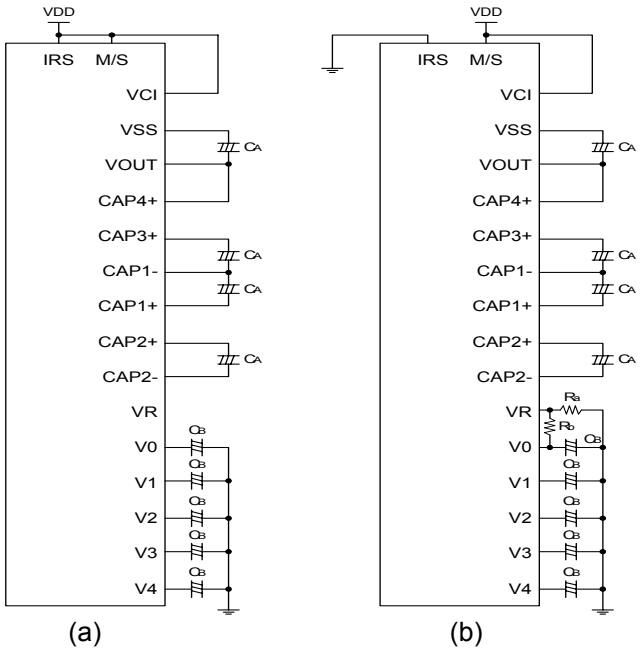


Fig. 11-(a~b) Reference Circuit Examples

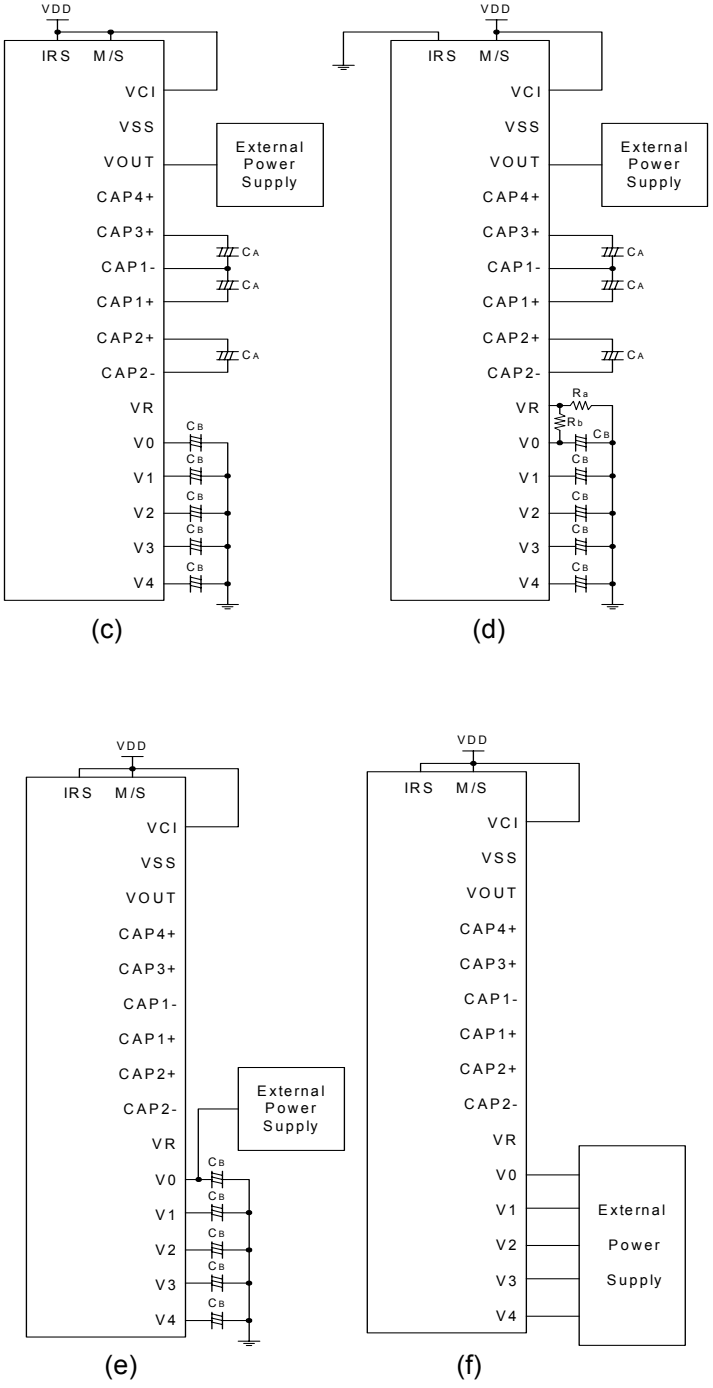


Fig. 11-(c~f) Reference Circuit Examples

Examples of shared reference settings, with V0 varied between 8V and 12V.

Item	Set Value	
CA	1.0 – 4.7	μF
CB	0.47 - 1.0	μF

NOTE

1. *Since the VR terminal input impedance is high, use short leads and shielded lines.*
2. *CA and CB are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.*
3. *Recommend X5R or X7R type Capacitors for CA and CB.*

6.1.21 Reset Circuit

When the /RST input falls to “L”, these LSI reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: normal (ADC command D0 = 0)
4. Power control resistor: (D2, D1, D0) = (0, 0, 0)
5. Serial interface internal register data clear
6. LCD power supply bias ratio: 1/9 bias
7. Read-modify-write OFF
8. Static indicator OFF: Static indicator register: (D1, D2) = (0, 0)
9. Display start line set to first line
10. Column address set to address 0
11. Page address set to page 0
12. Common output status normal
13. V0 voltage regulator internal power supply ratio set mode clear
14. V0 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
15. Electronic volume register set mode clear
16. Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0)
17. Test mode clear

When the reset command used only default settings, items 7 to 15 above are put into effect. The /RST terminal is connected to the MPU reset terminal, causing this IC to reinitialize simultaneously with the MPU. During power on, it is necessary to reinitialize using the /RST terminal.

In the EM65565A, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply an “L” signal to the /RST terminal when the external liquid crystal power supply is applied.

Even though the oscillator circuit operates while the /RST terminal is in “L”, the display timing generator circuit is stopped, and the DCLK, FR, FRS, and /BCT terminals are fixed to “H”. There is no influence on the D0 to D7 terminals.

7 Commands

Command	Command Code										Functions
	D/I	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	D	LCD display ON/OFF D=0: OFF, D=1: ON
Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
Column address set upper bit	0	1	0	0	0	0	1	Most column address				Sets the most 4 bits of the display RAM column address
Column address set lower bit	0	1	0	0	0	0	0	Least column address				Sets the least 4 bits of the display RAM column address
Status read	0	0	1	Status				0	0	0	0	Reads the status data
Display data write	1	1	0	Write data								Writes to the display RAM
Display data read	1	0	1	Read data								Reads from the display RAM
ADC select	0	1	0	1	0	1	0	0	0	0	D	Sets the display RAM address SEG output correspondence D=0: normal, 1: reverse
Display normal/reverse	0	1	0	1	0	1	0	0	1	1	D	Sets the LCD display normal/reverse D=0: normal, 1: reverse
Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	D	Display all points D=0: normal display D=1: all points ON
LCD bias set	0	1	0	1	0	1	0	0	0	1	D	Sets the LCD drive voltage bias ratio D=0: 1/9, D=1: 1/7
Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	Column address only increment at write: +1
End	0	1	0	1	1	1	0	1	1	1	0	Stop read-modify-write
Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
Common output mode select	0	1	0	1	1	0	0	D	*	*	*	Select COM output scan direction D=0: normal direction D=1: reverse direction
Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power Supply operating mode
V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio mode
Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Set the V0 output voltage electronic volume register
Electronic volume Register set	0	1	0	*	*	Electronic volume value						
Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	D	D=0: OFF, D=1: ON
Static indicator register set	1	0	1	*	*	*	*	*	*	Mode		Set the flashing mode
Power saver	0	1	0	1	0	1	0	1	1	1	0	Display OFF and display all points ON compound command
				1	0	1	0	0	1	0	1	
NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Don't use this command

7.1 Display ON/OFF

This command turns the display on and off. When the display OFF command is executed during a display all points ON mode, power saver mode is entered.

(AEH, AFH)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

Note: D = 0: Display is turned OFF

D = 1: Display is turned ON

7.2 Set Display Start Line

This command specifies a line address, thus, marking the display line that corresponds to C0.

(40H to 7FH)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	0	62
1	1	1	1	1	1	63

7.3 Set Column Address

This command specifies a DDRAM column address. When the column address is set, it is split into two parts (the upper 4-bits and the lower 4-bits). The column address is automatically incremented by 1 each time the MPU accesses from the set address to the DDRAM. Therefore, the MPU can access the data continuously. The column address stops to be incremented at address 131 (83H), and the page address is not changed continuously.

Upper bits (10H to 18H), Lower bits (00H to 0FH)

D/I	/RD	/WR(R/W)		D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	Upper bits	0	0	0	1	A7	A6	A5	A4
			Lower bits	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0		0	0	1	0	2
↓	↓	↓	↓	↓	↓	↓	↓	↓
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

7.4 Set Page Address

This command is used to specify a page address equivalent to a row address for MPU access to the DDRAM.

(B0H to B8H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page Number
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
0	1	1	1	7
1	0	0	0	8

7.5 Select ADC

This command specifies a segment driver direction. The column address is automatically incremented by 1 each time a read or a write display data operation is performed.

(A0H, A1H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

Note: D=0 clockwise output (forward) S0 (00H) → S131 (83H)

D=1 counterclockwise output (reverse) S0 (83H) → S131(00H)

7.6 Write Display Data

Write data from the data bus into the DDRAM. The column address is automatically incremented by "1" after a write operation.

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

7.7 Read Display Data

Read data from the DDRAM onto the data bus. The column address is automatically incremented by "1" after a read operation. When serial interface is used, reading the display data becomes invalid.

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

7.8 Read Status

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0

Busy: the busy bit indicates whether the driver accepts instruction or not
Busy=0: The driver will accept new instruction
Busy=1: No new instruction will be accepted

ADC:
ADC=0: Reverse (column address 131-n ↔ segment driver n)
ADC=1: Normal (column address n ↔ segment driver n)

ON/OFF: indicates the current status of the display
ON/OFF=0: Display ON
ON/OFF=1: Display OFF

Reset: indicates whether the driver is executing a hardware or software reset or if it is in normal operation mode
Reset=0: Normal operation
Reset=1: Currently executing a reset instruction

7.9 Read-Modify-Write

This instruction supersedes the column address register auto-increment after a data read. The current contents of the column address register are saved. This mode remains active until an “End” instruction is received.

When the “End” instruction is entered, the column address returns to the initial mode address prior to the input of the Read-modify-Write instruction. This function can reduce the MPU load when data change is repeated at a specific display area (such as cursor blinking). Any instruction can be used except for the column address set instruction which cannot be used.

(E0H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

7.10 End

This instruction cancels the read-modify-write instruction, returning the column address to the initial mode address.

(EEH)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

7.11 Reset

This instruction initializes the display data line register, hence, the column address, the page address counter, the V0 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and read-modify-write mode and test mode are released. It does not affect the contents of the DDRAM. When the power supply is turned on, a reset signal is entered in the /RST pin. The reset instruction cannot be used in place of the reset signal.

(E2H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

7.12 Display All Points ON

This command makes it possible to force all display points ON regardless of the content of the DDRAM. The contents of the DDRAM are maintained when this is done.

(A4H, A5H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	D	D=0: Normal display
											D=1: Display all point ON

7.13 Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the DDRAM. When this is done the DDRAM contents are maintained.

(A6H, A7H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	D	D=0: Normal (RAM data “H” LCD ON)
											D=1: Reverse (RAM data “L” LCD ON)

7.14 LCD Bias Set

This command specifies the voltage Bias ratio for the LCD

(A2H, A3H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	1	D	D=0 : 1/9 Bias
											D=1 : 1/7 Bias

7.15 Common Output Mode Select

This command can select the scan direction of the common output terminal

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	0	0	D	*	*	*	D=0 : Normal COM0→COM63
											D=1 : Reverse COM63→COM0

Note: * stands for don't care

7.16 Power Controller Set

This command sets the function of power supply circuit

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	0	0	1	0	1	D2	D1	D0	Voltage Follower Circuit D0=0: OFF, D0=1: ON Voltage Regular Circuit D1=0: OFF, D1=1: ON Booster Circuit D2=0: OFF, D2=1: ON

7.17 V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio.

(20H, 27H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	1+Rb/Ra ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								↓	↓	↓	↓
								1	1	1	Large

7.18 Electronic Volume

This command is used in pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other

Electronic Volume Mode Set:

When this command is input, the electronic volume register set command is enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used.

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set:

This command specifies the LCD drive voltage V0 to assume one of the 64 Voltage levels. When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0).

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	V_0
0	1	0	*	*	0	0	0	0	0	1	Small
					↓	↓	↓	↓	↓	↓	↓
					1	1	1	1	1	1	Large

Note: * stands for don't care

7.19 Static Indicator

This command controls the static drive system indicator display. This is used when one of the static indicator LCD drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal.

Static Indicator ON/OFF:

When the static indicator ON command is entered, the static indicator register set command is enabled.

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	D	D=0: OFF D=1: ON

Static Indicator Register Set:

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	Blinking at approximately 0.5 second
									1	0	Blinking at approximately 1 second
									1	1	Constantly ON

Note: * stands for don't care

7.20 Power Save

The power save mode is entered when the display all points ON is performed while in display OFF mode. The power save mode includes the sleep mode and the standby mode. The sleep mode is entered when the static indicator is OFF, and the standby mode is entered when the static indicator is ON. This mode is cleared by the command display all points OFF.

In sleep mode, all operations in the *LCD* display system stops, and remains in that state as long as there are no accesses from the MPU. In sleep mode operation, the oscillator circuit, the *LCD* power supply circuit, and all *LCD* driver circuits are halted.

In standby mode operation, the duty *LCD* display system operations are halted and only the static driver system for the indicator continues to operate, providing the minimum required current consumption for the static driver. In sleep mode operation, the *LCD* power supply circuit and the duty system LCD drive circuits are halted. The static drive system does not operate and the oscillator circuit continues to operate.

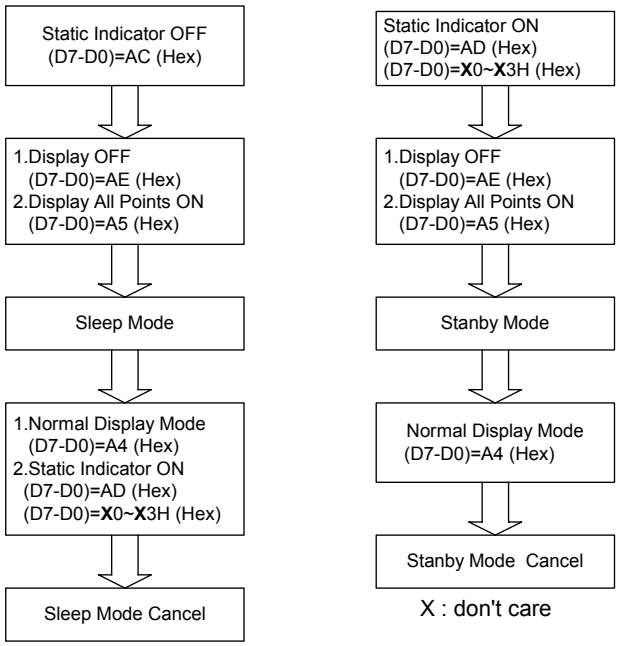


Fig. 12 Power Saving Method Flow Diagram

7.21 NOP

Non-operation command

(E3H)

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

7.22 Test

This command is for IC testing purposes. It can be cleared by applying an “L” signal to /RST input though the reset command or by using a NOP.

D/I	/RD	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

Note: * stands for don’t care

Initialization:

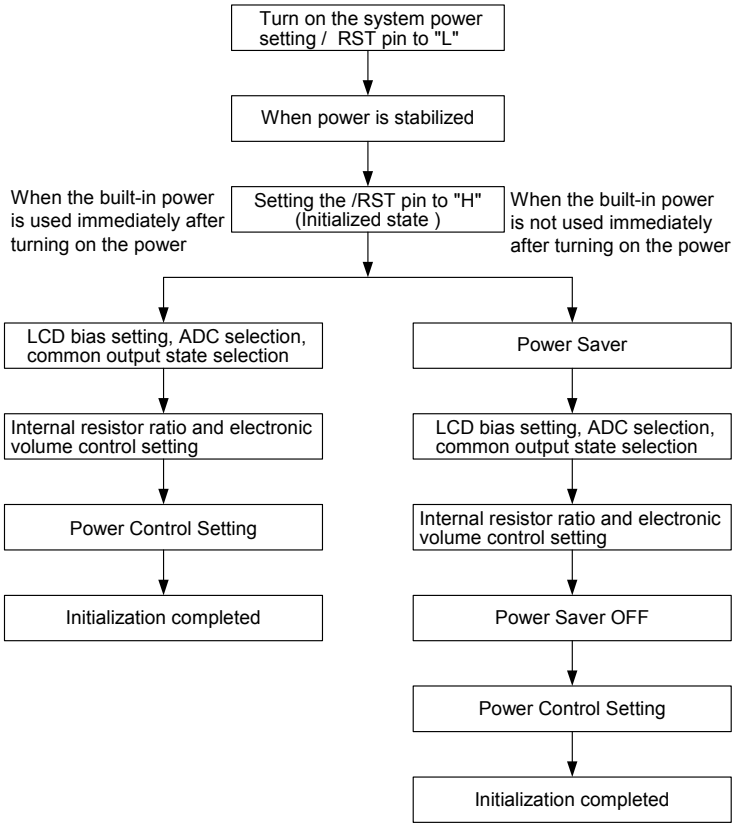


Fig. 13 Initialization Process Flow Diagram

The Relationship between oscillator frequency f_{OSC}, display clock frequency f_{CL} and the LCD frame rate frequency f_{FR}, is shown in the following table:

Oscillator Circuit	f_{CL}	f_{FR}
When the internal oscillator circuit is used (DCLKS="H")	$F_{OSC}/4$	$f_{CL}/65=f_{OSC}/(4*65)$
When the internal oscillator circuit is not used (DCLKS="L")	External input	$f_{CL}/(4*65)$

8 Absolute Maximum Ratings

Unless otherwise noted, V_{SS} = 0V

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	–0.3 to +4.0	V
Power supply voltage		V_{OUT}, V_0	-0.3 to 12	V
Power supply voltage		V_1, V_2, V_3, V_4	-0.3 to V_0	V
Input voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage		V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature		T_{OPR}	–30 to +85	°C
Storage temperature	TCP COG	T_{STR}	–55 to +100 –55 to +125	°C

Notes and Cautions

1. *Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$.*
2. *Permanent damage to the LSI may result if the LSI is used outside the absolute maximum ratings conditions. Moreover, it is recommended that in normal operation, the IC be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions, but may have a negative impact on the LSI reliability as well.*

9 DC Characteristics

Item		Symbol	Conditions & Application Pins		Rating			Units
					Min.	Typ.	Max.	
Operating Voltage (1)	Recommended voltage	V_{DD}	Pin V_{DD}		2.7		3.3	V
	Possible operating voltage		Pin V_{DD}		2.4		3.3	
Operating voltage (2)	Possible operating voltage	V_0			4.5		12	
		V_1, V_2			$0.6V_0$		V_0	
		V_3, V_4			V_{SS}		$0.4V_0$	
High-level input voltage		V_{IHC}	Pin D/I, D0-D7, /RD, /WR, /CS1, CS2, DCLKS, DCLK, FR, M/S, MPUS, P/S, /BCT, /RST, IRS, /PCT		$0.8V_{DD}$		V_{DD}	
Low-level input voltage		V_{ILC}			V_{SS}		$0.2V_{DD}$	
High-level output voltage		V_{OHC}	I_{OH}=-0.5mA	Pin D0-D7, FR, FRS, /BCT, DCLK	$0.8V_{DD}$		V_{DD}	
Low-level output voltage		V_{OLC}	I_{OL}=0.5mA		V_{SS}		$0.2V_{DD}$	
Input leakage current		I_{LI}	V_{IN}=V_{DD} or V_{SS} Pin D/I, /RD, /WR, /CS1, CS2, DCLKS, M/S, MPUS, P/S, /RST, IRS, /PCT		-1.0		1.0	µA
Output leakage current		I_{LO}	Pin D0-D7, FR, FRS, /BCT, DCLK		-3.0		3.0	
LCD driver ON resistor		R_{ON}	Ta=25°C, Pin COMn & SEGn	V_0=8V, |ΔV|=0.1V		3.2	5.4	kΩ

Item		Symbol	Conditions & Application Pins	Rating			Units
				Min.	Typ.	Max.	
Static consumption current		I_{SSO}	Pin V_{SS}, V_{SS2}		0.01	5	μA
Output leakage current		I_{0Q}	V_0=16V, Pin V_0		0.01	15	
Sleep mode current consumption		I_{DDS1}	VDD= 3V, 4 times booster		0.01	5	
Standby mode current consumption		I_{DDS2}	VDD= 3V, 4 times booster		4	8	
Display ON current consumption		I_{DDS3}	VDD= 3V, 4 times booster, All on pattern, Display on		220	290	
Display OFF current consumption		I_{DDS4}	VDD= 3V, 4 times booster, All on pattern, Display off	60	80	100	
Input terminal capacitance		C_{IN}	Ta=25°C, f=1MHz		5.0	8.0	pF
Oscillator Frequency	Internal oscillator	f_{OSC}	Ta=25°C Pin DCLK	18	22	26	kHz
	External input	f_{DCLK}		18	22	26	
Input voltage		V_{CI}	With double	2.4		3.5	V
			With triple	2.4		3.5	
			With quad	2.4		3	
			With five times			2.4	
Supply step-up output voltage		V_{OUT}	Pin V_{OUT}			12	
Voltage follower circuit operating voltage		V_{OUT}	Pin V_{OUT}	6		12	
Voltage follower circuit operating voltage		V_0	Pin V_0	4.5		12	
Base voltage		V_{REG}	Ta=25°C	2.128	2.15	2.172	

NOTE

1. *Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$.*
2. *Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V ±10%, Ta = –30°C to 85°C*
3. *Dynamic Current Consumption (1) during Display, with the Internal Power Supply OFF is Current consumed by total ICs when an external power supply is used.*

10 Timing Diagram

10.1 System Bus Read/Write Timing I (80-Series MPU)

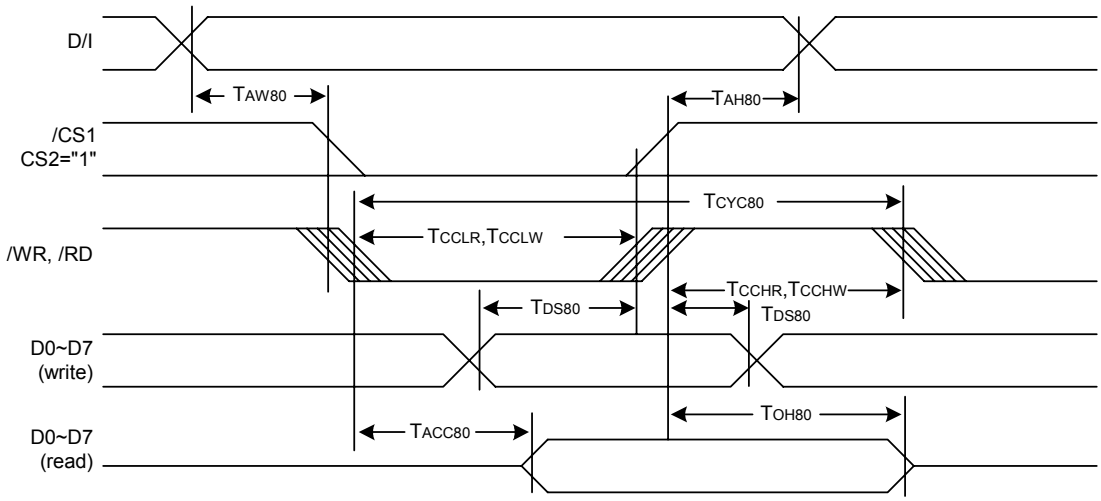


Fig. 14 System Bus Read/Write Timing Diagram for 80-Series MPU

(V_{DD}=2.4V to 3.3V, Ta=-30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	D/I	T_{AH80}		0	--	ns
Address setup time		T_{AW80}		0	--	ns
System cycle time	D/I	T_{CYC80}		300	--	ns
Control L pulse width (/WR)	/WR	T_{CCLW}		60	--	ns
Control L pulse width (/RD)	/RD	T_{CCLR}		120	--	ns
Control H pulse width (/WR)	/WR	T_{CCHW}		60	--	ns
Control H pulse width (/RD)	/RD	T_{CCHR}		60	--	ns
Data setup time	D0 to D7	T_{DS80}		40	--	ns
Address hold time		T_{DH80}		15	--	ns
/RD access time		T_{ACC80}	C_L=100pF	--	140	ns
Output disable time		T_{OH80}		10	100	ns

NOTE

1. *The input signal rise time and fall time (T_R, T_F) is specified at 15 ns or less. When the system cycle time is extremely fast, (T_R+T_F)≦(T_{CYC80}-T_{CCLW}-T_{CCHW}) for (T_R+T_F)≦(T_{CYC80}-T_{CCLR}-T_{CCHR}) are specified.*
2. *All timing is specified using 20% and 80% of V_{DD} as the reference.*
3. *T_{CCLW} and T_{CCLR} are specified as the overlap between /CS1 being "L" (CS2="H") and /WR and /RD being at the "L" level.*

10.2 System Bus Read/Write Timing (68-Series MPU)

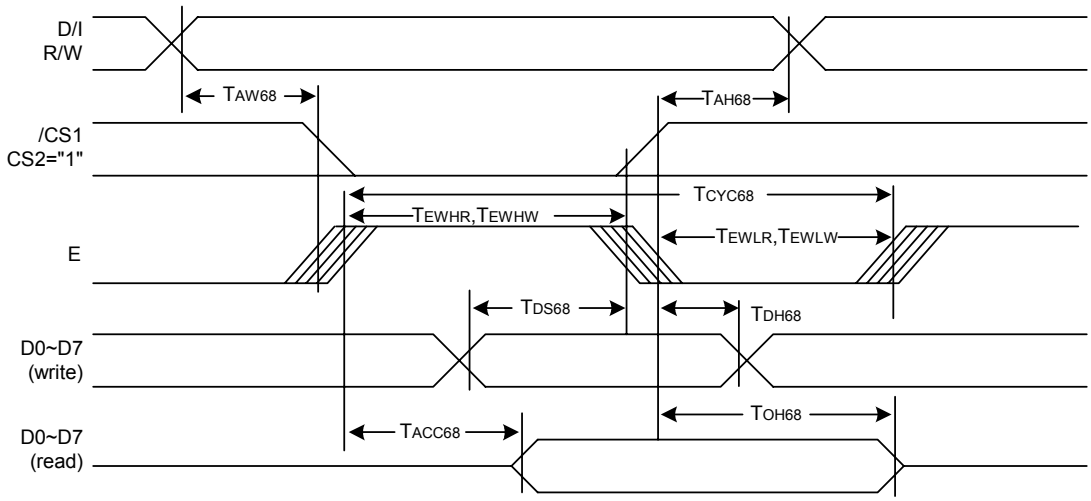


Fig. 15 System Bus Read/Write Timing Diagram for 68-Series MPU

(V_{DD}=2.4V to 3.3V, Ta=-30 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		D/I	T_{AH68} T_{AW68}		0 0	-- --	ns ns
System cycle time		D/I	T_{CYC68}		300	--	ns
Data setup time Data hold time		D0 to D7	T_{DS68} T_{DH68}		40 15	-- --	ns ns
Access time Output disable time			T_{ACC68} T_{OH68}	C_L=100pF	-- 10	140 100	ns ns
Enable H Pulse Time	Read Write	E	T_{EWHR} T_{EWHW}		120 60	-- --	ns ns
Enable L Pulse Time	Read Write	E	T_{EWLR} T_{EWLW}		60 60	-- --	ns ns

NOTE

1. *The input signal rise time and fall time (T_R, T_F) is specified at 15 ns or less. When the system cycle time is extremely fast, (T_R+T_F)≦(T_{CYC68}-T_{EWLW}-T_{EWHW}) for (T_R+T_F)≦(T_{CYC6}-T_{EWLR}-T_{EWHR}) are specified.*
2. *All timing is specified using 20% and 80% of V_{DD} as the reference.*
3. *T_{EWLW} and T_{EWLR} are specified as the overlap between /CS1 being "L" (CS2="H") and E.*

10.3 Serial Interface

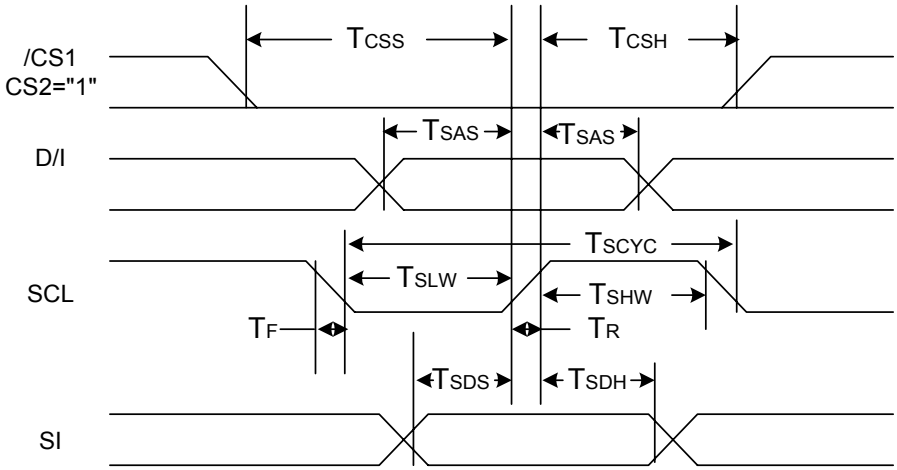


Fig. 16 Serial Interface Timing Diagram

(V_{DD}=2.4V to 3.3V, Ta=-30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period SDCLK "H" pulse width SDCLK "L" pulse width	SCL	T_{SCYC} T_{SHW} T_{SLW}		250 100 100	–	ns ns ns
Address setup time Address hold time	D/I	T_{SAS} T_{SHA}		150 150	–	ns ns
Data setup time Data hold time	SI	T_{SDS} T_{SDH}		100 100	–	ns ns
CS-SDCLK time	CS	T_{CSS} T_{CSH}		150 150	–	ns ns

1. The input signal rise and fall time (T_R, T_F) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of V_{DD} as the standard.

10.4 Display Control Output Timing

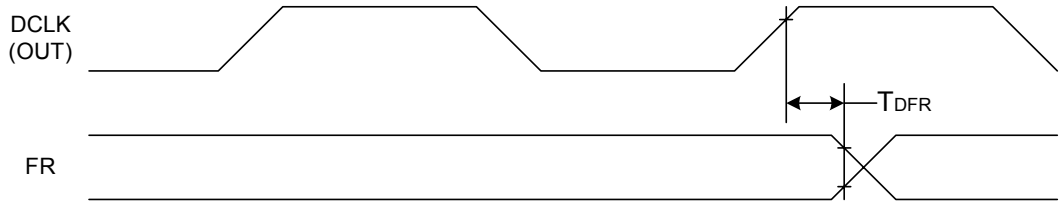


Fig. 17 Display Control Output Timing Diagram

(V_{DD}=2.4V to 3.3V, Ta=-30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	T_{DFR}	C_L=50pF	--	20	80	ns

10.5 Reset Timing

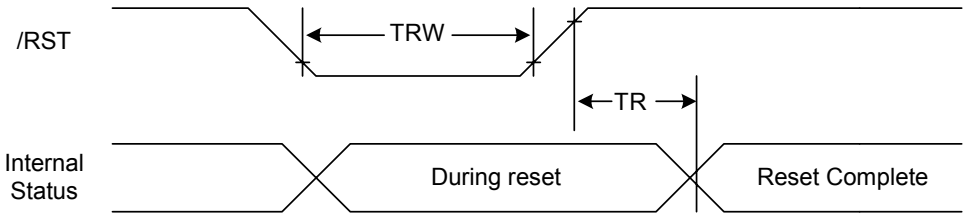


Fig. 18 Reset Timing Diagram

V_{DD}=2.4V to 3.3V, Ta=-30 to 85°C

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		T_R		–	–	1	μs
Reset "L" pulse width	/RST	T_{RW}		1	–	–	μs

*All timing is specified with 20% and 80% of V_{DD} as the standard.

11 Application Circuit

The MPU Interface (Reference example)

The EM65565A can be connected to either 80-Series MPU or 68-Series MPU. Moreover, using the serial interface it is possible to operate the EM65565A series ICs with fewer signal lines. The display area can be enlarged by using several EM65565A Series ICs. When this is done, the chip select signal can be used to select the individual ICs to access.

(1) 80-Series MPU

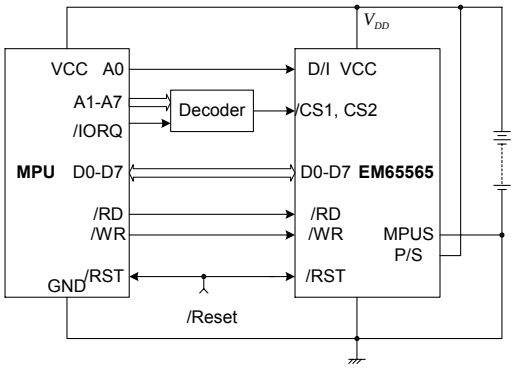


Fig. 19 Application Circuit Diagram for the 80 Series MPU

(2) 68-Series MPU

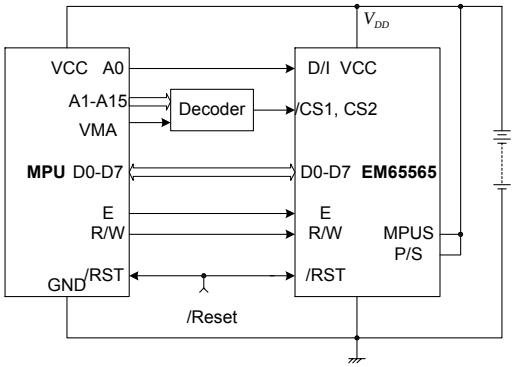


Fig. 20 Application Circuit Diagram for the 68 Series MPU

(3) Using the Serial Interface

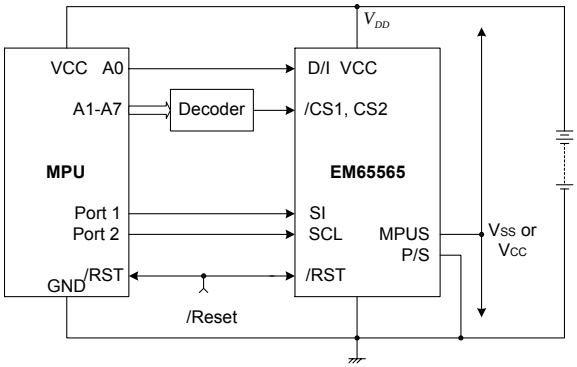


Fig. 21 Application Circuit Diagram when using Serial Interface

Connections Between the *LCD* Drivers (Reference Example)

The *LCD* area can be enlarged with ease through the use of multiple EM65565A ICs. Use the same equipment type.

EM65565A (master) → EM65565A(slave)

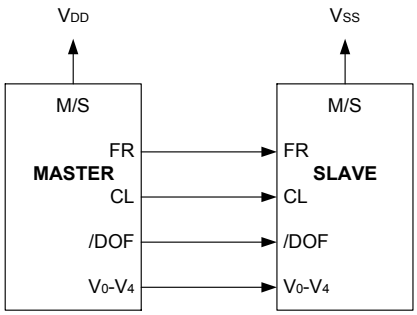


Fig 22 Master – Slave Circuit Diagram

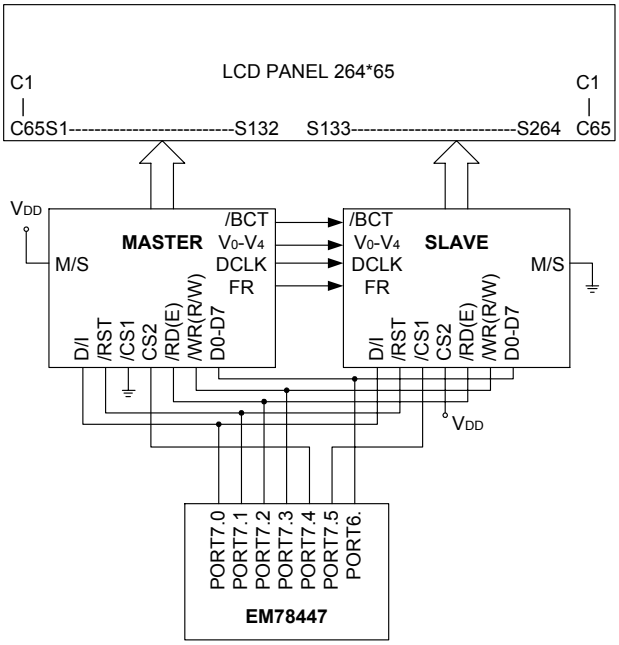
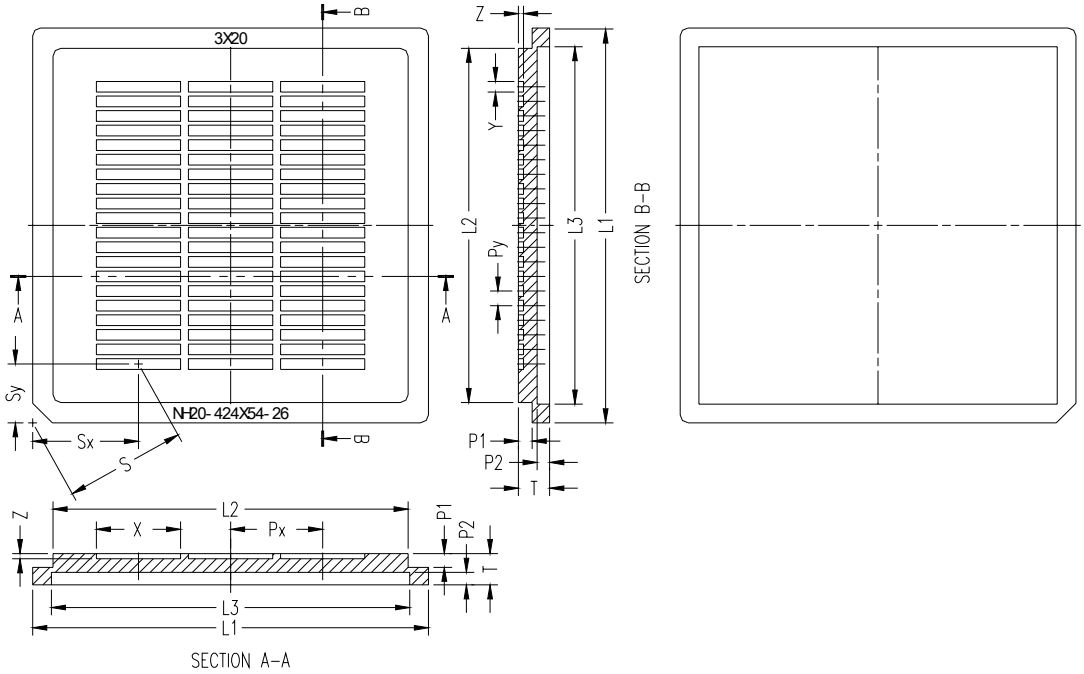


Fig. 23 Application Circuit Diagram for the LCD Panel 264x65

12 Recommended Cog Ito Traces Resistor

Interface	ITO Traces Resistance (Ω)
V_0 ~ V_4	Max = 300Ω
CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP4+, V_{OUT}	Max = 100Ω
V_{DD}	Max = 100Ω
V_{SS}	Max = 50Ω
/WR, /RD, /CS1, CS2, .., D7 ~ D0	Max = 3KΩ
/RST	5KΩ~10KΩ

12.1 Tray Information



12.2 Tray Outline Dimension

Unit: mm

Symbol	Dimension	Symbol	Dimension
L1	50.60	Z	0.66
L2	45.40	Px	11.77
L3	45.80	Py	1.87
T	4.00	Nx	3
Sx	13.53	Ny	20
Sy	7.54	N	60
S	15.49	P1	1.76
X	10.77	P2	1.60
Y	1.37		